A 640-Gb/s 4 × 4-MIMO D-Band CMOS Transceiver Chipset

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***Abstract*— This work presents a D-band (110–170 GHz) CMOS transceiver (TRX) chipset that covers a 56-GHz (114–170 GHz) signal-chain bandwidth. Both the transmitter (TX) and the receiver (RX) operate as heterodyne architectures with external intermediate frequency (IF) and local oscillator (LO) signals. An eight-way low-*Q* power-combined power amplifier (PA), a two-way low-*Q* power-combined low-noise amplifier (LNA), wideband-impedance-transformation passive mixers, common-source-based cascaded distributed amplifiers (DAs), and a low-loss wideband chip-to-waveguide printed circuit board (PCB) transition are proposed with improved bandwidth and linearity to support high-order wideband quadrature amplitude modulation (QAM) signals. The TRX chipset was fabricated using a 65-nm CMOS process. The TX achieves a 13-dBm saturated output power at 130 GHz with 1150-mW dc power. The RX achieves a 12-dB noise figure (NF) with 550-mW dc power. The proposed TRX chipset achieves a data rate of 200 Gb/s by 32QAM in the single-input–single-output (SISO) over-the-air (OTA) measurement at 0.32 m. A data rate of 150 Gb/s by 16QAM is realized with 43-dBi antennas at 15 m. Additionally, a 640-Gb/s 4 × 4 OTA line-of-sight multiinput multioutput (LOS-MIMO) is demonstrated at 0.52 m.**

***Index Terms*— 200 Gb/s, 640 Gb/s, 6G, CMOS, D-band, line-of-sight multiinput multioutput (LOS-MIMO), single-input–single-output (SISO), subterahertz (sub-THz), transceiver (TRX) chipset, wideband design.**

I. Introduction

THE ever-changing technological advances and social developments are placing increasingly higher demands on the throughput of wireless communications [1], [2], [3], [4], [5]. Recent new applications such as smart cars and high-speed indoor devices require data rates at hundreds of Gb/s levels [6]. Over the past decade, millimeter-wave (mm-Wave) and subterahertz (sub-THz) bands have been emerging as promising candidates for the 5G and 6G of high-speed wireless communications due to their high bandwidth capability [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21].

The reported wireless single-input–single-output (SISO) data rates with a bit error rate (BER) smaller than 10^{-3} in the past 20 years keep increasing. It could be seen that several wireless communication systems with data rates exceeding 100 Gb/s have been reported, demonstrating the potential and feasibility of next-generation high-speed wireless communication systems [21], [22], [23], [24], [25], [26], [27], [28], [29], [30]. However, such reported previous works operating at the sub-THz frequency band may suffer from low output power, limited bandwidth, and insufficient signal-to-noise ratio (SNR), which limit the wireless data rate and communication distance [19], [21], [23], [27], [29].

Considering the recent development trend [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], it is reasonable to set a higher target for wireless communication speed and distance compared with other state-of-the-art works. To achieve such kinds of targets, a D-band CMOS transceiver (TRX) chipset that covers a 56-GHz (114–170 GHz) signal-chain bandwidth is proposed in this work. The proposed TRX chipset includes wideband and high-linearity techniques that could support wideband high-order quadrature amplitude modulation (QAM) signals. In the SISO over-the-air

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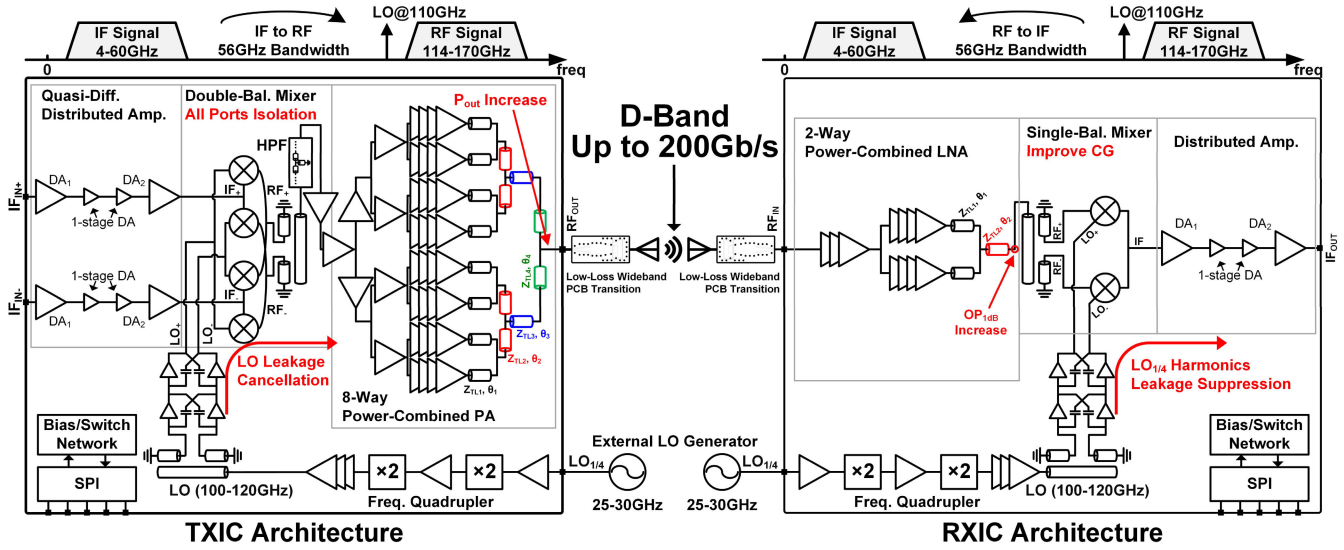


Fig. 1. Block diagram of the proposed D-band CMOS TRX chipset.

(OTA) measurements, the TRX chipset achieves a data rate of 200 Gb/s by 32QAM at a distance of 0.32 m. A data rate of 150 Gb/s by 16QAM is realized with 43-dBi antennas at a distance of 15 m. To further increase the wireless throughput, a 4 × 4 line-of-sight multiinput multioutput (LOS-MIMO) structure with four sets of TRX modules is also demonstrated with a total wireless throughput of 640 Gb/s at a distance of 0.52 m. All the measured results satisfy the error vector magnitude (EVM) rms requirements for BER $< 10^{-3}$ [31]. To the best of the author's knowledge, this work realizes the highest SISO and MIMO wireless data rate as of June 2024 compared with other reported works.

The rest of this article is organized as follows: Section II explains the TRX chipset system configuration, system link budget calculation, and LOS-MIMO setup. Section III shows the details of circuit block designs. Section IV describes the printed circuit board (PCB) interface designs. Section V demonstrates the measurement setups and results. Section VI concludes this article.

II. System Configuration

A. Overall System Configuration

Fig. 1 shows the block diagram of the TRX chipset and its frequency allocation. Both the transmitter (TX) and the receiver (RX) are heterodyne architectures with external local oscillator (LO) signals.

The proposed TX consists of a quasidifferential distributed amplifier (DA), a passive double-balanced upconversion mixer, an eight-way power-combined power amplifier (PA), a frequency quadrupler with LO amplifiers, and a serial peripheral interface (SPI) controller. The quasidifferential DA using cascaded topology with single-stage amplifiers provides 56-GHz bandwidth for intermediate-frequency (IF) signals from 4 to 60 GHz. The double-balanced mixer supports dc to 60 GHz at the IF port with theoretical all-ports isolation, greatly reducing the LO leakage to the radio frequency (RF) port [32]. A 90–180-GHz Marchand balun is placed at the output of the mixer to combine the differential RF signals. A high-pass filter (HPF) is placed after the balun to reduce unwanted frequency components. The PA combines eight ways using transmission lines (TLs) to improve the output power, and it has a 56-GHz RF bandwidth from 114 to 170 GHz.

The proposed RX includes a two-way power combined low-noise amplifier (LNA), a passive single-balanced down-conversion mixer, a single-ended DA, a frequency quadrupler with LO amplifiers, and an SPI controller. The two-way power-combined LNA utilizes a similar combiner with the PA to improve LNA linearity for wideband signals. It also provides the same RF bandwidth from 114 to 170 GHz as the PA. The single-balanced mixer reduces $LO_{1/4}$ harmonics leakage to the IF port, and it also improves conversion gain (CG) and linearity by using differential LO signals [32]. The same balun with the TX is placed at the mixer input port to generate differential signals. The DA in the RX shares the same design as the TX, and the TX and RX chips also use the same LO chain design. The 25–30-GHz external $LO_{1/4}$ signal's frequency is quadrupled inside the chip, and a differential LO signal is generated to drive the mixers. The differential LO amplifiers use the capacitive-cross-coupled neutralization architecture to increase the gain and reduce the differential mismatch of the LO signals [33]. The biases and switches are controlled through the SPI controller in both the TX and the RX.

To keep the wideband and low-loss characteristics of the connection between the RF ports of the TRX chipset and antennas, which is essential for the communication distance and speed, a PCB transition from the CMOS chip to the standard waveguide flange (UG-387) is included in both the TX and RX modules. It can cover an RF bandwidth from 112 to 170 GHz with a flat frequency response.

In general, high-order QAM SISO signals with data rates up to 200 Gb/s are supported in the entire signal chain with the proposed TRX chipset.

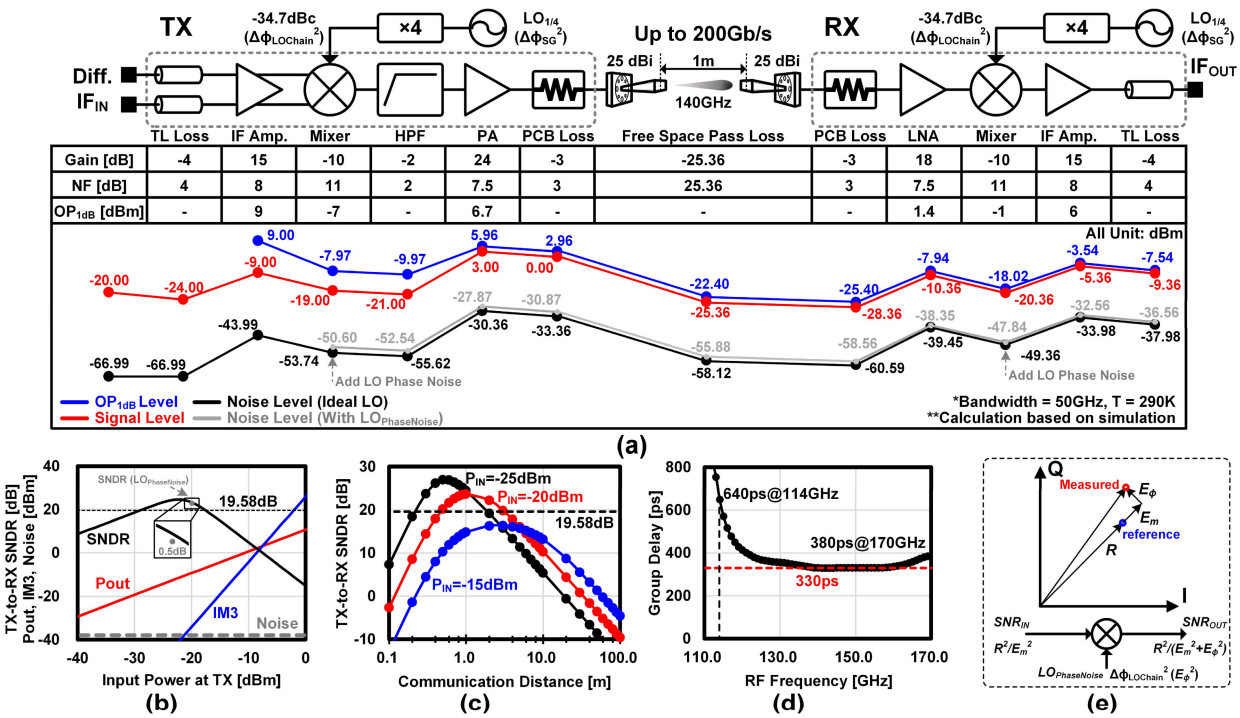


Fig. 2. Link budget calculations of the proposed TRX chipset. (a) Power-level diagram of the TRX. (b) Calculated TX-to-RX SNDR versus input power at 1 m. (c) Calculated TX-to-RX SNDR versus communication distance with $P_{IN} = -25$ dBm, $P_{IN} = -20$ dBm, and $P_{IN} = -15$ dBm. (d) Simulated group delay of the overall link. (e) Degradation of the mixer SNR due to the LO phase noise.

TABLE I
REQUIRED SNR FOR BER $< 10^{-3}$

Modulation	BPSK	QPSK	16QAM	32QAM	64QAM	128QAM	256QAM
SNR (MER) [dB]	5.16	9.80	16.54	19.58	22.55	25.49	28.41
EVM_{RMS} [%]	55.21	32.36	14.89	10.50	7.46	5.32	3.80
EVM_{RMS} [dB]	-5.16	-9.80	-16.54	-19.58	-22.55	-25.49	-28.41

B. TX-to-RX Link Budget Calculation

To evaluate the effective data rate, a BER threshold value is selected as 10^{-3} to maintain a sufficient coding rate after the forward error correction (FEC) [14], [21], [24], [29]. For the M-order QAM signal, the required SNR can be calculated by the following equation [34]:

$$\mathrm{SNR} = \log_2 M \frac{M-1}{3\log_2\sqrt{M}}\left(\mathrm{erfc}^{-1}\left(\frac{\mathrm{BER}\cdot\log_2\sqrt{M}}{1-\frac{1}{\sqrt{M}}}\right)\right)^2 \tag{1}$$

where all variables are in plain ratios. In the measurement, EVM_{rms} values are used for the BER evaluation. The relationship between SNR, EVM, and modulation error ratio (MER) is explained in the following equation:

$$\mathrm{SNR[dB]} = \mathrm{MER[dB]} = -20\lg(\mathrm{EVM_{rms}}[\%]/100). \tag{2}$$

Table I summarizes the required SNR (MER) and EVM_{rms} (not EVM_{MAX}) [31].

To get BER $< 10^{-3}$, the SNR at the final output port must be larger than the values of Table I. In real communication systems, nonlinearity also needs to be considered, so that the signal-to-noise-and-distortion ratio (SNDR) is used here to estimate system performance. The SNDR is defined as the ratio between signal power and the sum of noise and intermodulation distortion (IM3) [24].

Fig. 2(a) illustrates the link budget calculations, based on the simulation results of the proposed TRX chipset in the SISO case. The calculation utilizes a 140-GHz signal with a 50-GHz bandwidth at 290 K. The cascaded output 1-dB compression point (OP1dB), signal power level, and noise power level are presented at each stage. The input power level is -20 dBm to make sure that SNDR has sufficient margin. Here, the target modulation is 32QAM. Fig. 2(b) depicts the calculated TX-to-RX SNDR versus the TX input power at 1 m. The TX input power should be larger than -32 dBm and smaller than -18 dBm to maintain an SNDR exceeding 19.58 dB. Fig. 2(c) shows the calculated TX-to-RX SNDR versus the communication distance for various TX input powers of -25, -20, and -15 dBm, respectively. For short-range cases, a lower input power level can be employed to ensure enough SNDR, whereas a higher input power level with binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK) can be utilized for long-range scenarios.

The upper calculation assumes a flat group delay and the use of ideal LO signals without any phase noise. It is evident that these two factors exert a considerable influence on the SNDR in actual wireless communications, and thus, they must be considered in the link budget calculations.

The group delay represents the distortion of the modulated signals. Fig. 2(d) shows the simulated group delay of the overall link. A nonflat group delay will cause intersymbol interference (ISI), which makes EVM worse. The degradation

of the EVM can be calculated by obtaining the phase ripples from the group delay [35]. However, this EVM deterioration resulting from nonflat group delay can be reduced by using an equalization function, thereby minimizing signal distortion and enhancing the EVM performance [36]. This is utilized in the measurement mentioned in Section V.

Additionally, nonideal LO signals invariably contain phase noise, which results in a deterioration of the SNR via mixers. The external $LO_{1/4}$ signal features an integrated phase noise component, $\Delta\phi^2_{SG}$, which can be calculated by the following equation [37]:

$$\Delta\phi^2_{SG} = 2\int_{1\,\text{kHz}}^{25\,\text{GHz}} L_{SG}(f)df \tag{3}$$

where $L_{SG}(f)$ is the single sideband (SSB) phase noise of the external $LO_{1/4}$ signal. Therefore, the LO chain will output an integrated phase noise, $\Delta\phi^2_{LOChain}$, whose value is dependent on $\Delta\phi^2_{SG}$, frequency quadrupler, and amplifiers. This value is added directly to the output by the mixers while maintaining the same level [37]. If the input of the mixer has a certain SNR value, SNR_{IN}, the SNR degradation due to the LO phase noise can be calculated by the following equation [38], [39]:

$$\frac{1}{\text{SNR}_{\text{OUT}}} = \frac{E_m^2 + E_\phi^2}{R^2} = \frac{1}{\text{SNR}_{\text{IN}}} + \Delta\phi^2_{\text{LOChain}} \tag{4}$$

where R represents the reference vector, E_m is the magnitude error vector, and E_ϕ is the phase error vector. Fig. 2(e) shows the influence of the LO phase noise, as explained in (4).

The revised link budget considering the phase noise of the LO signal is also illustrated in Fig. 2(a) and (b). With the inclusion of LO phase noise in the calculations, the overall link SNDR exhibited a reduction of approximately 0.5 dB when TX $P_{in} = -20$ dBm.

C. 4 × 4 LOS-MIMO Configuration

Attaining a higher data rate with an SISO system may prove to be challenging, particularly considering the necessity to guarantee both a more expansive bandwidth and a higher SNDR. In contrast, MIMO systems can provide higher data rate capacity without the necessity of increasing bandwidth requirements. LOS-MIMO systems are particularly well-suited for point-to-point wireless communications, offering better spectrum efficiency [40].

Fig. 3 provides an overview of the D-band 4 × 4 LOS-MIMO with the singular value decomposition (SVD) architecture [41]. The entire LOS-MIMO system is composed of four TX/RX elements, a matrix V, and a matrix U*. The RF signals contain four streams occupying the same frequency band, which means that f_{RF1}, f_{RF2}, f_{RF3}, and f_{RF4} are the same. In this instance, the SVD is applied to the TX–channel–RX matrix

$$\mathbf{R}\cdot\mathbf{H}\cdot\mathbf{T} = \mathbf{U}\cdot\mathbf{\Sigma}\cdot\mathbf{V}^* \tag{5}$$

where $\mathbf{H}$ represents the channel matrix. $\mathbf{T}$ and $\mathbf{R}$ are the diagonal matrices that represent the TX and the RX, respectively. The matrices $\mathbf{U}$ and $\mathbf{V}^*$ are unitary, and $\mathbf{\Sigma}$ is the diagonal matrix with singular values equal to the square root of the eigenvalues of the matrix $\mathbf{RHT}\cdot(\mathbf{RHT})^*$ [36], [37]. If the four-stream input matrix $\mathbf{X}$ is applied to the system, the resulting final output matrix $\mathbf{Y}$ is given by

$$\begin{aligned}\mathbf{Y} &= \mathbf{U}^*\cdot\mathbf{R}\cdot\mathbf{H}\cdot\mathbf{T}\cdot\mathbf{V}\cdot\mathbf{X} = \mathbf{\Sigma}\cdot\mathbf{X}\\ &= \begin{bmatrix}\sqrt{\boldsymbol{\lambda_1}}\mathbf{x_1} & \cdots & \mathbf{0}\\ \vdots & \ddots & \vdots\\ \mathbf{0} & \cdots & \sqrt{\boldsymbol{\lambda_4}}\mathbf{x_4}\end{bmatrix}\end{aligned} \tag{6}$$

where $\boldsymbol{\lambda_1}, \boldsymbol{\lambda_2}, \boldsymbol{\lambda_3}$, and $\boldsymbol{\lambda_4}$ represent the eigenvalues of the $\mathbf{RHT}\cdot(\mathbf{RHT})^*$. This method allows for the decomposition of MIMO signals. In certain instances, the matrix $\mathbf{V}$ can be designated as the identity matrix $\mathbf{I}$, thereby enabling the MIMO signal decomposition to be conducted exclusively at the RX end [41]. Moreover, for the MIMO system with high isolation between different streams, the $\mathbf{RHT}$ is approximately equal to the identity matrix $\mathbf{I}$ if no gain and loss are considered, which implies that $\mathbf{Y} = \mathbf{X}$, and the MIMO system can be reduced to a combination of four SISO systems.

In this work, high-directivity H–V-polarized antennas are utilized to achieve high isolation, so that the SNDR analysis with the SISO case is also useful for the MIMO system. The generation and decomposition of the MIMO signals are performed using external equipment.

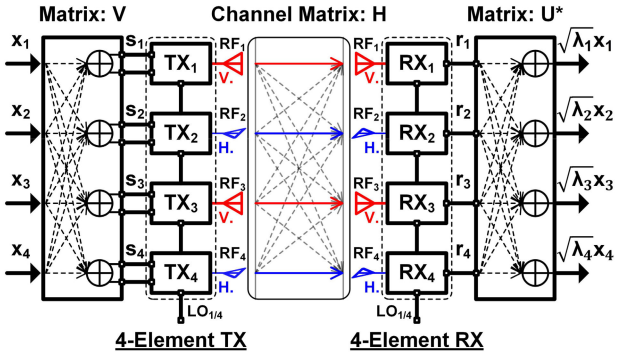


Fig. 3. Overview of the D-band 4 × 4 LOS-MIMO with the SVD.

III. Circuit Block Design

This section presents a comprehensive analysis of the circuit blocks, including the PA, LNA, DA, mixers, and LO chains. The results of the simulations and measurements are also presented.

A. Power-Combined PA and LNA

Fig. 4(a) explains an in-phase TL-based power combining and low-Q wideband impedance matching techniques in PA design. The PA unit of driving stages uses a TL-embedded gain-boosting structure, which could enhance the CMOS transistor's gain performance at D-band frequencies [43].

The embedded structure comprises two principal parameters, namely the lengths of TL_1 and TL_2, which are employed to regulate the gain response across the D-band frequencies. The simulation results show that longer lengths of TL_1 and

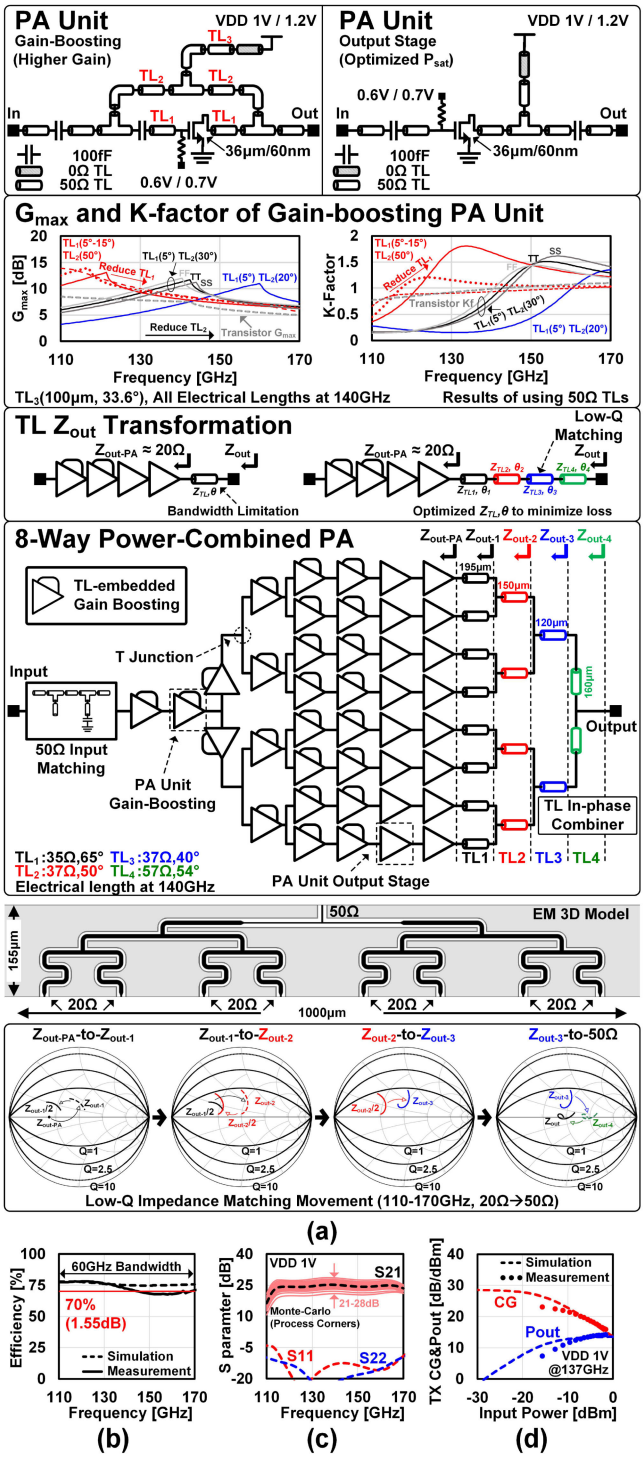


Fig. 4. Proposed PA design. (a) PA unit designs and the low-Q power combining technique. (b) Passive efficiency of the eight-way combiner. (c) Simulated PA S-parameters. (d) TX CG and P_{out} at 137 GHz.

TL_2 yield a peak at a lower frequency. A shorter TL_1 is preferable, as a longer TL_1 results in a reduction in the K factor. Furthermore, all TLs within the embedded structure are 50 Ω. Additionally, the simulation is based on the typical–typical (TT) process corner.

The gain-boosting structure incorporates power feedback at its output port, which constrains the output power. The PA output stage utilizes a single common source transistor without any gain-boosting structure to achieve the maximum possible saturated output power.

Both these PA units utilize a low characteristic impedance TL to connect to the power network, which is equivalent to a large capacitance shunted to the ground (GND). This ensures that the single-ended power network has minimal impact on the impedance matching. The D-band transistor model was created using the methods described in [44].

The PA unit has a 20-Ω output impedance $Z_{\text{out-PA}}$, and it can be tuned by the addition of a series of TL. For wideband matching design, the impedance needs to stay inside the low-Q region on the Smith chart [45]. In the eight-way combiner design, four different kinds of TLs (TL_1, TL_2, TL_3, and TL_4) are utilized to achieve the wideband power combining and impedance matching from 20 (PA) to 50 Ω (load). The combiner is designed based on electromagnetic (EM) simulation using high-frequency structure simulator (HFSS), and its layout size is 1 × 0.155 mm. The impedance trajectory from 110 to 170 GHz is plotted on the Smith chart, which shows that a low-Q matching ($Q < 1$) is realized in this design. According to the stand-alone back-to-back combiner test element group (TEG) measurement, a 70% average passive efficiency is achieved over the whole D-band as shown in Fig. 4(b), which is calculated by the following equation:

$$\eta_{\text{passive}} = 10^{(0.5\times S21)/10} \times 100\% \tag{7}$$

where $S21$ (dB) represents the de-embedded insertion loss of the back-to-back eight-way combiner. It is assumed that a low return loss is present in (7).

Fig. 4(c) shows the simulated S-parameters of the proposed PA. The PA has a 25-dB gain with $S11$ and $S22$ values smaller than −10 dB across the 114–170-GHz frequency range. Additionally, a Monte-Carlo simulation for different process corners is performed to see the variation of the PA's gain, which is from 21 to 28 dB in the most unfavorable situations. The measured TX saturated output power at 137 GHz is 13 dBm, while the saturated power of a PA unit is 5.5 dBm, which is shown in Fig. 4(d). The reasons for the discrepancies in Fig. 4(d) will be discussed in Section V-A.

The LNA shares the same amplifier unit and combines technique with PA to enhance the OP1dB. Fig. 5(a) explains the LNA's topology and the EM 3-D model of the combiner. The combiner size is 0.25 × 0.175 mm. Fig. 5(b) shows the simulated LNA S-parameters. The LNA has an 18-dB gain with $S11$ and $S22$ smaller than −10 dB across the same frequency range as PA. A Monte-Carlo simulation incorporating various process corners is also conducted to assess the impact of transistor mismatch. The result shows a gain variation of 15–19.2 dB in the worst case.

Fig. 5(c) shows an average 9-dB noise figure (NF) in the simulation. Fig. 5(d) illustrates the simulated gain and P_{out} as a function of the LNA input power. The realization of a −14.5-dBm input 1-dB point through the two-way power combining is also demonstrated.

B. Cascaded Common-Source-Based DA

Fig. 6(a) illustrates the design of the DA with a bandwidth of 4–60 GHz. The conventional DA can achieve a wide

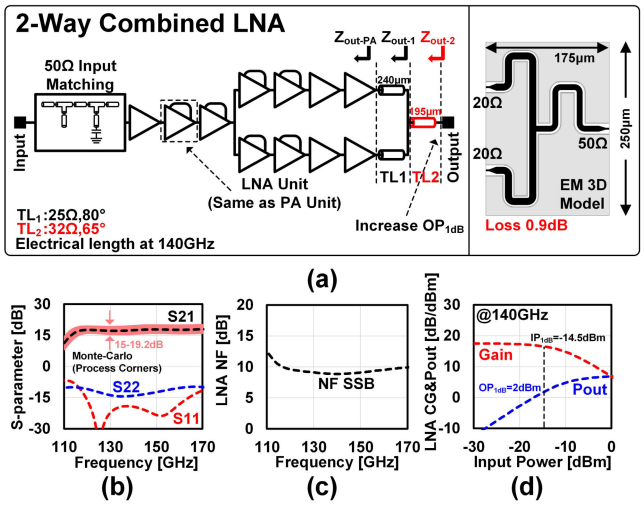


Fig. 5. Proposed LNA design. (a) LNA schematic. (b) Simulated LNA S-parameters. (c) Simulated LNA SSB NF. (d) LNA gain and P_{out} at 140 GHz.

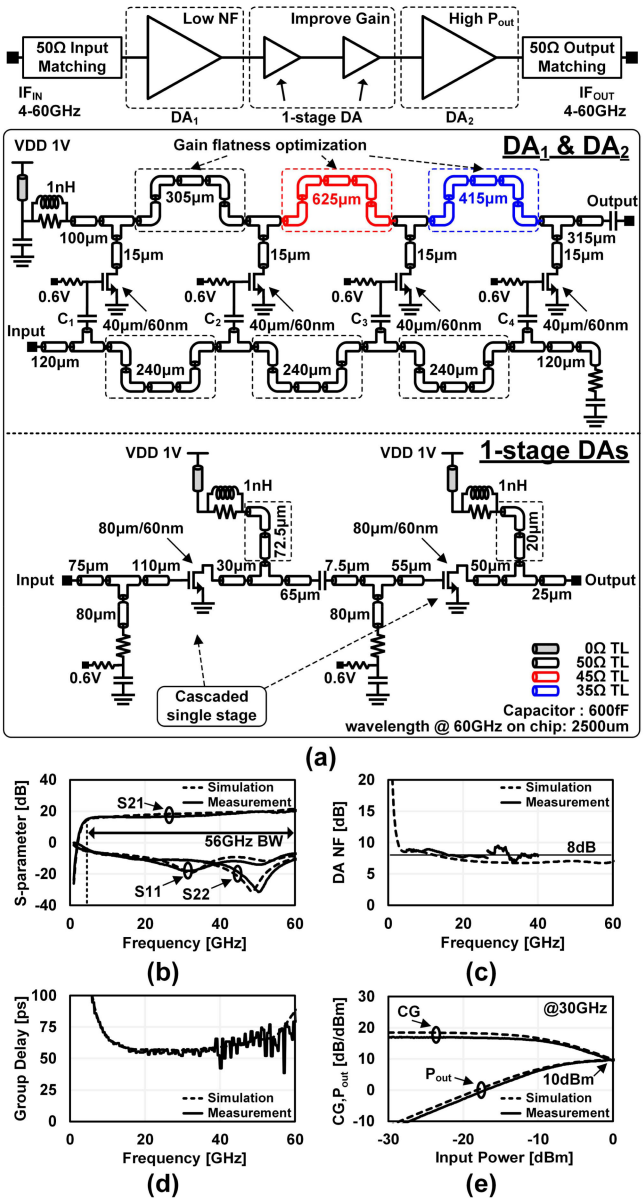


Fig. 6. Proposed DA design. (a) DA's schematic. (b) DA S-parameters. (c) DA NF. (d) DA group delay. (e) DA CG and P_{out}.

bandwidth but suffers from lower gain due to the additive gain mechanism [46], [47]. In this work, a common-source-based cascaded DA is utilized to maintain high gain, low NF, and high linearity at frequencies exceeding 60 GHz [47]. The first (DA_1) and the third (DA_2) stages are designed as conventional DAs with 40-μm/60-nm transistors. The TLs are tuned to achieve optimal gain flatness. It can be observed that the TLs on the output side of the DA_1 and DA_2 are longer than those on the input side. This is due to the presence of parasitic capacitance to the ground associated with C_{1-4}, which results in a larger delay. The second stage consists of two cascaded single-stage amplifiers with 80-μm/60-nm transistors, which serve to enhance the DA's gain.

Fig. 6(b) shows the DA S-parameter's simulation and measurement results. An average gain of 18 dB is achieved over the 4–60-GHz frequency range.

Fig. 6(c) shows a 7–8-dB NF in both the simulation and measurement. The measurement is up to 40 GHz due to the equipment limitations.

Fig. 6(d) shows the group delay of the DA. The precision of the measurement above 40 GHz is influenced by the calibration inaccuracies of the vector network analyzer (VNA) employed in the measurement process.

Fig. 6(e) demonstrates a 10-dBm saturated output power at 30 GHz. In comparison to previous studies [46], [47], the supply voltage is reduced to 1 V with the use of common-source transistors.

C. Wideband Passive TX/RX Mixers

Fig. 7 presents an explanation of TX/RX mixers, TX HPF, and the differential LO driver designs, accompanied by simulation results of mixer CG.

The TX mixer is designed as a double-balanced passive mixer with theoretical all-ports isolation. The differential RF signals at the mixer output are combined by a 1.2-dB-loss Marchand balun with a frequency range of 90–180 GHz [48]. The IF port is a differential port that is connected to the output of the DAs. The LO port is a single-ended port that is followed by a balun and a differential LO driver. The differential capacitive-cross-coupled LO driver is designed to reduce the mismatch of differential LO signals [33], providing a saturated LO power of 8 dBm to the gate of the switch transistors. The measured level of leakage from LO to RF is -40 dBm. An HPF with a 3-dB attenuation difference at 102 GHz is positioned after the RF balun. A 40-dB attenuation difference for the image band can be achieved in combination with the PA and PCB transition. The RX mixer is designed as a single-balanced passive mixer. It has the same LO driver as the TX mixer. The differential RF signal is generated by the same balun design as the TX. RF signals are mixed with differential LO signals, which can enhance the CG in comparison to a single-switch mixer [32]. A single-ended IF signal is generated for external equipment. In the RX on-wafer measurement utilizing RF probes, no $LO_{1/4}$ harmonic leakage is observed

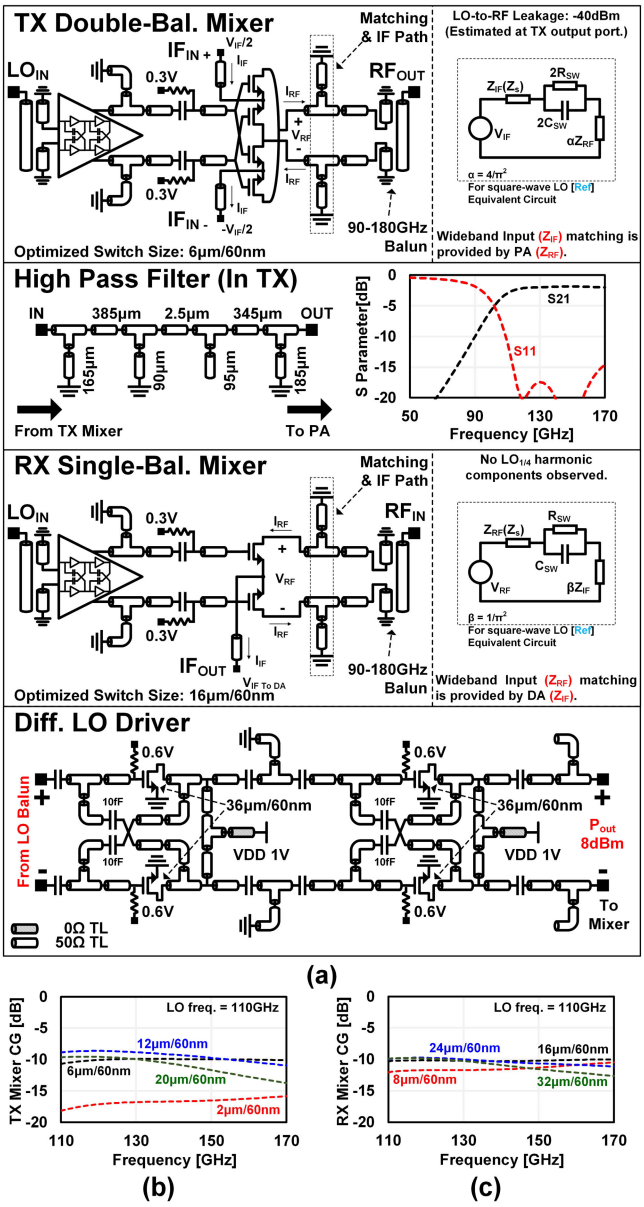


Fig. 7. Proposed mixer designs. (a) TX double-balanced mixer, RX single-balanced mixer, and differential LO driver designs. (b) TX mixer's CG with swept switch size: 2 μm/60 nm, 6 μm/60 nm, 12 μm/60 nm, 20 μm/60 nm, f_{LO} = 110 GHz. (c) RX mixer's CG with swept switch size: 8 μm/60 nm, 16 μm/60 nm, 24 μm/60 nm, 32 μm/60 nm, and f_{LO} = 110 GHz.

at the IF output. The $LO_{1/4}$ harmonic leakage through the pad (PAD), substrate, and power network is significantly attenuated by distributed GND cells and decoupling capacitors connected to the substrate and power network, respectively. To achieve the maximum CG, both the TX mixer and the RX mixer utilize bias voltage close to V_{th} (0.3 V) on the gate.

In the case of passive mixers, the input impedance can be considered to comprise two components. The first component is the impedance of the switch, which is composed of R_{SW} and C_{SW}. R_{SW} represents the channel resistance when the switch is on. C_{SW} represents the switch's equivalent capacitance when the switch is off. Furthermore, the load impedance is converted to the input frequency with a specific factor, which constitutes the second part [49]. The mixer equivalent circuits are illustrated in Fig. 7(a). In such cases, a larger switch size may provide a higher CG at lower frequencies, but this is accomplished by a gain drop at higher frequencies due to a larger C_{SW}. Conversely, a smaller switch size may offer less C_{SW}, but the CG is constrained across the entire band due to a larger R_{SW}.

To achieve optimal CG and gain flatness over the entire D-band frequency range, it is necessary to select an appropriate switch size to ensure good impedance matching and a small C_{SW}. Fig. 7(b) depicts the TX mixer's CG as a function of the swept switch size. The optimal switch size is determined to be 6 μm/60 nm (black dotted line), which enables the attainment of a flat gain characteristic and an average simulated CG of approximately −10 dB over the whole D-band frequency range. Fig. 7(c) shows the CG of the RX mixer with sweeps of the switch size. The optimal switch size is determined to be 16 μm/60 nm (black dotted line), with an average simulated CG of approximately −10 dB across the entire D-band frequency range. Both the TX and RX mixers use 110-GHz LO here. Furthermore, the CG and bandwidth characteristics of the proposed mixers exhibit negligible variation across different process corners.

It is also noteworthy that a pair of TL shunts are positioned at the RF side of both the TX and RX mixers. The TL shunts provide a signal path for lower IF frequencies and also serve impedance-matching functions for the RF side.

D. LO Chain

Fig. 8(a) demonstrates the circuit design for the LO frequency. The entire LO chain comprises an $LO_{1/4}$ frequency quadrupler and an LO amplifier.

The $LO_{1/4}$ frequency quadrupler is comprised of an input amplifier (Amp. 1), a middle-stage amplifier (Amp. 2), and two frequency doublers. The input amplifier provides input matching from 25 to 30 GHz. The middle-stage amplifier is responsible for amplifying signals in the frequency range of 50–60 GHz. Amp. 2 utilizes a single amplifier to reduce power consumption and reduce layout area. Moreover, the signal power level at 50–60 GHz remains sufficiently high to justify the inclusion of a single amplifier. The frequency doublers utilize common-source transistors with a low bias voltage in proximity to V_{th} (0.3 V) to enhance the second harmonic component [19]. The LO amplifier comprises three stages using a similar gain-boosting architecture as PA units to drive the LO signal to the saturated level. To reduce the unwanted harmonic components, a 90° open-TL shunt at $LO_{3/4}$ is placed, which serves as a ground short for the $LO_{3/4}$ signals. Furthermore, the narrowband characteristics of the final LO amplifier can be used to constrain other harmonics.

Fig. 8(b) shows the simulated input matching of the $LO_{1/4}$ frequency quadrupler. $S11$ is less than the −10 dB from 25 to 30 GHz. Fig. 8(c) depicts the output power of the $LO_{1/4}$, $LO_{2/4}$, $LO_{3/4}$, and LO signals versus the input power of the external $LO_{1/4}$ signal, with the $LO_{1/4}$ frequency set to 27.5 GHz. The simulation result shows a 35-dB constraint on the maximum unwanted harmonic component in comparison

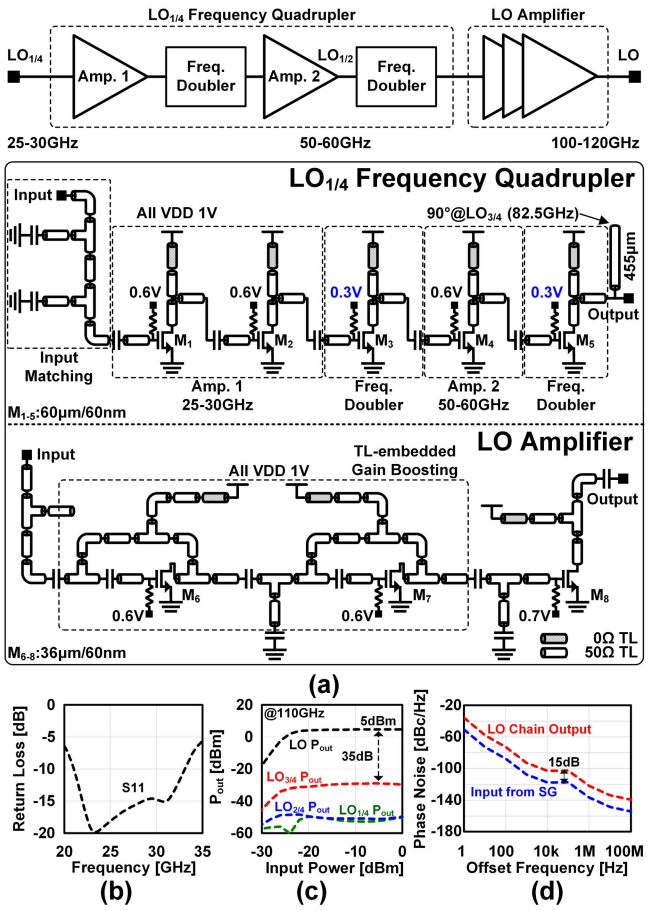


Fig. 8. Proposed LO chain design. (a) $LO_{1/4}$ frequency quadrupler and LO amplifier designs. (b) Input matching of the LO chain. (c) $LO_{1/4}$, $LO_{2/4}$, $LO_{3/4}$, and LO output power versus the input power when $f_{LO} = 110$ GHz. (d) Simulated SSB phase noise of the LO chain, incorporating the differential LO driver discussed in Section III-C.

to the LO signal. This could be further reduced by the LO driver discussed in the mixer section.

It can be observed that the entire LO chain contributes to the phase noise on the LO signal. The results of the simulation are presented in Fig. 8(d), which demonstrates an approximate 15-dB increase, resulting in an integrated phase noise of −34.7 dBc from 1 kHz to 25 GHz with extrapolations.

IV. PCB Interface Design

A well-designed PCB is a crucial component of the proposed wireless communication system, as it serves as the interface for the IF, LO, and RF signals. In general, a PCB with low loss and a wideband frequency response is preferable.

This section presents a series of PCB designs. The images of the TRX modules and comprehensive flip-chip components are provided, accompanied by a detailed explanation of the PCB transition from the CMOS chip to the standard rectangular waveguide. Additionally, the PCB design of the connector part for IF and LO signals is also demonstrated.

A. TX/RX Modules and Flip-Chip Implementation

Fig. 9 illustrates the TRX modules' photographs and implementations of the TRX chipset.

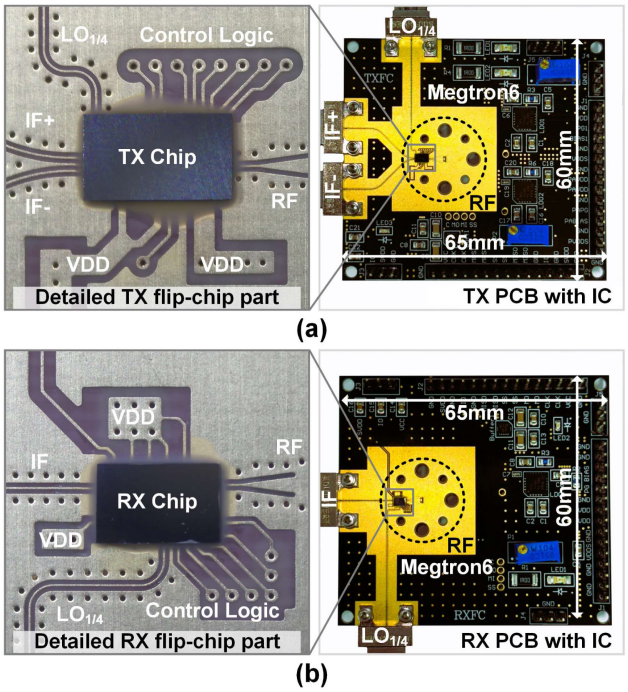


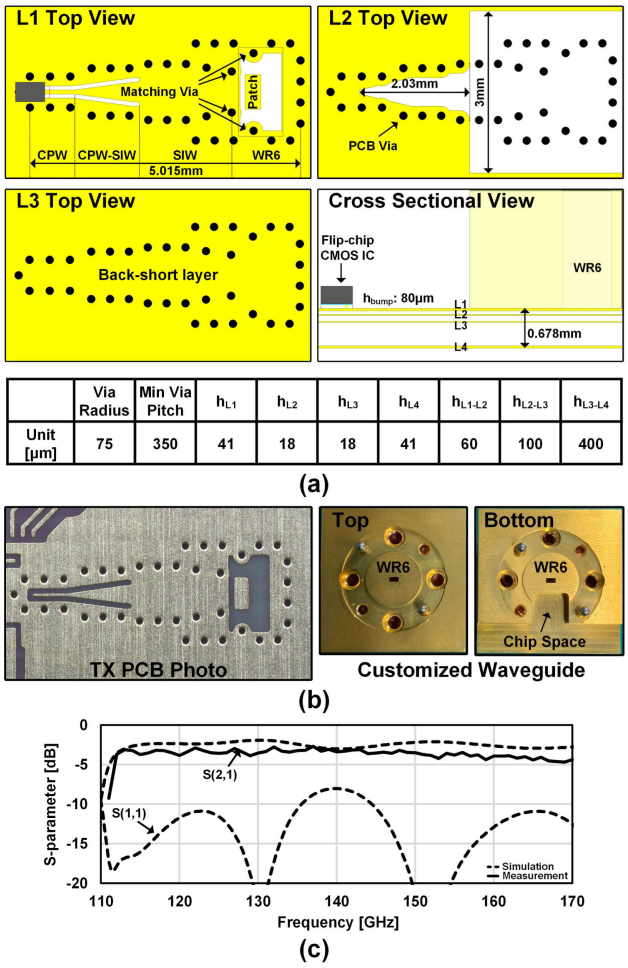
Fig. 9. Photographs of TRX modules. (a) TX module and top-viewed flip-chip implementation. (b) RX module and top-viewed flip-chip implementation.

Fig. 9(a) illustrates the specifics of the TX module. The TX module features an $LO_{1/4}$ signal interface, a differential IF signal interface, and an RF signal interface. Fig. 9(b) illustrates the details of the RX module. Similarly, the RX module is equipped with an $LO_{1/4}$ signal interface, a single-ended IF signal interface, and an RF interface. The $LO_{1/4}$ and IF signal interfaces are based on the Southwest 1892-04A-6 Connectors, which are capable of withstanding frequencies up to 67 GHz. The RF signal interface is a standard waveguide flange (UG-387) to connect with the WR6 (110–170 GHz) waveguide.

The TX and RX PCB modules are fabricated using a material designated as Megtron6, with a PCB size of 60 × 65 mm. The CMOS chip is implemented on the PCB by the flip-chip technique, with the use of bumps.

B. RF PCB Transition From CMOS Chip to Waveguide

Fig. 10(a) shows PCB information and the proposed RF PCB transition design from the CMOS chip to the WR6 waveguide. The PCB comprises four layers, while the transition is made with the upper three layers, L1, L2, and L3. L1 is the layer that is connected to the CMOS chip and the waveguide, and L3 is the layer that serves as a back-short layer. The height from L1 to L3 is approximately $\lambda/4$ at 140 GHz, which can enhance the power delivery to the waveguide [50], [51]. The entire PCB transition consists of four distinct parts: the coplanar waveguide (CPW), the CPW-to-substrate-integrated-waveguide (SIW) part, the SIW, and the SIW-to-WR6 part. The CMOS chip is connected to the PCB CPW through the use of gold bumps. Furthermore, the height of the bumps is optimized at 80 μm to reduce



	Via Radius	Min Via Pitch	h_{L1}	h_{L2}	h_{L3}	h_{L4}	$h_{L1\text{-}L2}$	$h_{L2\text{-}L3}$	$h_{L3\text{-}L4}$
Unit [μm]	75	350	41	18	18	41	60	100	400

Fig. 10. PCB transition from the CMOS chip to the WR6 waveguide. (a) Transition design and PCB information. (b) Photographs of the proposed transition and customized waveguide. (c) Measured and simulated transition insertion loss over the entire D-band frequency range.

the parasitic capacitance from the signal to the ground. The CPW-to-SIW section comprises a tapered connection, which enables the attainment of a wideband characteristic. The SIW is designed to transmit D-band signals. As for the SIW-to-WR6 transition, a patch on the L1 layer and matching vias with a 75-μm diameter facilitate an optimized wideband frequency response [50], [51].

Fig. 10(b) illustrates the actual photographs of the PCB transition and the customized waveguide. The top surface of the customized waveguide is utilized for antenna connections, while the bottom side includes an empty aperture for the CMOS chips. Fig. 10(c) demonstrates the simulated *S*-parameters and de-embedded measured insertion loss of the proposed PCB transition. The simulation shows a 3-dB loss and a less than −10-dB average return loss. The measurement result demonstrates a 3–4-dB loss at the frequency range of 112–170 GHz, which provides a wideband RF signal path for the TRX modules.

To provide further evaluation of the performance of the proposed PCB transition design, three different back-to-back PCBs are fabricated and subsequently measured, as illustrated in Fig. 11(a). The first

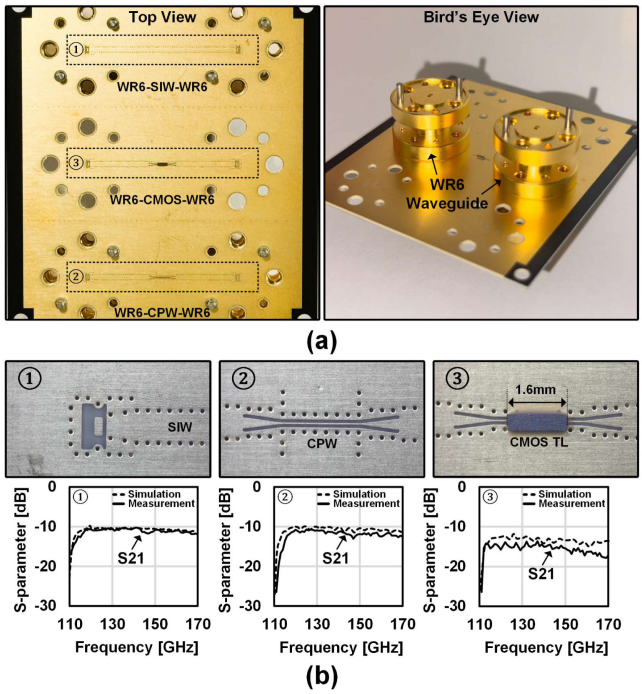


Fig. 11. Back-to-back PCB transition. (a) Top and bird's eye view of the back-to-back PCB transition design including WR6–SIW–WR6, WR6–CMOS–WR6, and WR6–SPW–WR6. (b) Detailed photographs and measured insertion loss.

back-to-back configuration is a back-to-back WR6–SIW–WR6 structure. Two SIW-to-WR6 transitions are connected through an SIW, and the loss of the SIW-to-WR6 is evaluated. The second back-to-back architecture incorporates a CPW at the center, in addition to the first one, and comprises two CPW-to-SIW transitions, which can be utilized to assess CPW loss. The third back-to-back architecture includes an additional 1.6-mm CMOS TL, based on the second one, to evaluate the loss of the bump connection.

Fig. 11(b) illustrates the detailed photographs of the three back-to-back architectures, along with their simulated and measured insertion loss. It can be observed that the SIW-to-WR6 has a good corresponding result between simulation and measurement. However, the back-to-back architectures, which include CPW and CMOS TL, demonstrate a notable loss increase between simulations and measurement. The observed degradation may be caused by the fabrication mismatch, surface roughness [52], and the potential for inaccurate material parameters at D-band frequency. These measurement results are used to derive the de-embedded PCB transition loss mentioned in Fig. 10(c).

C. Connector Part for IF and LO Signals

Fig. 12(a) shows the PCB design of the connector part for the IF and LO signals. The connector part utilizes the identical PCB configuration as that utilized for the RF transition. The Southwest 1892-04A-6 Connector's signal pin is connected to the PCB CPW on the L1 layer with a 90–150–90-μm CPW TL. And L3 serves as the CPW's bottom ground. The CPW on

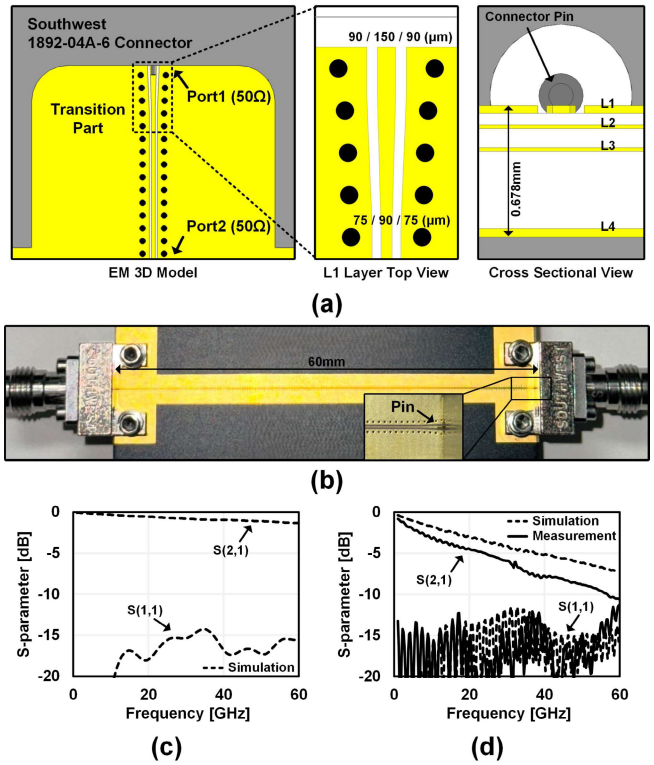


Fig. 12. PCB connections with the Southwest 1892-04A-6 Connector. (a) PCB design of the connector part. (b) 60-mm PCB TL with back-to-back connectors. (c) Simulated insertion loss of the PCB connection with the connector. (d) *S*-parameters of the back-to-back PCB TL of (b).

the PCB has a configuration of 75–90–75 μm, which results in a 50-Ω characteristic impedance.

Fig. 12(b) shows a photograph of a 60-mm PCB CPW TL with back-to-back connectors, which is utilized for the assessment of the losses associated with the connector part and the PCB TLs.

Fig. 12(c) shows simulated *S*-parameters of the connector part. A wideband input impedance matching ($S11 < -10$ dB) is achieved from dc to 60 GHz in the simulation.

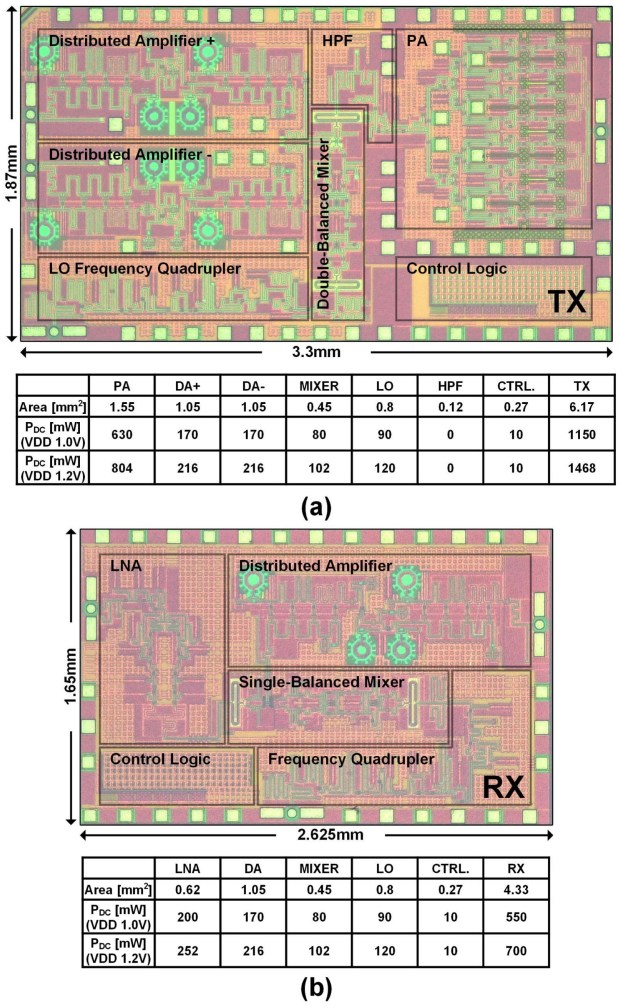
Fig. 12(d) shows the measured and simulated *S*-parameters of the back-to-back PCB CPW TL referenced in Fig. 12(b). The measurement results demonstrate that the design realizes a wideband input impedance matching up to 60 GHz, which is in accordance with the simulation results. However, the measurement also depicts an increased attenuation factor compared to the simulation, which may also be attributed to the surface roughness issue, similar to those observed in RF transition designs [52].

V. Measurement Result

This section presents the measurement results of the proposed TRX chipset including TX/RX performance, short-range OTA SISO, long-range OTA SISO, and short-range OTA LOS-MIMO scenarios.

A. TX/RX Modules Performance Measurement

Fig. 13 shows the chip micrographs with a breakdown of block area and power consumption. The proposed TRX chipset



	PA	DA+	DA-	MIXER	LO	HPF	CTRL.	TX
Area [mm^2]	1.55	1.05	1.05	0.45	0.8	0.12	0.27	6.17
P_{DC} [mW] (VDD 1.0V)	630	170	170	80	90	0	10	1150
P_{DC} [mW] (VDD 1.2V)	804	216	216	102	120	0	10	1468

	LNA	DA	MIXER	LO	CTRL.	RX
Area [mm^2]	0.62	1.05	0.45	0.8	0.27	4.33
P_{DC} [mW] (VDD 1.0V)	200	170	80	90	10	550
P_{DC} [mW] (VDD 1.2V)	252	216	102	120	10	700

Fig. 13. TRX chipset. (a) TX micrograph and power consumption. (b) RX micrograph and power consumption.

is fabricated in a 65-nm CMOS process. The TX chip size is 1.87 × 3.3 mm and the RX chip size is 1.65 × 2.625 mm. The TX and RX chips consume 1150 and 550 mW with a 1-V power supply and 1468 and 700 mW with a 1.2-V power supply, respectively. In the TX chip, two DAs for the differential IF signals may suffer from the mismatch issue due to their relevant far distance, which can lead to some decrease in CG, accompanied by gain ripples. The discrepancy between the two paths of the differential signals will ultimately result in the summation of a common-mode signal and a differential signal. The common-mode signal will be suppressed by the double-balanced mixer and the RF balun at its output port.

The TX and RX chips are measured individually after being implemented on the PCB. Fig. 14(a) and (b) shows the measurement setup. An external D-band mixer with a bandwidth of 60 GHz for both IF and RF signals is used here to realize frequency up- and downconversion. A Keysight E8257D signal generator (SG) with an external frequency tripler is utilized to provide 110-GHz LO for the external mixer. Another SG provides the $LO_{1/4}$ (27.5 GHz) for the TRX. A Keysight M8194A arbitrary waveform generator (AWG) is used to provide IF signals. A Keysight UXR1104A oscilloscope is

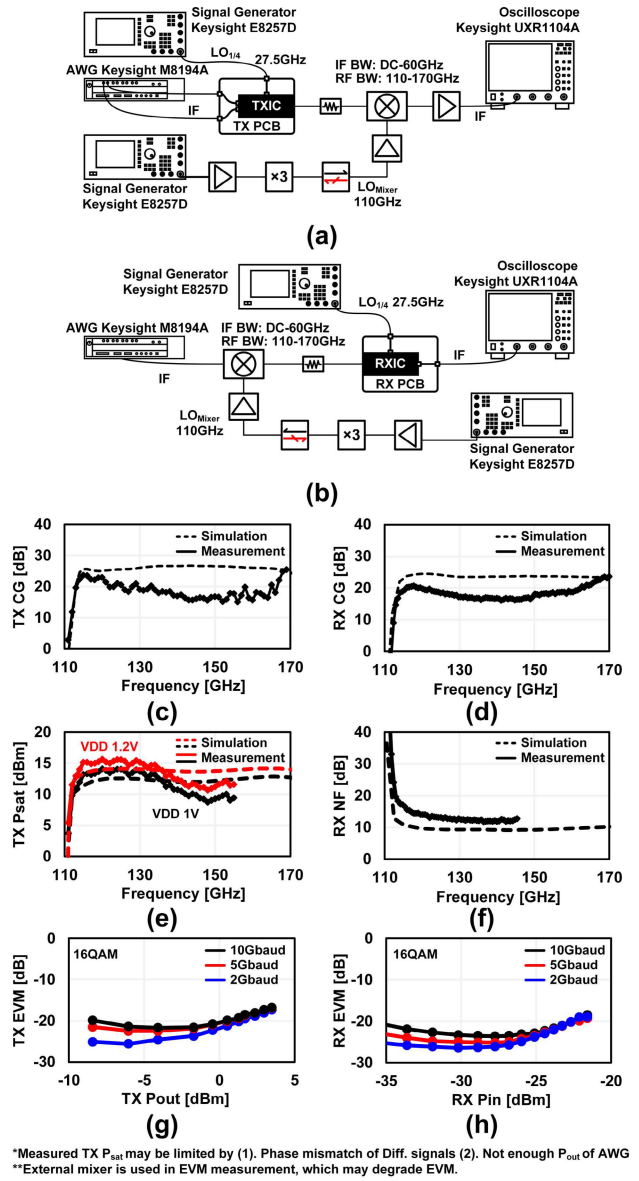


Fig. 14. TRX measurements. (a) TX module measurement setup. (b) RX module measurement setup. (c) TX CG versus RF frequency. (d) RX CG versus RF frequency. (e) TX saturated output power versus RF frequency with 1/1.2 V PA's drain supply voltage (VDD). (f) RX NF versus RF frequency. (g) Measured TX EVM versus TX output power. (h) Measured RX EVM versus RX input power.

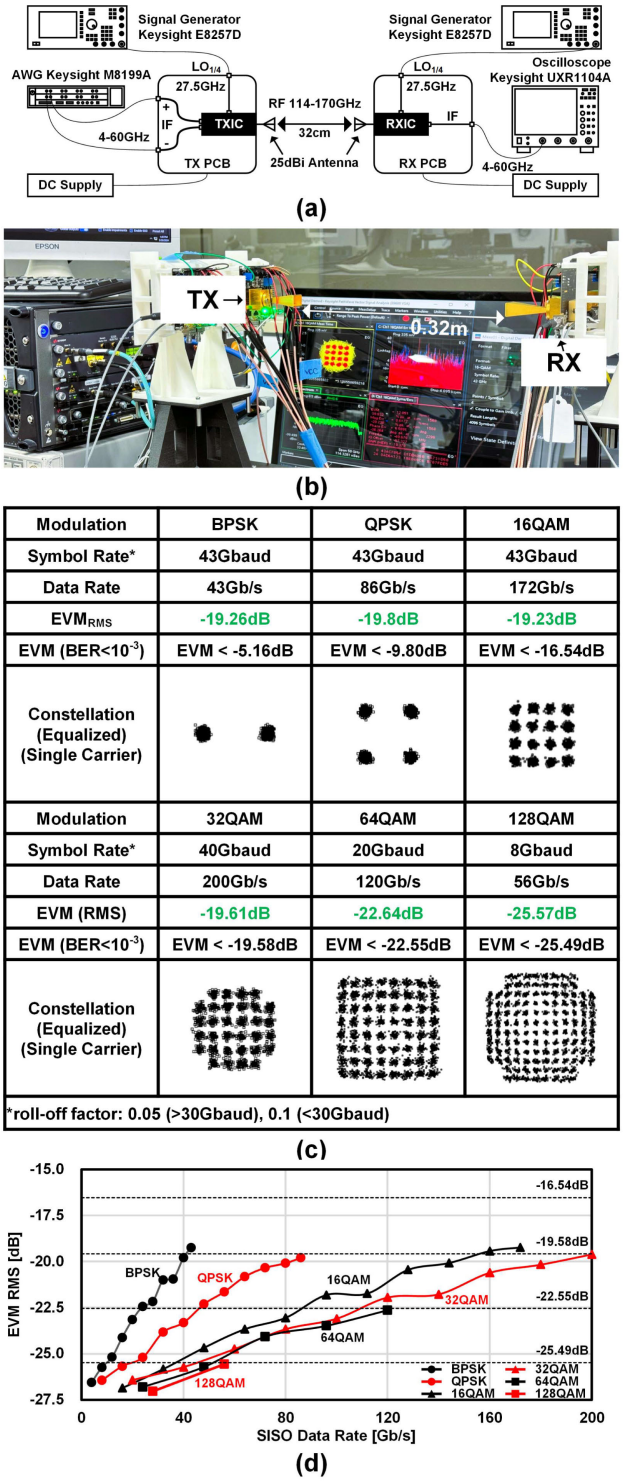
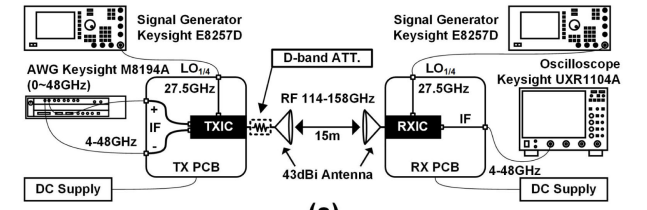


Fig. 15. Short-range SISO measurement at 0.32 m. (a) Short-range SISO measurement setup with 25-dBi horn antennas. (b) Measurement photograph. (c) Measured EVM and constellations. (d) Measured EVM_{rms} versus the SISO data rate.

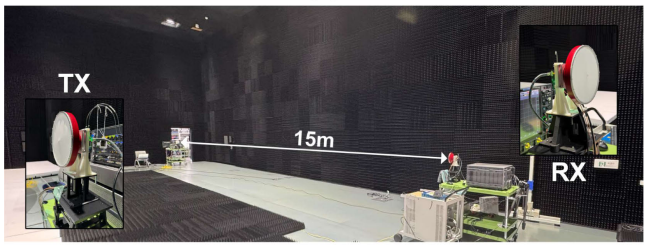
used to demodulate IF signals. Fig. 14(c)–(f) illustrates the TX CG, RX CG, TX P_{sat}, and RX SSB NF, respectively. All results are presented after de-embedding. In the measurement of saturated output power from the TX, the TX chip achieves a 12–15-dBm P_{sat} with a 1.2-V power supply. The results may be limited by the phase mismatch between the differential signals and insufficient output power from the AWG at higher frequencies.

In the CG measurement, both TX and RX chips achieve an 18–20-dB gain from 114 to 170 GHz. The average NF of the RX chip is 12 dB. The discrepancies in TX/RX CG and RX NF gain between the simulation and measurement results are primarily due to the inherent limitations in the accuracy of the passive circuit blocks, the transistor models employed for PA units, and the parasitic extraction (PEX) simulation for mixers as well as higher junction temperatures.

Fig. 14(g) and (h) shows the measured EVM results of the TX and RX with 2, 5, and 10 Gbaud 16QAM signals. These results are constrained by the linearity of the external mixer.



(a)

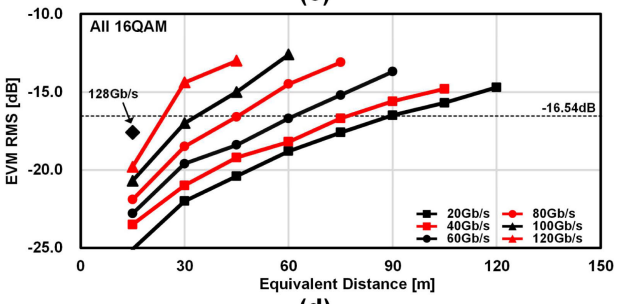


(b)

Modulation	16QAM	16QAM	32QAM	64QAM
Symbol Rate	5Gbaud	32Gbaud	30Gbaud	15Gbaud
Data Rate	20Gb/s	128Gb/s	150Gb/s	90Gb/s
Distance*	90m	15m	15m	15m
EVM (RMS)	-16.6dB	-17.6dB	-19.89dB	-22.62dB
EVM (BER<10^{-3})	EVM < -16.54dB	EVM < -16.54dB	EVM < -19.58dB	EVM < -22.55dB
Constellation (Equalized)				

* Equivalent Distance with Attenuator

(c)



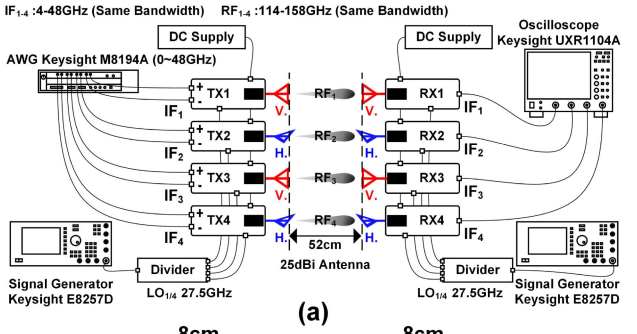
(d)

Fig. 16. Long-range SISO measurement at 15 m. (a) Long-range SISO measurement setup with 43-dBi antennas and a D-band attenuator. (b) Measurement photograph. (c) Measured EVM and constellations. (d) Measured EVM_{rms} versus the equivalent distance.

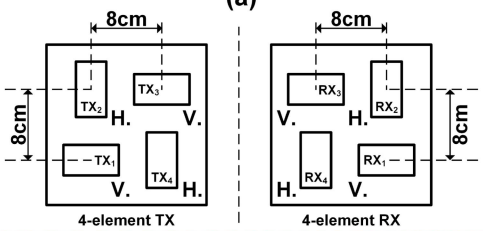
To maximize the TX output power, all OTA measurements discussed in the following utilize a 1.2-V power supply for the PA, whereas the other blocks utilize a 1-V supply.

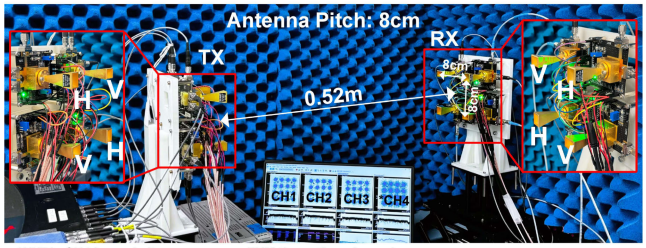
B. Short-Range OTA SISO Measurement

Fig. 15(a) demonstrates the OTA measurement configuration for the short-range SISO scenario. Fig. 15(b) shows the OTA setup's photograph. In this measurement, an AWG (Keysight M8199A) is employed to generate modulated signals up to 60 GHz, and an oscilloscope (Keysight UXR1104A) is utilized to evaluate the constellation and EVM. Two identical SGs (Keysight E8257D) provide external $LO_{1/4}$ (27.5 GHz) signals. The measurement is conducted at a distance of 0.32 m, utilizing the same 25-dBi horn antennas for both the TX and RX modules. The antennas are connected to the proposed



(a)





*UXR's CH4 is weak. It causes worse EVM than other channels.

Channel	CH1	CH2	CH3	CH4
Power Level*	0dB	-49.0dB	-24.8dB	-46.4dB

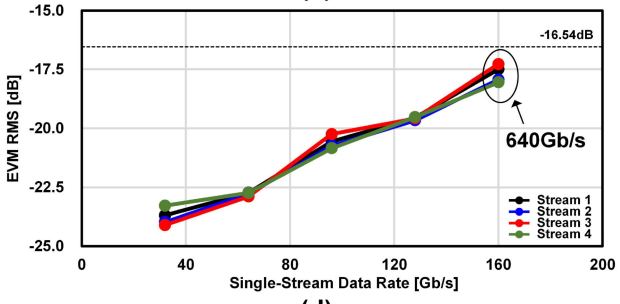
*Normalized signal power level when channel 1 is turned on.

(b)

Modulation	16QAM			
Stream*	Stream1 (V)	Stream2 (H)	Stream3 (V)	Stream4 (H)
Bandwidth	40GHz	40GHz	40GHz	40GHz
Data Rate	160Gb/s	160Gb/s	160Gb/s	160Gb/s
EVM (RMS)	-17.50dB	-17.94dB	-17.28dB	-18.05dB
EVM (BER<10^{-3})	EVM < -16.54dB	EVM < -16.54dB	EVM < -16.54dB	EVM < -16.54dB
Constellation (Equalized)				

* OFDM signal with 1024 carriers.

(c)



(d)

Fig. 17. Short-range LOS-MIMO measurement at 0.52 m. (a) Short-range 4 × 4 LOS-MIMO measurement setup with 25-dBi antennas. (b) Antenna arrangement and measurement photograph. (c) Measured EVM and constellations. (d) Measured EVM_{rms} versus the data rate of each stream.

RF PCB transition through the standard waveguide flange (UG-387). The maximum data rates, as measured, are 43 Gb/s

TABLE II
PERFORMANCE COMPARISON

	ISSCC 2018 [23]	JSSC 2019 [21]	TMTT 2020 [25]	IMS 2020 [53]	JSSC 2020 [24]	JSSC 2023 [27]	ISSCC 2024 [20]	JSSC 2024 [29]	This work			
Technology	65nm CMOS	40nm CMOS	130nm SiGe	130nm SiGe	80nm InP-HEMT	130nm SiGe	28nm CMOS	65nm CMOS	65nm CMOS			
RF Freq. [GHz]	70 - 105	252 - 279	225 - 255	222.5 - 257.5	275 - 305	110 - 170	90 - 180	88 - 136	114 - 170			
TRX Integration	TRX	TRX	TX & RX	TX & RX	Integrated PA	TRX	TX & RX	TRX	TX & RX			
Modulation*	16QAM	16QAM	QPSK	QPSK / 16QAM	16QAM	BPSK / QPSK 16QAM / 32QAM	OOK	16QAM	16QAM	32QAM	64QAM	128QAM
SISO TX-to-RX Data Rate** [Gb/s]	120	80	55	60 / N/A[#]	120	60 / 120 120 / N/A[##]	16 / 20	112	172	200	120	56
SISO EVM_{RMS} [dB]	-17	-18.42	-9.94	-14.52 / -14.61	-16.7	-11.15 / -9.9 -17.2 / -17.6	N/A	-16.6	-19.23	-19.61	-22.64	-25.57
MIMO TX-to-RX Data Rate** [Gb/s]	N/A	N/A	110	N/A	N/A	N/A	N/A	N/A	640	N/A	N/A	N/A
MIMO EVM_{RMS} [dB]	N/A	N/A	-9.94	N/A	N/A	N/A	N/A	N/A	-17.69	N/A	N/A	N/A
TX P_{sat} [dBm]	-1.9	-1.6	7.5	12	11	-8	15-18	0	12 - 15			
RX SSB NF [dB]	N/A	22.9	17	18.5	10 - 17[+]	10.08[▲]	6.2 - 8.5[▲]	15	12			
TX/RX P_{DC} [mW]	120/160	890/897	2850 (TRX)	1237 / 850	4500 / 4500	2500 / 1950	750 / 160[○]	200 / 120	1150 / 550 (1V) 1468 / 700 (1.2V)			
Antenna Gain [dBi]	23	24	25	21	50	4.8	15	15	25		43	
Communication Distance [m]	0.2	0.03	1 / 2	0.8	9.8	0.15	1 / 0.5	0.02	0.32 / 0.52		15 / 90	
RF Interface	Flip-Chip Implementation	Probing	On-Chip Antenna (Lens)	On-Chip Antenna (Lens)	Individual module	On-Chip Antenna (Lens)	Wire Bonding	Flip-Chip Implementation	Wideband Flip-Chip Implementation & PCB-to-Waveguide Transition			
TX/RX Area [mm^2]	6 (TRX)	11.06 (TRX)	4.02/3.36	7 / 5.1	N/A	27.2 (TRX)	0.69 / 0.77[○]	5.7 (TRX)	6.17 / 4.33			

*This work can also support BPSK & QPSK.
**Data rate for BER < 10^{-3}.
[#]Data rate of 100Gb/s is also reported with BER > 10^{-3}.
[##]Data rate of 200Gb/s is also reported with BER > 10^{-3}.
[+]NF of the RF PA.
[▲]Simulation result.
[○]On-chip PLL

in BPSK, 86 Gb/s in QPSK, 172 Gb/s in 16QAM, 200 Gb/s in 32QAM, 120 Gb/s in 64QAM, and 56 Gb/s in 128QAM.

Fig. 15(c) presents a summary of the measured constellations and EVM for BPSK, QPSK, 16QAM, 32QAM, 64QAM, and 128QAM cases. Modulated signals with a single carrier are used here with a roll-off factor of 0.05 (>30 Gbaud) and 0.1 (<30 Gbaud). The measured EVM_{rms} values are −19.26 dB (10.89%, BPSK at 43 Gb/s), −19.8 dB (10.23%, QPSK at 86 Gb/s), −19.23 dB (10.93%, 16QAM at 172 Gb/s), −19.61 dB (10.46%, 32QAM at 200 Gb/s), −22.64 dB (7.38%, 64QAM at 120 Gb/s), and −25.57 dB (5.27%, 128QAM at 56 Gb/s), which all satisfy the 10^{-3} BER criteria discussed in Table I.

Fig. 15(d) depicts the relationship between measured EVM_{rms} values and SISO data rates of various kinds of modulations. The required EVM_{rms} values for 16QAM, 32QAM, 64QAM, and 128QAM are also shown as the black dot lines. The maximum SISO data rate is achieved by 40-Gbaud 32QAM, which is 200 Gb/s.

C. Long-Range OTA SISO Measurement

To further evaluate the TRX modules' performance with extended communication distances, a long-range OTA SISO measurement is also conducted here.

Fig. 16(a) demonstrates the setup for the long-range OTA SISO measurement. Fig. 16(b) shows the measurement photograph. The measurement is conducted inside an anechoic chamber room. Similar to the short-range OTA SISO measurement setup, an AWG (Keysight M8194A) is utilized to generate single carrier modulated signals up to 48 GHz, and the same oscilloscope (UXR1104A) is utilized for signal evaluation. External $LO_{1/4}$ (27.5 GHz) signals are generated from two SGs (Keysight E8257D). The distance is fixed at 15 m, with two 43-dBi Cassegrain antennas. An additional D-band attenuator is positioned at the TX side to evaluate the equivalent communication distance. The maximum data rates, as measured, are 128 Gb/s in 16QAM at 15 m, 150 Gb/s in 32QAM at 15 m, and 90 Gb/s in 64QAM at 15 m. The maximum equivalent distance for 20-Gb/s 16QAM is 90 m.

Fig. 16(c) summarizes EVM values and constellations for 16QAM, 32QAM, and 64QAM cases. The measured EVM_{rms} values are −16.6 dB (14.79%, 20-Gb/s 16QAM at 90 m), −17.6 dB (13.18%, 128-Gb/s 16QAM at 15 m), −19.89 dB (10.13%, 150-Gb/s 32QAM at 15 m), and −22.62 dB (7.4%, 90-Gb/s 64QAM at 15 m), which all satisfy the 10^{-3} BER criteria.

Fig. 16(d) shows the measured various data rates of 16QAM signals' EVM_{rms} values versus the equivalent communication distance which is tuned by the embedded D-band attenuator at the TX side.

D. Short-Range OTA LOS-MIMO Measurement

Fig. 17(a) shows the setup of the short-range 4 × 4 LOS-MIMO measurement. Four TRX modules with H–V-polarized 25-dBi antennas form a 4 × 4 LOS MIMO architecture. The AWG (Keysight M8194A) is used here to generate OFDM MIMO signals up to 48 GHz. And the oscilloscope (Keysight UXR1104A) is utilized for MIMO signal decomposition. Both IF_{1-4} and RF_{1-4} signals occupy 44-GHz bandwidth

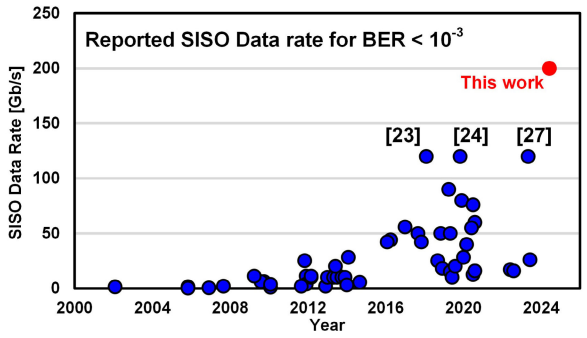


Fig. 18. Reported SISO data rate with BER $< 10^{-3}$ as of June 2024.

in the frequency band of 4–48 GHz and 114–158 GHz, respectively. Two SGs (Keysight E8257D) deliver external $LO_{1/4}$ (27.5 GHz) signals to the TRX modules with two power dividers. The communication distance is 0.52 m.

Fig. 17(b) shows the antenna arrangement, the measurement photograph, and received power levels of channel 1 (CH1), channel 2 (CH2), channel 3 (CH3), and channel 4 (CH4) when the signal in CH1 is turned on. The antenna pitch is 8 cm. This value represents the minimum that can be achieved given the limitations of the PCB size. Antenna spacing can affect the data rate in the measurement. As discussed previously, a larger spacing makes the MIMO system perform as a combination of four SISO systems. Conversely, small spacing increases the signal power level on the receiving side. This increased power level may result in a more nonlinear system and degradation in EVM, which also limits the data rate.

The measured maximum data rate per stream is 160 Gb/s by the 16QAM OFDM signals. The measured EVM_{rms} values are −17.5 dB (13.34%), −17.94 dB (12.68%), −17.28 dB (13.68%), and −18.05 dB (12.52%) for stream 1 (V-Pol.), stream 2 (H-Pol.), stream 3 (V-Pol.), and stream 4 (H-Pol.), respectively, which satisfies the 10^{-3} BER requirement. The total data rate is 640 Gb/s. The utilization of 16QAM rather than the targeted 32QAM is to achieve the maximum available data rate, considering the constraints imposed by the EVM. Fig. 17(c) shows the summary of the EVM_{rms} values and constellation. Fig. 17(d) shows the relationship of EVM_{rms} values versus the data rate of streams 1–4. It can be observed that there are still some EVM margins from the requirement of the 16QAM signals, which implies the potential of the proposed TRX chipset to achieve a higher data rate with wider bandwidth modulated signals.

VI. Conclusion

This work presents a D-band TRX chipset using a 65-nm CMOS process. The TRX chipset is capable of supporting a signal-chain bandwidth of up to 56 GHz. The wideband and improved linearity designs permit the support of high-order wideband QAM signals up to 200 Gb/s in the OTA measurement. A 4 × 4 LOS-MIMO configuration is also conducted to further increase the total wireless throughput. Fig. 18 illustrates a comparison between this work and other reported SISO data rates with BER $< 10^{-3}$ in the past 20 years. Table II demonstrates a comparison of the proposed TRX chipset with other reported state-of-the-art wireless TRXs. It shows the highest 200 Gb/s OTA SISO TX-to-RX data rate and the highest 640 Gb/s OTA MIMO TX-to-RX data rate as of June 2024, which provides a potential solution for the next generation of wireless communications.

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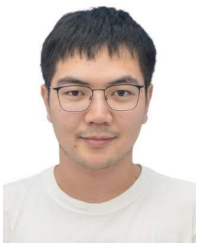

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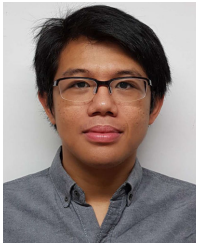

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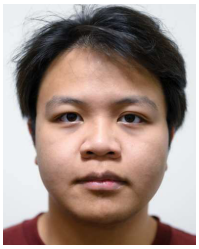

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