A DPD/Dither-Free DPLL Based on a Cascaded Fractional Divider and Pseudo-Differential DTCs Achieving a −62.1-dBc Fractional Spur

Dingxin Xu, *Member, IEEE*, Zezheng Liu, *Graduate Student Member, IEEE*, Yifeng Kuai, *Graduate Student Member, IEEE*, Hongye Huang, *Member, IEEE*, Yuncheng Zhang, *Member, IEEE*, Zheng Sun, *Member, IEEE*, Bangan Liu, *Member, IEEE*, Wenqian Wang, *Graduate Student Member, IEEE*, Yuang Xiong, *Graduate Student Member, IEEE*, Junjun Qiu, *Member, IEEE*, Waleed Madany, *Graduate Student Member, IEEE*, Yi Zhang, *Member, IEEE*, Ashbir Aviat Fadila, *Graduate Student Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Fellow, IEEE*

***Abstract*— This article presents a 7-GHz fractional-*N* digital phase-locked loop (DPLL) without any digital pre-distortion (DPD) on the integral nonlinearity (INL) of the digital-to-time converter (DTC) or dither. Utilizing a cascaded fractional divider, the fractional spur offset frequency can be shifted beyond the PLL bandwidth, resulting in less fractional spur degradation at near-integer channels. A pseudo-differential DTC (PD-DTC) technique that can cancel the even-symmetric nonlinearity components is also employed to achieve a better suppression of the fractional spur. Thanks to the aforementioned two techniques, a −62.1-dBc worst-case fractional spur can be achieved without degrading the in-band PLL phase noise (PN) or PLL locking time. Occupying 0.23-mm^2 area in a 65-nm CMOS process, this PLL can achieve a 143.7-fs integrated jitter with a 100-MHz reference frequency and 8.89-mW power consumption, which translates to a figure-of-merit (FoM) of −247.4 dB.**

***Index Terms*— Digital-to-time converter (DTC), fractional spur, fractional-*N*, frequency synthesizer, jitter, phase-locked loop (PLL).**

I. Introduction

MODERN wireless communication systems and frequency-modulated continuous-wave (FMCW) radar systems require extremely low integrated jitter and spur levels from the local oscillators. Because of the Process scalability and compatibility with phase or frequency modulations, digital phase-locked loop (DPLL) is a strong candidate in these applications [1], [2], [3], [4], [5]. Recent fractional-*N* DPLLs usually employ a digital-to-time converter (DTC) to cancel out the accumulated quantization noise (QN) from the delta-sigma modulator (DSM), which is used to control the divide ratio of the multi-modulus divider (MMD). Fig. 1 illustrates the operation of this kind of DTC-based fractional-*N* DPLL. The delay of the DTC (τ_{dtc}) in each reference cycle is controlled to match the corresponding accumulated QN ($\varepsilon_{\mathrm{qn}}$). The code-to-delay gain of the DTC (K_{dtc}) is usually calibrated by a least-mean-square (LMS) algorithm, such that $\varepsilon_{\mathrm{qn}}$ can be perfectly canceled [6]. However, the code-to-delay conversion of the DTC is not linear. The integral nonlinearity (INL) error of the DTC (τ_{inl}) will generate a periodical pattern at the output of the phase detector (PD), which will periodically modulate the frequency of the digitally controlled oscillator (DCO) and cause fractional spurs. The offset frequencies of those fractional spurs are usually located at αf_{ref} and the corresponding harmonics, where α is the fractional part of the frequency control word (FCW) and f_{ref} is the reference frequency. When α is close to 0 or 1, the fractional spurs fall in the PLL bandwidth and thus cannot be filtered by the PLL.

A large amount of effort has been devoted to mitigating the fractional spur problem in fractional-*N* PLLs. As shown in Fig. 2, those PLL techniques can be roughly classified into two types. The first type is to achieve a low fractional spur level by applying a digital pre-distortion (DPD) to the INL of the DTC [7], [8], [9]. In this case, a lookup table (LUT) is employed in the PLL to learn the shape of the DTC INL curve. The DPD scheme should be selected carefully based on the DTC characteristics for an effective INL cancellation. For example, Levantino et al. [7] implemented a first-order interpolation DPD because the employed variable slope DTC (VS-DTC) exhibited a continuous INL profile. On the other hand, Liu et al. [8] used a zero-order interpolation DPD to compensate for the mismatch-dominated INL of a path-selection DTC. Although an excellent fractional spur performance can be achieved by DPD-based techniques, the LUTs usually take hundreds of microseconds [7], [9] to one millisecond [8] time to update, hindering their applications in scenarios where the PLL locking time specification is tight.

Received 22 April 2024; revised 19 July 2024 and 8 September 2024; accepted 1 October 2024. This work was supported in part by the National Institute of Information and Communications Technology (NICT) under Grant JPJ012368C00801; in part by the Japan Science and Technology Agency (JST) under Grant JPMJFS2122; in part by the Support for Tokyo Tech Advanced Researchers (STAR); and in part by the VLSI Design and Education Center (VDEC) in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., and Keysight Technologies Japan, Ltd. *(Corresponding author: Dingxin Xu.)*

The authors are with the Department of Electrical and Electronic Engineering, Institute of Science Tokyo, Tokyo 152-8550, Japan (e-mail: xud@ssc.pe.titech.ac.jp).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3477498.

Digital Object Identifier 10.1109/JSSC.2024.3477498

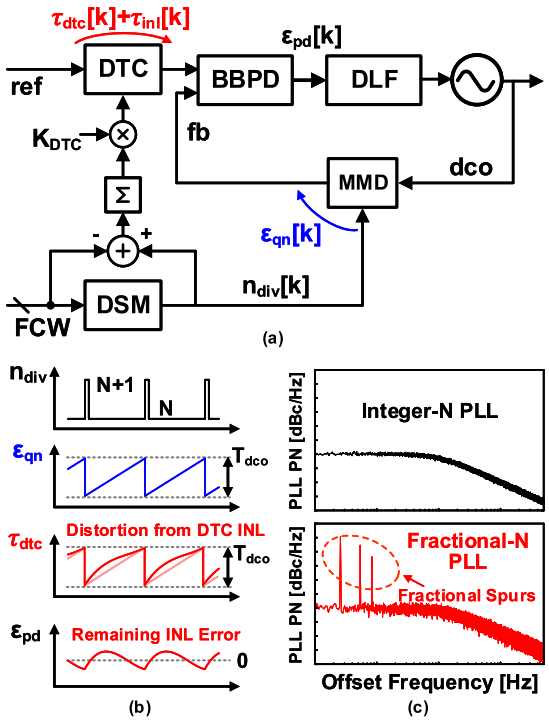


Fig. 1. (a) Schematic, (b) operation, and (c) output spectra of a DTC-based fractional-N DPLL.

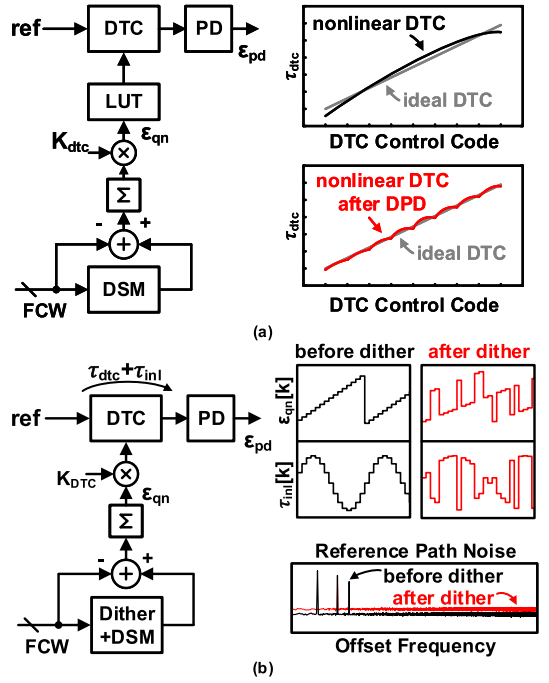


Fig. 2. Conventional DPD-based (a) and dither-based (b) fractional spur mitigation techniques.

Another commonly used technique to suppress the fractional spur is dithering [10], [11], [12]. As shown in Fig. 2(b), a dither signal can be fed into the input of the DSM to randomize the pattern of ε_{qn} and thus the pattern of τ_{inl}. In this way, the power of the fractional spurs will be scrambled into random noise. When applying this kind of technique, care must be taken to cancel the noise from the dither signal; otherwise,

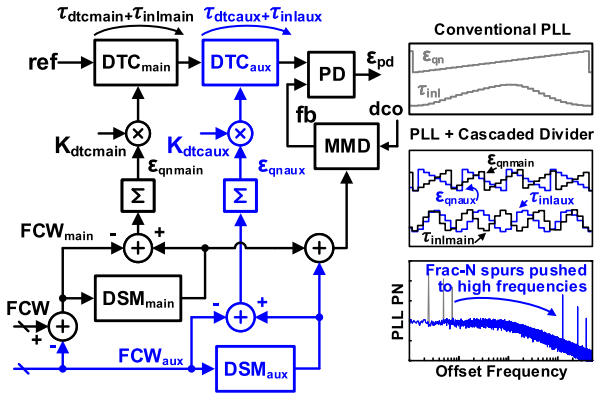


Fig. 3. Schematic and operation of the proposed cascaded fractional divider technique.

this noise will be transferred to the PLL output. Despite the random noise caused by the dither signal, the random noise floor will be elevated because of the spreaded fractional spur power. As a result, the improvement in the overall integrated jitter of the PLL could be limited, albeit the improvement in the fractional spur level is significant.

In order to suppress the fractional spur power without degrading the PLL locking time or elevating the random noise, we present a DPLL based on: 1) a cascaded fractional divider technique to shift the fractional spur to high frequency and 2) a pseudo-differential DTC (PD-DTC) technique with self-canceled even-symmetric nonlinearities [13]. This DPLL can achieve an integrated jitter of 143.7 fs and a worst-case fractional spur of −62.1 dBc from a 100-MHz reference.

The rest of this article is organized as follows. Section II introduces the proposed cascaded fractional divider technique and the corresponding optimal FCW allocation based on the analysis of fractional spurs generated by the DTC nonlinearity. Section III introduces the mechanism of even-symmetric nonlinearity cancellation in the PD-DTC, as well as the mismatch analysis, the noise analysis, and the implementation details of the PD-DTCs. The other implementation details of this DPLL are disclosed in Section IV. The measurement results, as well as a comparison to other recent fractional PLLs, are reported in Section V. In the end, we conclude this work in Section VI.

II. Cascaded Fractional Divider

A. Cascaded Fractional Divider Concept

Apart from dither and DPD, the fractional spurs at near-integer channels can be suppressed if these spurs can be pushed to higher frequencies. In [14], an offset was added to the DSM of a charge pump (CP) PLL to shift the accumulated QN pattern to a higher frequency. However, the employed PD faced a wider input range because of the offset frequency, which resulted in a degraded PD linearity. Moreover, the mechanisms of the fractional spur generation by PD nonlinearity and DTC nonlinearity, which will be disclosed later, are different, hindering the direct application of this technique to a DPLL. A cascaded PLL where all of the two stages were in fractional-N mode was reported in [15] to avoid low-frequency fractional spurs at the cost of one more PLL, which led to a moderate figure-of-merit (FoM) performance.

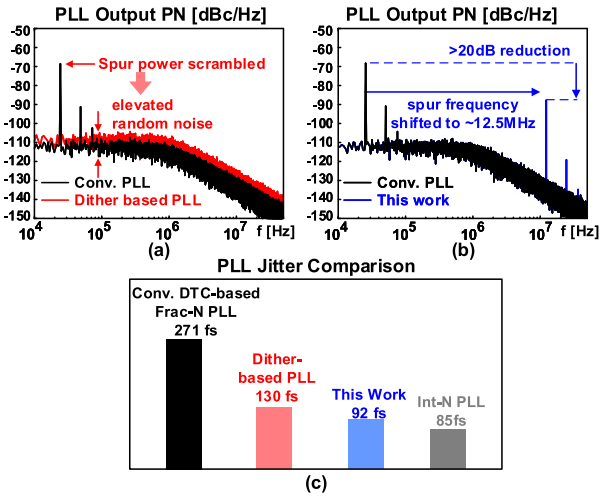


Fig. 4. Simulated spectrum of a DTC-based PLL with (a) dithering technique, (b) proposed cascaded divider technique, and (c) integrated jitter comparison of PLLs with different techniques.

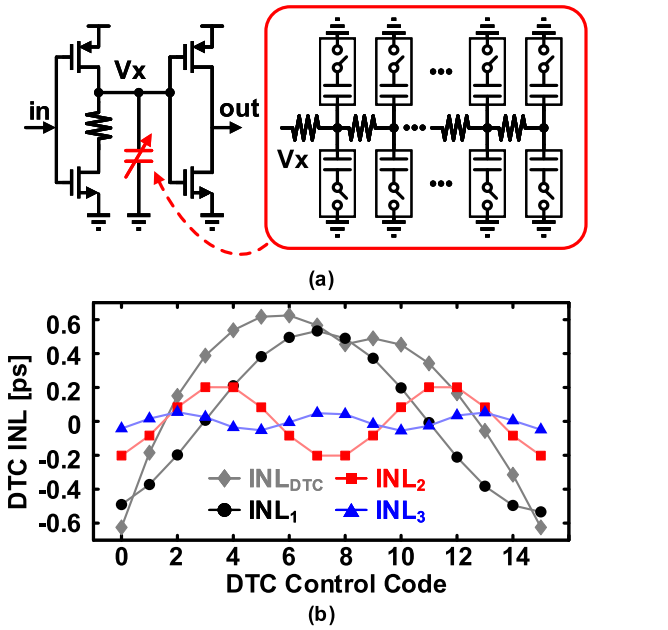


Fig. 5. (a) Schematic and (b) INL profile of a VS-DTC with layout-dependent parasitic resistance.

As shown in Fig. 3, a similar effect can be achieved by the proposed cascaded divider technique. With this technique, an auxiliary $\mathrm{FCW_{aux}}$ is subtracted from the original FCW to generate the $\mathrm{FCW_{main}}$, which is the input of the $\mathrm{DSM_{main}}$. In this way, the accumulated QN from the $\mathrm{DSM_{main}}$ ($\varepsilon_{\mathrm{qnmain}}$) can be shifted to a frequency that is $\mathrm{FCW_{aux}}\,f_{\mathrm{ref}}$ higher than the original frequency. As a result, the pattern of the INL error from the $\mathrm{DTC_{main}}$, which is used to cancel the $\varepsilon_{\mathrm{qnmain}}$, can also be pushed to a higher frequency. However, by simply subtracting $\mathrm{FCW_{aux}}$ from the original FCW, the PLL output frequency will also be shifted to $\mathrm{FCW_{aux}}\,f_{\mathrm{ref}}$ away. For this reason, another auxiliary $\mathrm{DSM_{aux}}$ and $\mathrm{DTC_{aux}}$ pair is employed to compensate for this frequency drift. The INL error pattern from the $\mathrm{DTC_{aux}}$ repeats at a frequency of $\mathrm{FCW_{aux}}\,f_{\mathrm{ref}}$ and thus will also be sufficiently filtered by the PLL. Note that the resolution of the $\mathrm{FCW_{aux}}$ needs not to be the same as that of the original FCW. Rather, the $\mathrm{FCW_{aux}}$ is designed to be 3 bit in this work to simplify the design of the DTC control and gain calibration logic.

Fig. 4(a) and (b) shows the simulation results of a DTC-based PLL before and after being applied with the conventional dithering technique and the proposed cascaded fractional divider technique, respectively.[1] In the simulations, the DTC is assumed to exhibit a sine-shaped INL with 0.5-ps peak-to-peak amplitude ($\mathrm{INL_{pp}}$), and the PLL output frequency is assumed to be near 7 GHz. It can be seen that with the dithering technique, the fractional spur can be effectively removed. However, the in-band random noise is elevated by around 4 dB because of the spreaded spur power. On the other hand, the fractional spur location can be pushed to be larger than 12.5 MHz with an $\mathrm{FCW_{aux}}$ of 1/8, leading to a more than 20-dB suppression in the fractional spur power with no elevated in-band phase noise (PN) in our proposed PLL topology. The integrated jitters of different PLL topologies are compared in Fig. 4(c). It shows that without any distortion from DTC nonlinearity, the integrated jitter can be 85 fs in an integer-N PLL. The integrated jitter will be heavily degraded to 271 fs by the fractional spur in fractional-N mode, which can be suppressed to 130 fs with the dithering technique. Nevertheless, thanks to the strong filtering strength on the high-frequency fractional spur, the integrated jitter can be suppressed even lower to 92 fs with the proposed cascade fractional divider technique.

[1]The simulations are carried out by passing the DTC nonlinearity, DCO noise, and reference noise through the transfer function of a type-II PLL with a second-order multistage noise-shaping (MASH-1-1) DSM. [16]. Meanwhile, it needs to be clarified that given enough number of LUT elements and calibration time, DPD-based PLL can achieve an integrated jitter that is almost the same as an integer-N PLL.

B. DTC INL Decomposition

One may think of using an $\mathrm{FCW_{ref}}$ of 1/2 to further push the fractional spur frequency to $0.5\,f_{\mathrm{ref}}$, just like the case in [14]. This will unfortunately not always result in the optimal fractional spur performance because of the high-order harmonic components from the τ_{inl}. To understand this, the profile of the DTC nonlinearity needs to be investigated.

Fig. 5 shows an example of the commonly used VS-DTC, where the delay is controlled by turning on or off different units of a capacitor bank. The nonlinearity of the VS-DTC comes mainly from the following three mechanisms: 1) the charging slope at the V_x node is different across different DTC control codes, which will generate a code-dependent delay at the comparator stage [17]; 2) the physical distances between the V_x node and different unit switch-capacitor cells are different, which leads to a layout-dependent delay difference at the input stage [9]; and 3) the amount of the accumulated charge at the bottom plate of each capacitor cell depends on the switch ON/OFF state in the previous reference cycle, leading to the memory effect and degraded DTC nonlinearity [18].

All the abovementioned mechanisms contribute to the overall DTC INL ($\mathrm{INL_{dtc}}$), which is shown in Fig. 5(b) as a gray curve. For the convenience of analysis in this and Section III,

INL_{dtc} can be represented by the following Fourier series:

$$\begin{aligned}\text{INL}_{\text{dtc}}[D_{\text{ctrl}}] &= \sum_i \text{INL}_i \\ &= \sum_i \left[a_i \cos\left(2\pi i \frac{D_{\text{ctrl}}}{2^m - 1}\right) \right. \\ &\quad \left. + b_i \sin\left(2\pi i \frac{D_{\text{ctrl}}}{2^m - 1}\right)\right] \end{aligned} \tag{1}$$

where INL_i is the ith harmonic component of the DTC INL, m is the DTC number of bits, and D_{ctrl} is the DTC control code. The first three INL harmonics, INL_1, INL_2, and INL_3, are also plotted in Fig. 5(b) as black, red, and blue curves, respectively. It can be seen that, unlike the nonlinearity profile of a CP, which can be well-approximated by a second- or third-order polynomial [19], the harmonic components of the INL_{dtc} can be significantly different and more complicated depending on the specific topology and implementation of the DTC.

C. Optimal FCW Allocation

The optimal FCW_{aux} can be found by taking the previously analyzed INL_{dtc} profile into consideration. Because of the harmonic-rich nature of INL_{dtc}, it is not difficult to prove that when being mapped to ε_{qn}, the resulting periodical nonlinearity noise (PNN) of the DSM will also contain multiple harmonics [19], [20]. For the DSM with a given order, we can denote the possibility that ε_{qn} (and INL_{dtc}) resides on the pth "track" at kth reference cycle as $P_p[\text{k}]$. The PNN at the kth reference cycle can be expressed by the weighted average of the distortion caused by INL_{dtc}

$$\text{PNN}[k] = \sum_p \text{INL}_{\text{dtc}}^p[k] P_p[k] \tag{2}$$

where $\text{INL}_{\text{dtc}}^p$ represents the distortion generated by INL_{dtc} on pth track. Similar to (1), PNN can be represented by the following Fourier series:

$$\begin{aligned}\text{PNN}[k] &= \sum_j \text{PNN}_j[k] \\ &= \sum_j c_j \cos\left[2\pi j(\alpha + \text{FCW}_{\text{aux}})k + \varphi_j\right] \end{aligned} \tag{3}$$

where φ_j is the phase term that is related to the initial state of the DSM. Because the phase error information in a DPLL is handled in a discrete-time fashion [21], [22], each PNN_j can be further rewritten as

$$\text{PNN}_j[k] = c_j \cos\left[2\pi k \cdot \text{mod}((\alpha + \text{FCW}_{\text{aux}})j, 1) + \varphi_j\right] \tag{4}$$

where $\text{mod}(\cdot)$ denotes the modulo operation.

Equation (4) implies that the fractional spur frequency generated by the jth harmonic component of the PNN will appear at an offset frequency of $\text{mod}((\alpha + \text{FCW}_{\text{aux}})j, 1) \cdot f_{\text{ref}}$. For any integer $(\text{FCW}_{\text{aux}} \cdot j)$, the fractional spur will be aliased back to in-band, resulting in almost zero suppression strength because of the low-pass PLL characteristic.

TABLE I
FCW MAPPING TABLE OF THE CASCADED FRACTIONAL DIVIDER

FCW	FCW_{int}	FCW_{aux}	FCW_{main}
[N,N+1/8]	N	1/8	[1/8,1/4]
[N+1/8,N+1/4]	N	0	[1/8,1/4]
[N+1/4,N+3/8]	N	-1/8	[1/8,1/4]
[N+3/8,N+1/2]	N	-1/4	[1/8,1/4]
[N+1/2,N+5/8]	N	1/4	[3/4,7/8]
[N+5/8,N+3/4]	N	1/8	[3/4,7/8]
[N+3/4,N+7/8]	N	0	[3/4,7/8]
[N+7/8,N+1]	N	-1/8	[3/4,7/8]

Fig. 6 shows the pattern of the first three terms of the PNN when different FCW_{aux}s are selected.[2] It can be seen from Fig. 6(a) that when no FCW_{aux} is applied, the fractional spurs are located at αf_{ref}, $2\alpha f_{\text{ref}}$, and $3\alpha f_{\text{ref}}$, respectively. When an FCW_{aux} of 1/2 is selected, the fractional spurs generated by PNN_1 and PNN_3 can be moved to higher frequencies, resulting in much smaller spur amplitudes. However, the fractional spur generated by PNN_2 remains at the same frequency as the case of a 0 FCW_{aux}. In order to obtain sufficient filtering strength for all the dominant harmonic components of the PNN, an FCW_{aux} of 1/8 is selected in this work for near-integer FCWs.[3] As can be seen from Fig. 6(c), the fractional spurs generated by the first three harmonic components of the PNN can all be moved beyond the PLL bandwidth. Moreover, an FCW mapping table, as shown in Table I, is utilized to ensure a consistent fractional spur level across different frequency channels.

III. Pseudo-Differential DTC

Stronger fractional spur suppression can be achieved by reducing the INL_{dtc} amplitude, which can be realized by either implementing high-linearity DTCs or utilizing the range-reduction technique [23]. However, recent high-linearity DTC topologies such as the constant-slope DTC (CSDTC) [24] or the inverse-constant-slope DTC (ICS-DTC) [10] require extra bias currents, which increase the implementation complexity. On the other hand, further reducing the DTC range to $1/M$ inevitably introduces M phase mismatches that need to be calibrated, which will cost extra PLL settling time [12]. In this section, we introduce a different way to reduce the INL_{dtc} amplitude by a PD-DTC.[4]

[2]The amplitudes of PNN_1, PNN_2, and PNN_3 are assumed to be equal in Fig. 6, which will not affect the generality of the foregoing analysis.

[3]Generally, the FCW_{aux} should be selected according to the PLL bandwidth, the profile of PNN, and the in-band and out-of-band noise contributions, such that the PLL jitter can be minimized.

[4]The concept of using two DTCs was first proposed in [25] to cancel the common mode supply ripples. However, the effect of reducing INL was not reported in [25]. Recently, it was proposed in a patent [26] that a lower INL can be achieved by canceling out the nonlinearities which can be represented by even-order polynomials. Nonetheless, the detailed implementation, mismatch analysis, noise analysis, and design considerations were not covered in [25], which will be the focus of this section.

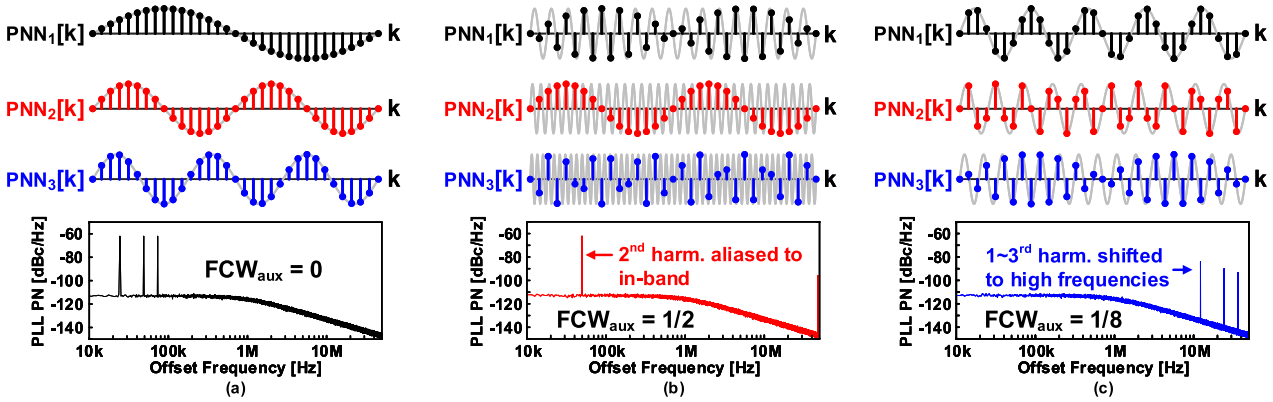


Fig. 6. Simulated PLL spectrum with the $\mathrm{FCW_{aux}}$ of (a) 0, (b) 1/2, and (c) 1/8, respectively.

A. PD-DTC Mechanism

With the PD-DTC technique, two identical DTCs (DTC_p and DTC_n) instead of one DTC are utilized to generate a relative delay to cancel the $\varepsilon_{\mathrm{qn}}$, as depicted in Fig. 7(a) and (b). When the $\varepsilon_{\mathrm{qn}}$ becomes larger, the delay of the DTC_p ($\tau_{\mathrm{dtc}p}$) is tuned to be longer, while the delay of the DTC_n ($\tau_{\mathrm{dtc}n}$) is tuned to be shorter. In this way, the required delay ranges for DTC_p and DTC_n are both halved, which leads to lower INL amplitudes in the two DTCs. Furthermore, the INLs of the two DTCs (INL_p and INL_n) can be expressed by the following two Fourier series:

$$\mathrm{INL}_p[D_{\mathrm{ctrl}}] = \sum_i \left[d_i \cos\left(2\pi i \frac{D_{\mathrm{ctrl}}}{2^m - 1}\right) + e_i \sin\left(2\pi i \frac{D_{\mathrm{ctrl}}}{2^m - 1}\right)\right] \quad (5)$$

$$\mathrm{INL}_n[D_{\mathrm{ctrl}}] = \sum_i \left[d_i \cos\left(2\pi i \frac{D_{\mathrm{ctrl}}}{2^m - 1}\right) - e_i \sin\left(2\pi i \frac{D_{\mathrm{ctrl}}}{2^m - 1}\right)\right]. \quad (6)$$

Note that the two INL profiles contain exactly the same even-symmetric components, which will cancel themselves due to the time-domain differential operation of the PD and result in the following equivalent INL ($\mathrm{INL_{diff}}$) profile:

$$\mathrm{INL_{diff}}[D_{\mathrm{ctrl}}] = \sum_i 2e_i \sin\left(2\pi i \frac{D_{\mathrm{ctrl}}}{2^m - 1}\right). \quad (7)$$

It needs to be clarified that although (7) implies a doubled odd-symmetrical INL components, an overall INL improvement can still be achieved, thanks to the lower INL amplitude that comes with the halved DTC delay ranges. The simulated INL_p, INL_n, and $\mathrm{INL_{diff}}$ are shown in Fig. 7(c) as black, red, and blue curves, respectively.[5] Due to the naturally low odd-symmetric INL components, the PD-DTC can achieve a much lower equivalent INL amplitude, which greatly relaxes the noise-power-linearity tradeoff in conventional DTC designs.[6] The single VS-DTC INL with only odd-symmetrical components is also shown in Fig. 7(c) as the gray curve. It can be seen that the amplitude of odd-symmetrical INL remains almost unchanged with the PD-DTC technique, indicating no INL degradation from the doubled odd-symmetrical INL components.

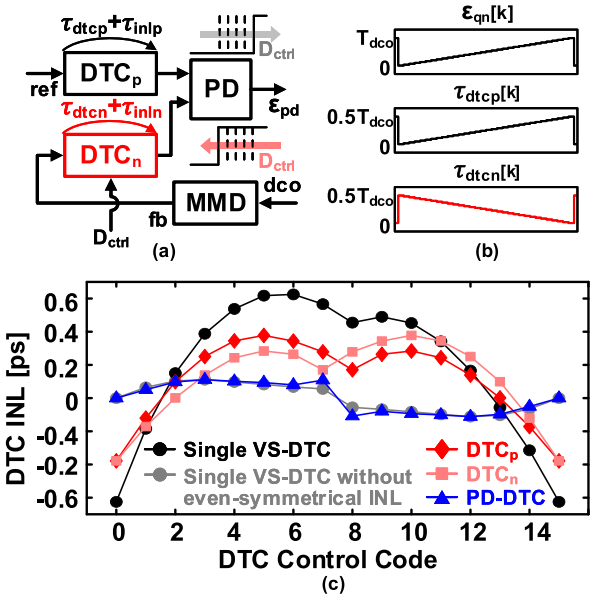


Fig. 7. Simplified schematic (a), operation (b), and even-symmetric INL cancellation effect (c) of the PD-DTC.

B. PD-DTC Implementation

In order to balance the design complexity, chip area, and DTC INL characteristics, care must be taken when implementing the PD-DTC. As will be described in Section IV, the most significant bits (MSBs) from $\varepsilon_{\mathrm{qnmain}}$ and $\varepsilon_{\mathrm{qnaux}}$ are canceled by $\mathrm{DTC_{main}}$ and $\mathrm{DTC_{aux}}$, respectively. However, if the DTC gain is controlled in the digital domain, considerably high hardware resources are required for the complicated multi-bit multiplication operations.

To this aim, a coarse–fine segment structure of the DTC is employed to cancel the $\varepsilon_{\mathrm{qnmain}}$. The coarse stage of the single DTC branch is shown in Fig. 8(a). The delay range of the DTC is controlled by passing the coarse DTC gain control code K_{dtcmain} to a voltage mode digital-to-analog converter

[5]The resistor of the DTC in Fig. 5(a) is adjusted to control the $\mathrm{DTC}_{p,n}$ delay ranges in the simulations.

[6]Another similar concept was presented in [27], where the time-domain differential operation was utilized to cancel the nonlinearities in a pair of phase interpolators.

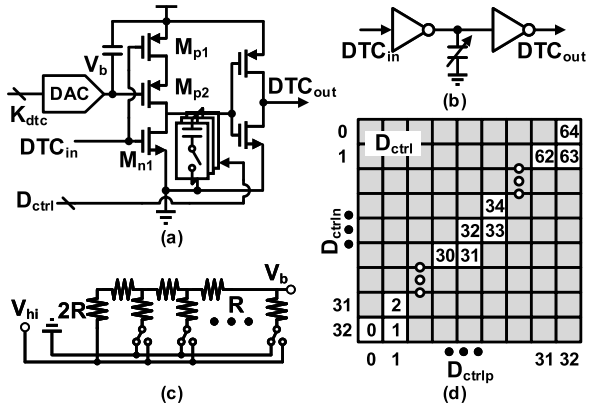


Fig. 8. Schematics of (a) single DTC branch of DTC_{main} and DTC_{aux}, (b) single DTC branch of DTC_{fine}, (c) R-2R ladder DAC for the gain control of DTC_{main} and DTC_{aux}, and (d) possible decoding scheme to improve the PD-DTC resolution.

(DAC), which is used to control the bias voltage (V_b) of the active resistor (M_{p2}). A 10-pF capacitor is connected between the V_b node and the DTC supply to bypass the supply ripple, which might modulate the ON-resistance of M_{p2}. In this way, a fine range resolution can be achieved in the coarse stage, which is sufficient to cancel all the MSBs of the ε_{qnmain} without generating any residue QN. Note that because the $K_{dtcmain}$ is usually fixed for a given frequency channel, the nonlinearities from the DAC do not generate any influence on the DTC INL. This allows a simple 10-bit R-2R ladder implementation for the DAC, which is shown in Fig. 8(c). The least significant bits (LSBs) of the ε_{qnmain} (ε_{qnfine}) are canceled by the fine DTC stage as shown in Fig. 8(b), where the delay is controlled by a capacitor bank that loads a simple inverter. The fine DTC control code is generated by multiplying the fine DTC gain ($K_{dtcfine}$) with the ε_{qnfine}, which requires a much smaller number of bits in the multiplication operation compared to a conventional fully digital DTC gain control scheme [6].

The two branches of the 6-bit DTC_{main} are controlled by the codes with inversed signs directly, which is the same for the 3-bit DTC_{aux}. When D_{ctrl} increases by 1, the control code for the p-branch (D_{ctrlp}) will also be increased by 1, while the control code for the n-branch (D_{ctrln}) will be decreased by 1 at the same time.

In order to improve the PD-DTC resolution, the decoding scheme in Fig. 8(d) is adopted for the 6-bit DTC_{fine}. In this decoding scheme, the control codes for the two branches are controlled separately as D_{ctrl} changes. Nevertheless, it is worth mentioning that the decoding scheme in Fig. 8(d) increases the risk of INL_{diff} degradation, which will be explained later in this section. This is also why the decoding scheme in Fig. 8(d) is not applied for the DTC_{main} and DTC_{aux}.

C. Mismatch Analysis

As mentioned earlier in this section, the mismatch between the two DTCs needs to be considered when implementing a PD-DTC. For the simplicity of analysis, the PD-DTC can be modeled as the circuits shown in Fig. 9(a), where R_p, stands for the ON-resistance contributed by M_{p1} and M_{p2} in the DTC_p; C_{fixp} stands for the fixed-value capacitance at the comparator input node in the DTC_p, which is mainly contributed by the parasitic gate-to-source capacitance; and $C_0 D_{ctrlp}$ stands for the capacitance of the capacitor bank in the DTC_p. Similarly, R_n, C_{fixn}, and $C_0 D_{ctrln}$ stand for the corresponding variables in the DTC_n. The relative delay (τ_{diff}) generated by the PD-DTC can, thus, be expressed by

$$\begin{aligned}\tau_{diff} &= \tau_{dtcp} - \tau_{dtcn} \\ &= R_p C_p \ln\left(\frac{V_{DD}}{V_{DD} - V_{thp}}\right) - R_n C_n \ln\left(\frac{V_{DD}}{V_{DD} - V_{thn}}\right) \\ &= \tau_{ofst} + \tau_{resp} D_{ctrlp} - \tau_{resn} D_{ctrln} \end{aligned} \tag{8}$$

where $C_p = C_{fixp} + C_0 D_{ctrlp}$ is the total capacitance at the DTC_p comparator input, $C_n = C_{fixn} + C_0 D_{ctrln}$ is the total capacitance at the DTC_n comparator input, $\tau_{ofst} = R_p C_{fixp} \ln((V_{DD}/(V_{DD} - V_{thp}))) - R_n C_{fixn} \ln((V_{DD}/(V_{DD} - V_{thn})))$ is a fixed term that will be nullified by the PLL, $\tau_{resp} = R_p C_0 \ln((V_{DD}/(V_{DD} - V_{thp})))$ is the delay resolution of the DTC_p, and $\tau_{resn} = R_n C_0 \ln((V_{DD}/(V_{DD} - V_{thn})))$ is the delay resolution of the DTC_n, respectively.

As implied by (8), the mismatch between C_{fixp} and C_{fixn} contributes only to the τ_{ofst} and thus will not degrade the INL_{diff} much.[7] On the other hand, any mismatches between R_p and R_n or between V_{thp} and V_{thn} will result in the mismatch between the code-to-delay gains of the DTC_p and the DTC_n, which might degrade INL_{diff} heavily depending on the DTC decoding scheme, as will be shown in the following.

For the DTC decoding scheme shown in Fig. 8(d), (8) can be re-written as follows by replacing D_{ctrlp} and D_{ctrln} with $\lceil 0.5 D_{ctrl} \rceil$ and $\lfloor 0.5 D_{ctrl} \rfloor$, where $\lceil \cdot \rceil$ denotes the ceiling operation and $\lfloor \cdot \rfloor$ denotes the flooring function

$$\begin{aligned}\tau_{diff}[D_{ctrl}] &= \tau_{ofst} + \tau_{resp} \left\lceil \frac{D_{ctrl}}{2} \right\rceil - \tau_{resn} \left\lfloor \frac{D_{ctrl}}{2} \right\rfloor \\ &= \tau_{ofst} + \hat{\tau}_{res} D_{ctrl} + \Delta\tau_{res}[D_{ctrl}]. \end{aligned} \tag{9}$$

In (9), $\hat{\tau}_{res} = ((\tau_{resp} + \tau_{resn})/2)$ is the effective resolution of the PD-DTC and $\Delta\tau_{res}[D_{ctrl}] = (-1)^{D_{ctrl}} \cdot ((\tau_{resp} - \tau_{resn})/2)$ is the term that represents the mismatch between the ideal and actual differential delays at D_{ctrl}. It can be seen that the sign of $\Delta\tau_{res}$ changes whenever D_{ctrl} increases by 1, which will generate a "sawtooth" pattern in the INL profile.[8]

Fig. 9(b) and (c) shows the 100-run Monte Carlo simulation results of the $DTC_{p,n}$ INL in Fig. 8(a). The delay range of each single branch is set to 140 ps for matching with the practical implementation. It can be seen that the INL spread due to the mismatch within $DTC_{p,n}$ can be as low as ±40 fs, while the average peak-to-peak INL amplitude is around 765 fs. The average INL amplitude can be further reduced to 297 fs with a spread of ±43 fs, as shown in Fig. 9(e), thanks to the pseudo-differential operation. This corresponds to approximately 8-dB fractional spur suppression in behavioral simulations. With the decoding scheme in Fig. 8(d), the average differential INL

[7]The mismatch between the delay offsets in DTC_p and DTC_n does cause the mismatch between the slope-induced nonlinearities in each DTC. This mismatch, however, will only generate insignificant degradation on the INL_{diff}.

[8]It needs to be clarified that the decoding scheme in Fig. 8(d) itself also creates the "sawtooth" pattern in the INL_{diff}, which is because of the interpolation between INL_p and INL_n. However, this will not degrade the INL_{diff} if the DTC_p and the DTC_n are perfectly matched.

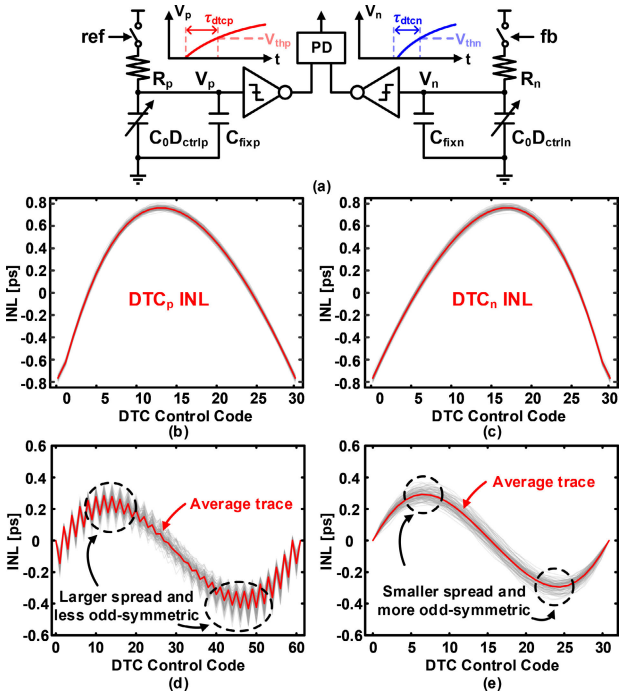


Fig. 9. (a) Mismatch analysis model of PD-DTC; and the overlay of 100 Monte Carlo simulations of the (b) DTC_p INL, (c) DTC_n INL, and PD-DTC INL (d) with and (e) without the decoding scheme to extend the equivalent PD-DTC number of bits.

amplitude of the PD-DTC will be degraded by the mismatch between DTC_p and DTC_n to 361 fs with a spread of ±55 fs, which is shown in Fig. 9(d).

D. PN Comparison With Single DTC

The PN difference between the single DTC and the PD-DTC is also necessary to be studied because the latter utilizes two DTCs, which might contribute to more in-band PN. Although a direct noise analysis is tedious, the PN comparison between the single DTC and the PD-DTC could be easy because the jitter, i.e., the PN of the DTC is related to only the amplitude of the noise voltage and the slew rate (SR) at the input node of the comparator stage [28]. For simplicity, we assume the nominal value of $V_{thp,thn}$ equals $0.5V_{DD}$ and represent the nominal values of $R_{p,n}$ and $C_{fixp,fixn}$ as R and C_{fix}, respectively. The SR at the time when V_p crosses $0.5V_{DD}$ can be calculated as $SR_p = (V_{DD}/(2R(C_{fix} + D_{ctrl}C_0)))$. Similarly, for node V_n, we can derive $SR_n = (V_{DD}/(2R(C_{fix} + (2^m - D_{ctrl})C_0)))$. The total jitter contributed by the PD-DTC (σ^2_{diff}) can then be expressed as

$$\begin{aligned}\sigma^2_{diff} &= \frac{\sigma_v^2}{SR_p^2} + \frac{\sigma_v^2}{SR_n^2} \\ &= \frac{4R^2\sigma_v^2}{V_{DD}^2} \cdot \left[(C_{fix} + D_{ctrl}C_0)^2 \right. \\ &\qquad \left. + \left(C_{fix} + \left(2^m - D_{ctrl}\right)C_0\right)^2\right] \end{aligned} \tag{10}$$

where σ_v^2 represents the overall voltage noise power contributed by the active resistor, switch transistor, etc.

Because the power consumption of the DTC is mainly determined by the total amount of charge dissipated at the

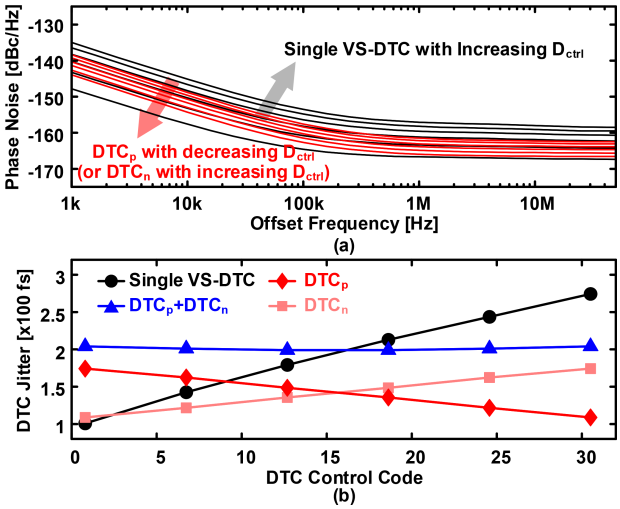


Fig. 10. Simulated (a) PNs of a single VS-DTC with 280-ps delay range and the two branch DTCs from a PD-DTC with the same differential delay range and (b) jitters contributed by the single VS-DTC and the PD-DTC.

capacitor in every cycle, a single VS-DTC with a capacitor bank, of which the unit capacitance is $2C_0$, is considered for a fair comparison. The SR of the single VS-DTC comparator input voltage when it crosses $0.5V_{DD}$ can be calculated as $SR_{se} = (V_{DD}/(2R(C_{fix} + 2D_{ctrl}C_0)))$. The jitter of the single VS-DTC can be expressed as

$$\sigma^2_{se} = \frac{\sigma_v^2}{SR_{se}^2} = \frac{4R^2\sigma_v^2}{V_{DD}^2} \cdot \left(C'_{fix} + 2D_{ctrl}C_0\right)^2 \tag{11}$$

where C'_{fix} is the fixed-value capacitance at the single VS-DTC comparator input node, which is usually different from C_{fix} due to the difference in the layout.

The difference between the PD-DTC and the single VS-DTC PN characteristics is, thus, revealed by (10) and (11): the PN power of the single VS-DTC increases monotonically with an increasing D_{ctrl}, while the PN power of the PD-DTC becomes lower when D_{ctrl} approaches the central value. As a result, the PN of the PD-DTC is not necessarily worse than that of the single VS-DTC when being applied with different delay control codes.

The post-layout simulations on the previously mentioned DTC_{main} and a single VS-DTC with the same delay range of 280 ps are conducted to verify the above noise analysis. Fig. 10(a) shows that with the increasing D_{ctrl}, the PN of the DTC_p in the PD-DTC increases and the PN of the DTC_n decreases. On the other hand, the PN of the single VS-DTC elevates with an increasing D_{ctrl}, which matches well with the predictions above. The jitters of different DTCs are also simulated across different DTC control codes, which are summarized and shown in Fig. 10. It can be seen that the jitter of the single VS-DTC does increase monotonically with the D_{ctrl}, while the total jitter of the PD-DTC becomes lower when D_{ctrl} approaches the central code. Moreover, at the central DTC control code, the jitter of the PD-DTC is almost the same

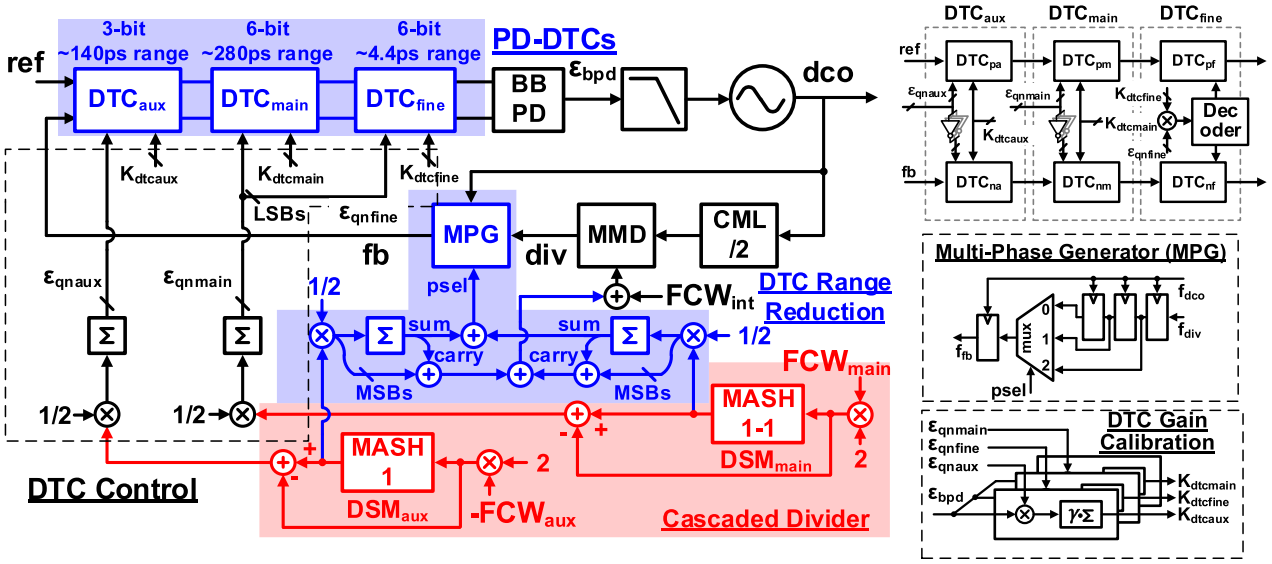


Fig. 11. Implemented DPLL with the cascaded fractional divider, PD-DTCs, DTC range reduction, and LMS-based DTC gain calibrations.

with the jitter of the single VS-DTC, implying on average no or negligible jitter degradation.[9]

IV. Implementation of the DPLL

The detailed schematics of the implemented DPLL utilizing the aforementioned cascaded fractional divider and PD-DTC techniques are shown in Fig. 11. A bang-bang PD (BBPD) is utilized in the DPLL to reduce the power consumption from the multi-bit time-to-digital converter (TDC). A MASH-1-1 DSM is used as the DSM_{main} for generating enough randomness on the $\varepsilon_{\text{qnmain}}$, which is helpful in accelerating the DTC gain calibration at near-integer channels. A MASH-1 DSM is used as the DSM_{aux} in order not to extend the required delay range of the DTC_{aux}, which might cause in-band PN degradation. Similar to the DTC_{main} and DTC_{fine}, the $\varepsilon_{\text{qnaux}}$ is canceled by a PD-DTC_{aux}. For design simplicity, the 3-bit DTC_{aux} is implemented by reusing the DTC_{main} with the LSBs of the DTC control code tied to the ground. The differential delay range of the DTC_{aux} is around 140 ps. The DTC retiming technique in [29] is applied for suppressing the memory effect in all the DTCs.

The gains of the DTC_{main}, DTC_{fine}, and DTC_{aux} are all calibrated in the background by LMS-based calibrators [6]. The gain calibration loop bandwidth of DTC_{fine} is designed to be less than that of DTC_{main} and DTC_{aux} for avoiding racing between different loops. The convergence process of the DTC gain calibration is shown in Fig. 12(b), where $\text{FCW}_{\text{main}} = 2^{-3} + 2^{-10}$ and $\text{FCW}_{\text{aux}} = 2^{-3}$. This corresponds to a near-integer channel, where the DTC gain calibrations become slower. It shows that all the DTC gain calibrations can converge within 4000 reference cycles when the initial

[9]In the simulation, the transistor sizes in the single VS-DTC are doubled such that C'_{fix} can be controlled to be two times of the C_{fix}. For this reason, the flicker noise of single VS-DTC is lower for D_{ctrl} close to 0.

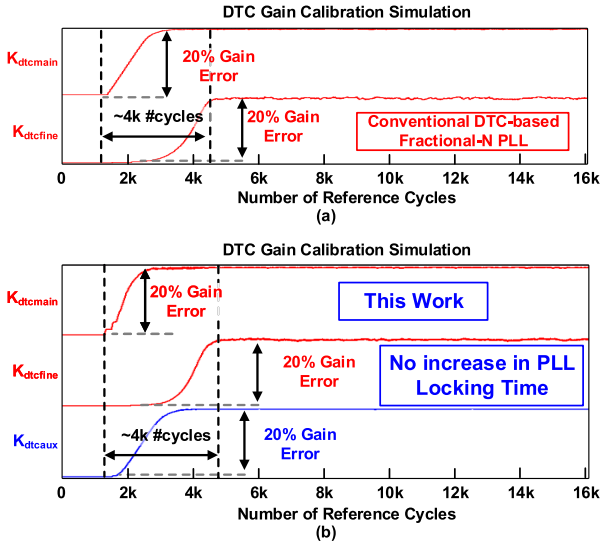


Fig. 12. Simulated convergence processes of the DTC gain calibrations in (a) conventional DTC-based fractional DPLL and (b) proposed DPLL with a cascaded fractional divider and PD-DTCs.

gain errors are both 20% away from the ideal values. In order to prove that no degradation in the DTC gain calibration time (and thus the PLL locking time) is generated in the implemented DPLL, the DTC gain calibrations of a conventional DTC-based DPLL are also simulated and shown in Fig. 12(a). It can be seen that in the conventional DTC-based DPLL, the DTC gain calibrations take only slightly less than 4000 reference cycles to converge with the same initial gain errors, which is almost the same as the case of our proposed DPLL. Note that in the simulation of Fig. 12(a), the fractional FCW is set to be equal to the FCW_{main} ($2^{-3} + 2^{-10}$) in Fig. 12(b) for a fair comparison. When the same near-integer channel is being synthesized, the calibration in a conventional PLL can become slower due to the reduced

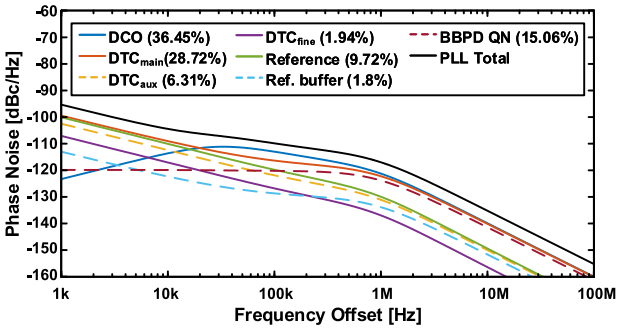


Fig. 13. PN breakdown according to Z-domain analysis.

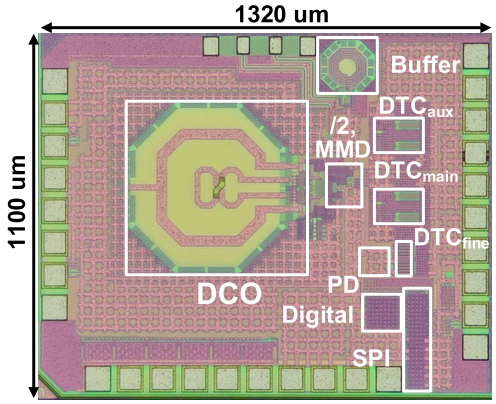


Fig. 14. Die micrograph of the proposed DPD/dither-free DPLL.

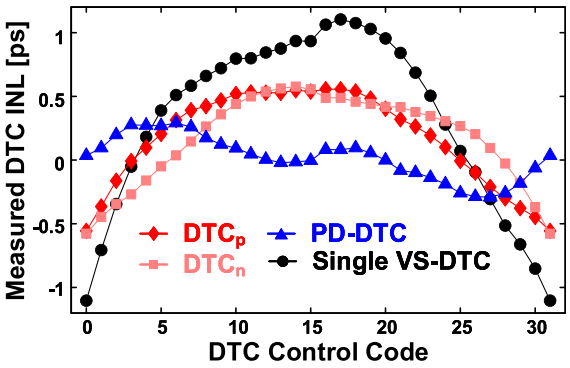


Fig. 15. Measured INLs of a single VS-DTC with 280-ps delay range and a PD-DTC pair with a 280-ps differential delay range.

correlation between BBPD output and DTC gain errors. On the other hand, although no special techniques are implemented in the proposed DPLL to mitigate the long frequency locking time caused by the limited BBPD gain, the gear-shifting technique in [30] can be readily applied.

Because the DCO is working with an output frequency of 6.5–7.5 GHz, a by-2 divider based on the current mode logic (CML) is used as a prescaler to avoid possible malfunctions in the MMD [15]. However, the required delay ranges of all the DTCs need to be doubled to cover the output period of the CML divider, which will cause the in-band PN degradation of the DPLL. To mitigate this problem, the DTC range reduction technique in [23] is implemented. Furthermore, a multi-phase generator (MPG) is utilized to generate different MMD output phases from different DCO edges. It is worth mentioning that no phase mismatch calibration is required for the implemented DTC range reduction technique because the output of the MPG is retimed by the DCO clock, which yields a perfect one DCO period delay between the neighboring MPG output phases. The schematic of the MPG is also shown in Fig. 11. The PLL PN is analyzed according to the Z-domain model [21], which is shown in Fig. 13. Thanks to the shorter delay range, which induces less noise contribution from the active resistor M_{p2}, the overall jitter contribution from DTC_{aux} is roughly 6.31%. This indicates that no much noise overhead is generated by DTC_{aux}.

V. Measurement Results

This DPD/dither-free DPLL is implemented in the 65-nm CMOS process. Fig. 14 shows the die micrograph of the DPLL, and the core area is 0.23 mm^2. The reference frequency of the DPLL is 100 MHz, which is generated by a signal generator (Rhode&Schwarz SMA100A). The total power consumption of the DPLL is 8.89 mW, with the power breakdown as follows: the DTC_{main} consumes 0.67 mW, the DTC_{fine} consumes 0.5 mW, the DTC_{aux} consumes 0.58 mW, the DCO consumes 3.3 mW, the digital logic consumes 0.34 mW, the CML prescaler, MMD, BBPD, and other internal buffers consumes 3.5 mW.

A. DTC Nonlinearity Measurement

In order to validate the effect of the proposed PD-DTC, the nonlinearities of the PD-DTC and the single VS-DTC are measured with the method reported in [31]. When measuring the PD-DTC, the two inputs of the DTC_{main} are both connected to the 100-MHz reference directly, the DTC K_{main} is adjusted manually to match the differential delay range of the PD-DTC to twice the DCO period, i.e., around 280 ps. On the other hand, only one DTC branch of the DTC_{main} is used for the single VS-DTC INL measurement. In this scenario, the K_{main} is adjusted to match the delay range of the measured VS-DTC branch to around 280 ps.

The measured INL profiles of the single VS-DTC and the PD-DTC are shown in Fig. 15. The INL_{pp} of the single VS-DTC is larger than 1.1 ps. Thanks to the halved delay range in each DTC branch of the PD-DTC, the INL_{pp} can be reduced to less than 600 fs. Moreover, an even lower differential INL_{pp} of less than 300 fs can be achieved. This corresponds to an improvement from 0.79% to 0.21% when being referred to the whole DTC delay range, leading to a much lower fractional spur level when being applied to the PLLs. Although the INL of DTC_{aux} cannot be measured, simulation shows that the differential INL_{pp} of DTC_{aux} is roughly 100 fs. When being filtered by less than 1-MHz bandwidth, the corresponding spur at 12.5 MHz can be less than -81 dBc, which is equivalent to approximately 3-fs jitter and will not limit the PLL spur/jitter performance.

B. DPLL Measurement

The PN spectrum and reference spur level of the DPLL in an integer-N channel of 7 GHz are shown in Fig. 16. The DPLL exhibits an integrated jitter of 115.3 fs with an integration

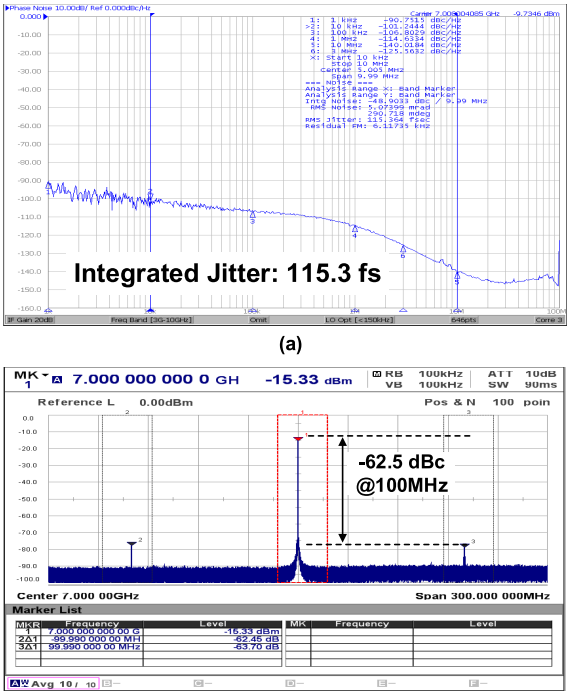


Fig. 16. Measured (a) PLL PN spectrum and (b) reference spur level when the PLL output frequency is 7 GHz.

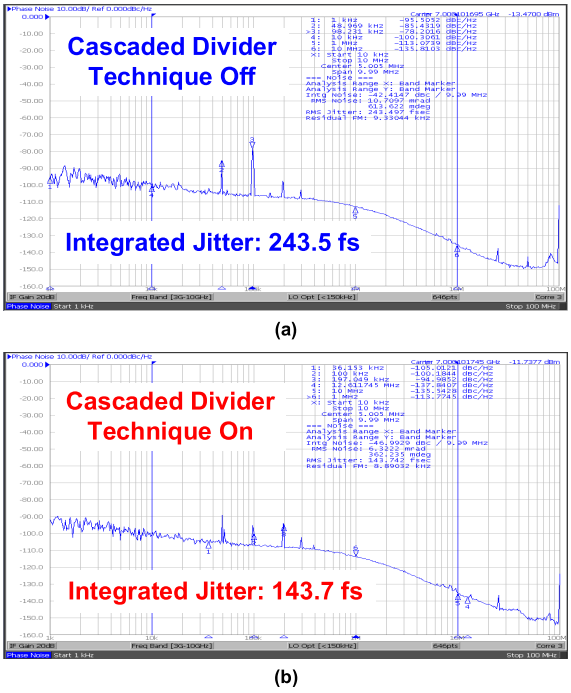


Fig. 17. Measured PLL PN spectrum (a) before and (b) after turning on the cascaded fractional divider technique at 7 GHz + 97.7 kHz.

bandwidth of 10 kHz–10 MHz. The reference spur level is measured to be −62.5 dBc.

The DPLL performances with and without the proposed cascaded divider technique are also measured at the fractional channel near 7 GHz. The measured fractional-N DPLL

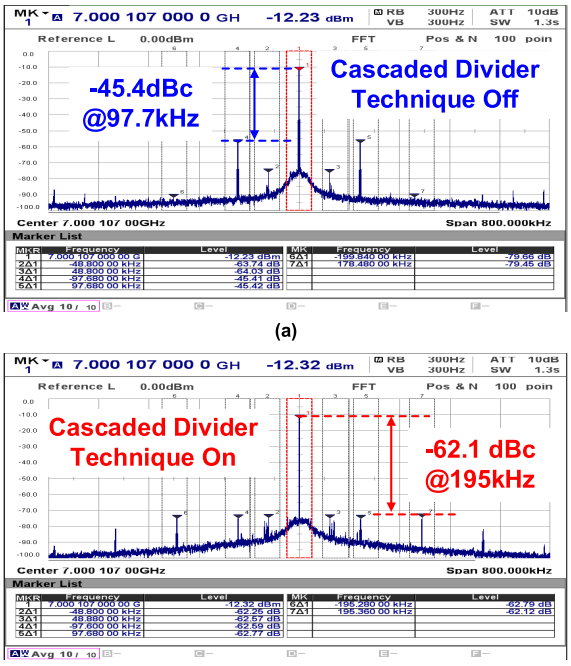


Fig. 18. Measured PLL output spectrum (a) before and (b) after turning on the cascaded fractional divider technique at 7 GHz + 97.7 kHz.

spectra are shown in Fig. 17. When the cascaded fractional divider technique is turned off, the DPLL integrated jitter is heavily degraded to 243.5 fs by the fractional spurs falling below the PLL bandwidth. When the cascaded fractional divider technique is turned on, the PNN pattern can be pushed to a higher frequency, which is then filtered by the loop characteristics and leads to a much lower integrated jitter of 143.7 fs. The fractional spur levels before and after turning on the cascaded fractional divider technique are measured and shown in Fig. 18.[10] It can be seen that before turning on the cascaded fractional divider technique, the worst fractional spur shows a level of −45.4 dBc with a 97.7-kHz offset frequency ($100/2^{10}$ MHz). After turning on the cascaded fractional divider technique with FCW_{aux} of 2^{-3}, the worst fractional spur is located at 195-kHz offset frequency ($100/2^{9}$ MHz), showing an amplitude of −62.1 dBc. The high-frequency fractional spurs of the PLL before and after turning on the cascaded fractional divider technique are shown in Fig. 19(a) and (b), respectively. It shows a less than −71-dBc fractional spur at 12.5977 MHz (12.5 MHz + 97.7 kHz). The PLL spectra at 7 GHz + 6 kHz before and after turning on the cascaded fractional divider technique with FCW_{aux} of 2^{-3} are shown in Fig. 20. The jitter integration bandwidth was extended to 1 kHz for covering all the fractional spurs, which shows a jitter improvement from 234.7 to 151 fs. The fractional spur measurement at the same frequency is shown in Fig. 21, which shows the worst spur level of −44.9 dBc at 6-kHz offset before turning on the cascaded fractional divider

[10]The correct PLL frequency is 7 GHz + 97.7 kHz, which is different from the frequency shown in the spectrum because of the limited absolute frequency resolution of the measurement equipment.

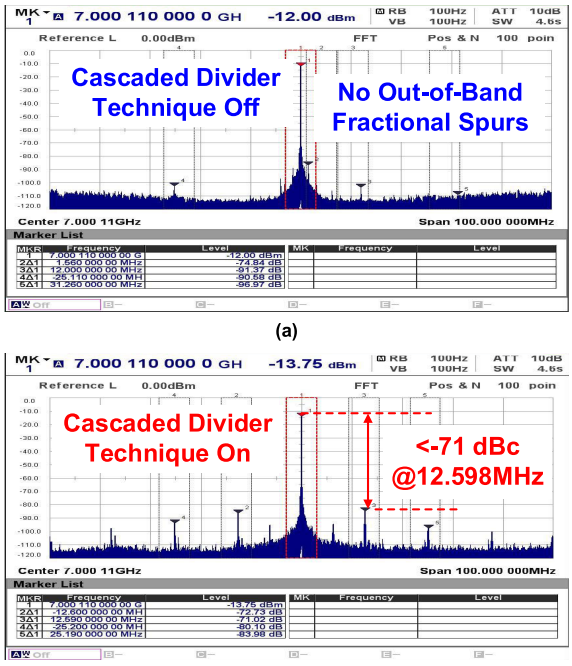


Fig. 19. Measured wide-span PLL output spectrum (a) before and (b) after turning on the cascaded fractional divider technique at a 7 GHz + 97.7 kHz.

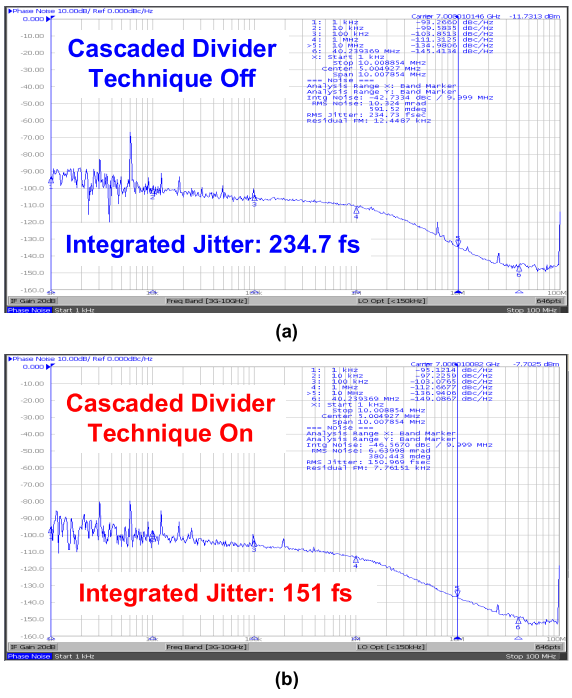


Fig. 20. Measured PLL PN spectrum (a) before and (b) after turning on the cascaded fractional divider technique at 7 GHz + 6 kHz.

technique, and −62.3 dBc at 6 kHz after turning on the cascaded fractional divider technique.

The fractional spur levels at different fractional-N channels near 7 GHz are also measured, which is shown in Fig. 22(a). It is observed that for the fractional spurs that fall below the PLL bandwidth, more than 15-dB suppression can be achieved

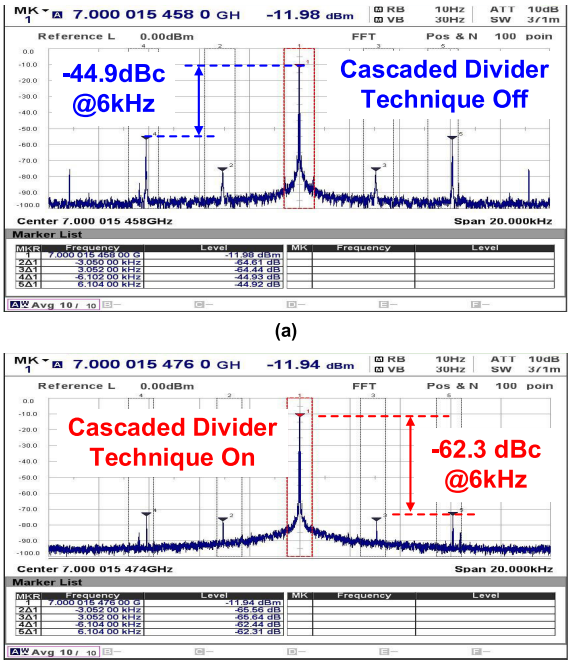


Fig. 21. Measured PLL output spectrum (a) before and (b) after turning on the cascaded fractional divider technique at 7 GHz + 6 kHz.

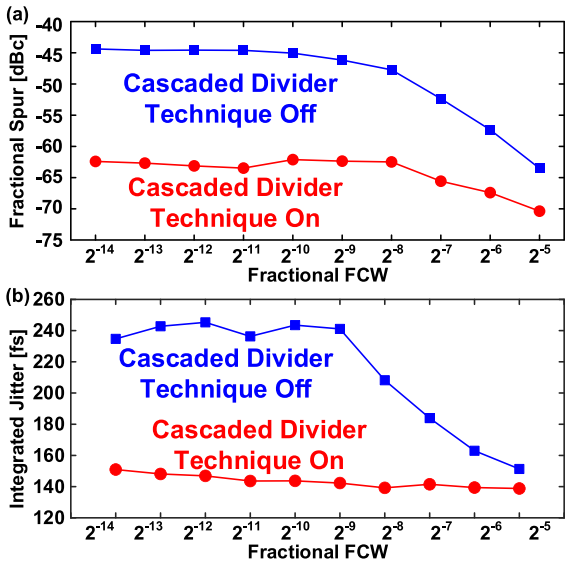


Fig. 22. (a) Measured worst-case fractional spur and (b) integrated jitter across different fractional channels near 7 GHz.

with the proposed cascaded fractional divider technique. The measured integrated jitter at the corresponding fractional-N channels is shown in Fig. 22(b), in which a larger than 80-fs jitter improvement can be achieved when the fractional spurs fall in the PLL bandwidth.

One may notice that as a first-order estimation, the measured INL shown in Fig. 15 should lead to a $20\log(\pi/2 \cdot \mathrm{INL_{pp}}/T_{\mathrm{dco}}) \approx -49.6$-dBc fractional spur, which is roughly 5 dB lower than the measured worst-case in-band fractional spurs [7]. This mismatch is caused mainly by two mechanisms: 1) no on-chip low dropout (LDO) is used for

TABLE II
COMPARISON WITH OTHER RECENT FRACTIONAL PLLS

	This Work	G. Castoro ISSCC'23 [32]	M. Mercandeli ISSCC'21 [33]	A. Santiccioli JSSC'20 [18]	S. Dartizio JSSC'23 [10]	Z. Gao JSSC'23 [34]	J. Kim ISSCC'21 [35]	H. Liu JSSC'18 [36]	X. Gao ISSCC'16 [37]	W. Wu ISSCC'21 [23]
Process [nm]	**65**	28	28	28	28	40	65	65	28	14
Topology	**DPLL**	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	SPLL
Technique	**Cascaded Fractional Divider + PD-DTC**	Multi DTC	DTC Gain Calibration	Replica DTC + Retiming	ICS DTC + FCW Dither	TAU + DPD	VDAC + DPD	Isolated CS-DTC	Replica DTC+ Sampling TDC	DTC Range Reduction
w/i DPD?	**No**	No	No	No	No	Yes	Yes	No	No	No
Reference Frequency [MHz]	**100**	250	250	500	250	40	150	26	40	76.8
Output Frequency [GHz]	**6.5~7.5**	9.25~10.75	12.9~15.1	12.8~15.2	9.25~10.5	2.56~4.1	14~16	2.0~2.8	2.7~4.3	6.2
Fractional Spur [dBc] (Normalized to 1GHz)	**-62.1 (-79)**	-60.3 (-79.6)	-50.4 (-72.7)	-61 (-83.6)	-71.9 (-91.2)	-59 (-67.5)	-61 (-84.5)	-56 (-63.6)	-54 (-69.3)	-66.4*** (-82.2)
Integrated Jitter [fs]	**143.7**	77.1	107.6	66.2	76.7	182	104	530	159	93.2
Integration Bandwidth [Hz]	**10k~10M**	1k~100M	1k~100M	1k~100M	10k~100M	10k~40M	10k~30M	10k~10M	10k~40M	10k~40M
Reference Spur [dBc]	**-62.5**	-71.1	-73.2	-80.1	-70.5	-73.5	N/A	-72	-78	-70.5
Power [mW]	**8.89**	17.9	10.8	19.8	17.2	3.48	7.3	0.98	8.2	14.2
FoM* [dB]	**-247.4**	-249.7	-249.0	-250.6	-249.9	-249.4	-251.0	-246	-246.8	-249.1
FoM_{ref}** [dB]	**-237.4**	-235.8	-235.1	-233.6	-236.0	-243.4	-239.3	-241.85	-240.78	-240.2
Area [mm^2]	**0.23**	0.36	0.16	0.17	0.33	0.31	0.21	0.23	0.3	0.31

*FoM = 10log[(Power/1mW)(Jitter/1s)^2] **FoM_{ref} = 10log[(Power/1mW)(Jitter/1s)^2] + 10log(f_{ref}/10MHz) ***Normalized to output frequency

regulating the supply of DTCs, which leads to the residue memory effect and thus INL degradation even though the DTC retiming technique is implemented [29] and 2) the DTCs are interfering with each other through the shared ground. As a result, the DTC_{aux} delay becomes dependent on the control code of DTC_{main}, which in turn causes extra degradation in DTC_{main} INL. The INL degradation from the abovementioned two mechanisms cannot be captured by the results shown in Fig. 15, which is only effective for code-independent INL errors. Fortunately, fractional spurs can still be suppressed by the cascaded fractional divider technique under the existence of memory effects.

On the other hand, the measured DTC_{main} INL in Fig. 15 shows a second-order harmonic with an amplitude of 70 fs. Because the same structure is also used as DTC_{aux}, the phase error induced by DTC_{aux} INL (driven by MASH-1 DSM_{aux}) may exhibit strong second harmonic at 25 MHz. Moreover, other circuits such as BBPD and DCO also contribute to nonlinearities and cause the mixing effect of phase error generated by DTC_{main} and DTC_{aux} INLs. Behavioral simulation shows that the 195-kHz spur in Fig. 18(b) originates from the mixing of second-order phase error harmonic components generated by DTC_{main} and DTC_{aux} INLs at 25 MHz + 195 kHz and 25 MHz, respectively. Moreover, coupling between different building blocks is also a limiting factor for further reducing the fractional spur power. For example, the CML divider can cause a ripple of 3.5 GHz + 48.8 kHz on the DTC supplies. This ripple will modulate the DTC delay and induce the 48.8-kHz fractional spur in Fig. 18(a) and (b).

Table II summarizes the performance of recent PLLs [10], [18], [23], [32], [33], [34], [35], [36], [37]. It can be seen that the DPLL in this work can achieve a very competitive performance, especially the fractional spur performance, which is even better than some works with DPD. Fig. 23 shows a comparison of PLLs with less than 60-dB fractional spurs

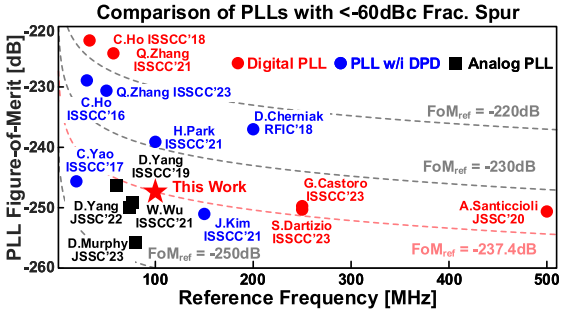


Fig. 23. Comparison of PLLs with less than 60-dBc fractional spurs.

[38], [39], [40], [41], [42], [43], [44], [45], [46]. Thanks to the cascaded fractional divider technique and the PD-DTCs, this DPLL can achieve a fractional spur suppression without any noise penalty below the PLL bandwidth, leading to an FoM_{ref} of −237.4 dB, which is the best among recent DPD-less DPLLs. It should be clarified that the proposed two fractional spur suppression techniques can be readily integrated together with DPD techniques for achieving stronger fractional spur suppression when it is allowed by the PLL locking time specification. Because the INL of PD-DTC is dominated by odd-symmetrical components, the number of required LUT elements can be reduced if the DPD scheme in [9] is used. Meanwhile, careful layout techniques can be adopted to reduce the high-order harmonic DTC INL components caused by layout parasitic. In that case, a simple 1/2 FCW_{aux} can be used, which can greatly relax the area and noise penalty caused by DTC_{aux} because the required DTC_{aux} differential delay range can be half of the DCO cycle.

VI. CONCLUSION

This work presents a 6.5–7.5-GHz DPD/dither-free DPLL in a 65-nm CMOS process. The presented DPLL demonstrates

an integrated jitter of 143.7 fs at the near-integer channel when working with a 100-MHz reference frequency. The power consumption of the DPLL is 8.89 mW, which leads to an FoM of -247.4 dB. A worst-case fractional spur level of -62.1 dBc is achieved without the help of any dithering, which might cause the elevation of random noise. Meanwhile, no DPD on the DTC INL is utilized in the presented DPLL, guaranteeing no overhead in the PLL locking time. These excellent characteristics are achieved by exploiting: 1) a cascaded fractional divider technique which can shift the in-band fractional spurs to the out-of-band for being filtered by the PLL and 2) PD-DTCs with self-canceled even-symmetric INL components, which greatly relaxes the noise-power-nonlinearity tradeoff in the conventional DTCs. When compared with DPD-less DPLLs with less than -60-dBc fractional spurs, the presented DPLL can achieve the best FoM_{ref} of -237.4 dB.

REFERENCES

[1] R. B. Staszewski et al., "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[2] H. Liu et al., "A DPLL-centric Bluetooth low-energy transceiver with a 2.3-mW interference-tolerant hybrid-loop receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3672–3687, Dec. 2018.

[3] D. Cherniak, L. Grimaldi, L. Bertulessi, R. Nonis, C. Samori, and S. Levantino, "A 23-GHz low-phase-noise digital bang-bang PLL for fast triangular and sawtooth chirp modulation," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3565–3575, Dec. 2018.

[4] B. Liu et al., "An HDL-described fully-synthesizable sub-GHz IoT transceiver with ring oscillator based frequency synthesizer and digital background EVM calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.

[5] Y. Jo et al., "A wideband LO generator for 5G FR1 bands using a single LC-VCO-based subsampling PLL and a ring-VCO-based fractional-resolution frequency multiplier," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3338–3350, Dec. 2023.

[6] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs_{rms} integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[7] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.

[8] B. Liu et al., "A fully synthesizable fractional-N MDLL with zero-order interpolation-based DTC nonlinearity calibration and two-step hybrid phase offset calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 2, pp. 603–616, Feb. 2021.

[9] C. Hwang, H. Park, Y. Lee, T. Seong, and J. Choi, "A low-jitter and low-fractional-spur ring-DCO-based fractional-N digital PLL using a DTC's second-/third-order nonlinearity cancellation and a probability-density-shaping $\Delta\Sigma$M," *IEEE J. Solid-State Circuits*, vol. 57, no. 9, pp. 2841–2855, Sep. 2022.

[10] S. M. Dartizio et al., "A low-spur and low-jitter fractional-N digital PLL based on an inverse-constant-slope DTC and FCW subtractive dithering," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3320–3337, Dec. 2023.

[11] Q. Zhang, H.-C. Cheng, S. Su, and M. S.-W. Chen, "Fractional-N digital MDLL with injection-error scrambling and calibration," *IEEE J. Solid-State Circuits*, vol. 59, no. 1, pp. 40–51, Jan. 2024.

[12] H. Park, C. Hwang, T. Seong, and J. Choi, "A low-jitter ring-DCO-based fractional-N digital PLL with a 1/8 DTC-range-reduction technique using a quadruple-timing-margin phase selector," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3527–3537, Dec. 2022.

[13] D. Xu et al., "10.3 A 7 GHz digital PLL with cascaded fractional divider and pseudo-differential DTC achieving -62.1dBc fractional spur and 143.7fs integrated jitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 67, Feb. 2024, pp. 192–194.

[14] H.-Y. Jian, Z. Xu, Y.-C. Wu, and M.-C. F. Chang, "A fractional-N PLL for multiband (0.8–6 GHz) communications using binary-weighted D/A differentiator and offset-frequency $\Delta - \Sigma$ Modulator," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 768–780, Apr. 2010.

[15] D. Xu et al., "A 6.5-to-8GHz cascaded dual-fractional-N digital PLL achieving -63.7dBc fractional spurs with 50MHz reference," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[16] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for $\Sigma - \Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.

[17] J. M. Daga and D. Auvergne, "A comprehensive delay macro modeling for submicrometer CMOS logics," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 42–55, Jan. 1999.

[18] A. Santiccioli et al., "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang–bang PLL with digital frequency-error recovery for fast locking," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3349–3361, Dec. 2020.

[19] V. Mazzaro and M. P. Kennedy, "Spur immunity in MASH-based fractional-N CP-PLLs with polynomial nonlinearities," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 6, pp. 2295–2306, Jun. 2021.

[20] Y. Donnelly and M. P. Kennedy, "Prediction of phase noise and spurs in a nonlinear fractional-N frequency synthesizer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 11, pp. 4108–4121, Nov. 2019.

[21] R. B. Staszewski and P. T. Balsara, "Phase-domain all-digital phase-locked loop," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 3, pp. 159–163, Mar. 2005.

[22] K. Kwon, O. A. B. Abdelatty, and D. D. Wentzloff, "PLL fractional Spur's impact on FSK spectrum and a synthesizable ADPLL for a Bluetooth transmitter," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1271–1284, May 2023.

[23] W. Wu et al., "A 14-nm ultra-low jitter fractional-N PLL using a DTC range reduction technique and a reconfigurable dual-core VCO," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3756–3767, Dec. 2021.

[24] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, Jun. 2015.

[25] A. Ba et al., "A 0.62 nJ/b multi-standard WiFi/BLE wideband digital polar TX with dynamic FM correction and AM alias suppression for IoT applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2018, pp. 308–311.

[26] A. S.-C. Li et al., "Differential digital-to-time converter for even-order INL cancellation and supply noise/disturbance rejection," U.S. Patent 11 387 833, Jul. 12, 2022.

[27] Z. Wang and P. R. Kinget, "A very high linearity twin phase interpolator with a low-noise and wideband delta quadrature DLL for high-speed data link clocking," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 1172–1184, Apr. 2023.

[28] A. Santiccioli, C. Samori, A. L. Lacaita, and S. Levantino, "Power-jitter trade-off analysis in digital-to-time converters," *Electron. Lett.*, vol. 53, no. 5, pp. 306–308, Mar. 2017. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/el.2016.4577

[29] W. Wu et al., "A 28-nm 75-fs_{rms} analog fractional-N sampling PLL with a highly linear DTC incorporating background DTC gain calibration and reference clock duty cycle correction," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1254–1265, May 2019.

[30] S. M. Dartizio et al., "A fractional-N bang-bang PLL based on type-II gear shifting and adaptive frequency switching achieving 68.6 fs-rms-total-integrated-jitter and 1.56 μs-locking-time," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3538–3551, Dec. 2022.

[31] C. Palattella, E. A. M. Klumperink, J. Z. Ru, and B. Nauta, "A sensitive method to measure the integral nonlinearity of a digital-to-time converter based on phase modulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 8, pp. 741–745, Aug. 2015.

[32] G. Castoro et al., "4.5 A 9.25 GHz digital PLL with fractional-spur cancellation based on a multi-DTC topology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 82–84.

[33] M. Mercandelli et al., "32.3 A 12.9-to-15.1GHz digital PLL based on a bang-bang phase detector with adaptively optimized noise shaping achieving 107.6fs integrated jitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 445–447.

[34] Z. Gao et al., "A low-spur fractional-N PLL based on a time-mode arithmetic unit," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1552–1571, Jun. 2023.

[35] J. Kim et al., "32.4 A 104-fs_{rms}-jitter and -61dBc-fractional spur 15 GHz fractional-N subsampling PLL using a voltage-domain quantization-error cancelation technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 448–450.

[36] H. Liu, D. Tang, Z. Sun, W. Deng, H. C. Ngo, and K. Okada, "A sub-mW fractional-N ADPLL with FOM of -246 dB for IoT applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3540–3552, Dec. 2018.

[37] X. Gao et al., "9.6 A 2.7-to-4.3 GHz, 0.16psrms-jitter, −246.8dB-FOM, digital fractional-N sampling PLL in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 174–175.

[38] C.-R. Ho and M. S.-W. Chen, "A fractional-N digital PLL with background-dither-noise-cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spurs in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 394–396.

[39] Q. Zhang, S. Su, C.-R. Ho, and M. S. Chen, "29.4 A fractional-N digital MDLL with background two-point DTC calibration achieving −60dBc fractional spur," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 410–412.

[40] C.-R. Ho and M. S.-W. Chen, "A digital PLL with feedforward multi-tone spur cancellation scheme achieving $< --73$ dBc Fractional Spur and $< --110$ dBc reference spur in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3216–3230, Dec. 2016.

[41] H. Park, C. Hwang, T. Seong, Y. Lee, and J. Choi, "32.1 A 365fs$_{rms}$-jitter and −63 dBc-fractional spur 5.3 GHz-ring-DCO-based fractional-N DPLL using a DTC second/third- order nonlinearity cancelation and a probability-density-shaping $\Delta\Sigma$M," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 442–444.

[42] C.-W. Yao et al., "24.8 A 14nm fractional-N digital PLL with 0.14psrms jitter and −78dBc fractional spur for cellular RFICs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 422–423.

[43] D. Cherniak et al., "A 15.6-18.2 GHz digital bang-bang PLL with −63 dBc in-band fractional spur," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 36–39.

[44] D. Yang et al., "16.6 A calibration-free triple-loop bang-bang PLL achieving 131fsrms jitter and −70 dBc fractional spurs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 266–268.

[45] D. Yang et al., "A harmonic-mixing PLL architecture for millimeter-wave application," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3552–3566, Dec. 2022.

[46] D. Murphy, D. Yang, H. Darabi, and A. Behzad, "A calibration-free fractional-N analog PLL with negligible DSM quantization noise," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2513–2525, Sep. 2023.

Dingxin Xu (Member, IEEE) received the B.Eng. degree from the Southern University of Science and Technology, Shenzhen, China, in 2018, and the M.Eng. and Ph.D. degrees from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2020 and 2024, respectively.

In the summer of 2023, he was an Intern with the RF/Analog Department, Qualcomm, San Diego, CA, USA, where he was designing a frequency synthesizer in an advanced technology node. He is currently a Post-Doctoral Researcher with the Institute of Science Tokyo. His research interests include mixed-signal circuit and frequency synthesizer design.

Dr. Xu was a recipient of Tokyo Tech Advanced Human Resource Development Fellowship for Doctoral Students from 2021 to 2023 and the ISSCC 2023 Student-Research-Preview (SRP) Poster Award. He serves as a reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, and IEEE SOLID-STATE CIRCUITS LETTERS.

Zezheng Liu (Graduate Student Member, IEEE) received the B.Sc. degree from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2019, and the M.E. degree in electrical and electronic engineering from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2021, where he is currently pursuing the Ph.D. degree.

His research interests include mixed-signal circuit and frequency synthesizer design.

Yifeng Kuai (Graduate Student Member, IEEE) received the B.Eng. degree from Shanghai Jiao Tong University, Shanghai, China, in 2021, and the M.Eng. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2023.

His research interest is phase-locked loop (PLL) design.

Hongye Huang (Member, IEEE) was born in Guilin, China, in 1994. He received the B.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2016, and the M.E. degree from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree.

He was an Intern with SiTime Japan, Tokyo, in 2022, where he developed digital signal processing for clock synthesis systems. His current research interests include mixed-signal integrated circuits, frequency synthesizers, and design automation for synthesizable clock circuits.

Mr. Huang currently serves as a reviewer for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS and IEEE ACCESS. He was a scholarship recipient of the Watanuki International Scholarship Foundation in fiscal years 2020 and 2021.

Yuncheng Zhang (Member, IEEE) received the B.S. and M.E. degrees in electrical engineering from the University of Science and Technology of China (USTC), Hefei, China, in 2013 and 2016, respectively, and the Ph.D. degree from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2022.

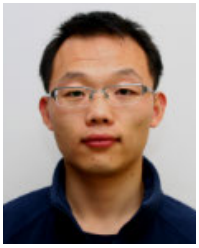
In 2022, he joined the Institute of Science Tokyo, as a Post-Doctoral Researcher, where he is currently an Assistant Professor. His research interests include power-efficient wireless transceivers, all-digital phase-locked loops, and analog-to-digital converters.

Dr. Zhang was a recipient of the Best Design Award at the IEEE/ACM ASP-DAC University Design Contest in 2021.

Zheng Sun (Member, IEEE) was born in Yancheng, China, in 1993. He received the B.S. degree in information engineering from Southeast University, Nanjing, China, in 2014, the M.S. degree in information, production, and systems engineering from Waseda University, Fukuoka, Japan, in 2015, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2021.

From April 2021 to July 2021, he was a Post-Doctoral Researcher with Tokyo Institute of Technology. He is currently with Apple Inc., Tokyo, working on wireless connectivity. He was involved in low-power transceivers for the Internet of Things, mixed-signal circuits, and low-power digital phase-locked loop (PLL) designs. His research interests include transceivers for Bluetooth low energy, low-power/high-performance LC-voltage-controlled oscillator (VCO) for industrial, scientific, and medical (ISM)/5G applications, and ultra-low-jitter PLLs for 5G cellular and harmonic suppression techniques for the power amplifier.

Dr. Sun currently serves as a reviewer for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the *Microelectronics Journal* published by Elsevier, and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Bangan Liu (Member, IEEE) received the B.Eng. degree from Northwestern Polytechnical University, Xi'an, China, in 2011, the M.S. degree from the University of Science and Technology of China, Hefei, China, in 2014, and the Ph.D. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He was an Intern with the Apple Japan Design Center, Tokyo, in 2019. He is currently with Qualcomm Inc., San Diego, CA, USA, where he develops high-performance 5G cellular radio frequency integrated circuits (RFICs). His research interests include frequency synthesizers, digital-intensive/digitally assisted mixed-signal systems, and RF/millimeter-wave (mm-wave) circuits.

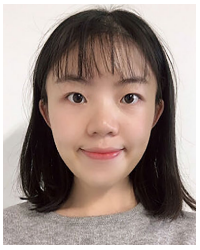
Dr. Liu also serves as a reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Wenqian Wang (Graduate Student Member, IEEE) was born in Xuancheng, China. He received the B.Eng. degree from the School of Microelectronics, Xidian University, Xi'an, China, and the M.Eng. degree from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, where he is currently pursuing the Ph.D. degree.

His current research interests include analog and mixed-signal circuits, as well as frequency synthesizers.

Yuang Xiong (Graduate Student Member, IEEE) received the B.Eng. degree from Beihang University, Beijing, China, in 2019, and the M.Eng. degree from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2022, where he is currently pursuing the Ph.D. degree.

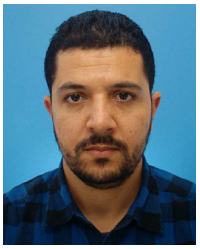
He is working on mixed-signal circuit design and his current interests include the Internet of Things (IoT) transceivers and frequency-modulated continuous-wave (FMCW) radar.



Junjun Qiu (Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the East China University of Science and Technology, Shanghai, China, in 2016, and the M.E. and Ph.D. degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2018 and 2022, respectively.

In 2023, she joined the Qualcomm Radio Frequency Integrated Circuit (RFIC) Design Group, San Diego, CA, USA, where she is currently a Senior Engineer and focuses on frequency synthesizer for wireless transceivers. She was focusing on fully synthesizable digital baseband circuit design for sub-GHz wireless transceiver system. Her current research interests include high-performance phase-locked loop design and mixed-signal wireless communication system design.

Dr. Qiu was a recipient of the IEEE SSCS Student Travel Grant Award in 2020 and the Predoctoral Achievement Award in 2021 and 2022.



Waleed Madany (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Aswan University, Aswan, Egypt, in 2012 and 2017, respectively. He is currently pursuing the Ph.D. degree with Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan.

His current research interests include a fully synthesizable digital phase-locked loop (DPLL) for frequency syntheses, clock generation, and digital calibrations for mixed-signal integrated circuits.

Yi Zhang (Member, IEEE) received the B.E. degree in microelectronic science and engineering from the Southern University of Science and Technology (SUSTech), Shenzhen, China, in 2018, and the M.E. degree in electrical and electronic engineering from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include both mixed-signal circuit design for millimeter-wave CMOS phased-array transceiver and power-efficiency receiver (RX) design for 5G and beyond-5G communication systems.

Ashbir Aviat Fadila (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Institut Teknologi Bandung, Bandung, Indonesia, in 2015, and the M.S. degree in electrical and electronic engineering from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

From 2015 to 2016, he was a Standard Cells Mask Layout Engineer with Marvell Technology Indonesia, Jakarta, Indonesia. From 2016 to 2017, he was a Research Assistant with the Institut Teknologi Bandung, researching system-on-chip (SoC) for the Internet of Things (IoT) applications. His current research interests include analog-mixed signals, data converters, and synthesizable analog circuits.

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed an 802.11ax wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motor with wireless communication. He is currently an Associate Professor with the Laboratory for Future Interdisciplinary Research of Science and Technology, Institute of Innovative Research, Institute of Science Tokyo. His current research interests include RF CMOS transceivers for the Internet of Things (IoT), 5G, and satellite communication and wireless power transfer.

Dr. Shirane is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE). Since 2019, he has been a member of the Technical Program Committee for IEEE International Solid-State Circuits Conference Student Research Preview.

Kenichi Okada (Fellow, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow with Japan Society for the Promotion of Science, Kyoto University. In 2003, he joined Tokyo Institute of Technology (now Institute of Science Tokyo), Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering. He has authored or co-authored more than 500 journal articles and conference papers. His current research interests include millimeter-wave and terahertz CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for 5G, WiGig, satellite and future wireless systems, digital phase-locked loop (PLL), synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low-energy, and sub-GHz applications.

Prof. Okada is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011, Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the Radio Frequency Integrated Circuits (RFIC) Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC Prolific Author Award in 2020, the Kenjiro Takayanagi Achievement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC, Best Paper Award in 2020, the IEEE ISSCC Author-Recognition Award in 2023, and more than 50 other international and domestic awards. He is/was a member of the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), RFIC Symposium, and A-SSCC. He is/was also a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).