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Analysis and Design of a Low-Loss 1–10 GHz Capacitive Stacking N-Path Filter/Mixer

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***Abstract*— This article presents a capacitive stacking N-path filter/mixer optimized for low losses over a wide 1–10 GHz RF range, implemented in 22-nm fully depleted silicon-on-insulator (FDSOI) technology. By making the baseband (BB) capacitor larger than the RF capacitor, the former will define the bandwidth (BW). As a result, the RF capacitor can be much smaller, effectively reducing the parasitic capacitance at the RF node and limiting the loss at 10 GHz to only 1.4 dB. The implications and limitations of this capacitive scaling technique are explored, and an eigenvalue-based analysis is presented to derive a transfer function (TF) and simple design equations. Using these design equations, a prototype has been implemented that achieves 20-MHz channel BW while occupying 0.05 mm^2 of active area. The design consumes 3.1-mW/GHz dynamic power with negligible static power and obtains a noise figure (NF) of 4.7–7.0 dB over an RF range of 1–10 GHz. The in-band (IB) input-referred third-order intercept point (IIP_3) is over 1 dBm across the RF range and across three samples, while the out-of-band IIP_3 is 17–28 dBm.**

***Index Terms*— Bottom-plate mixing, capacitive stacking, frequency-translated filter, fully depleted silicon-on-insulator (FDSOI), high linearity, impedance transformer, low loss, low noise, low parasitic capacitance, mixer-first receiver, N-path filter (NPF), N-path mixer, passive gain, passive mixer, RF front end, software-defined radio.**

I. Introduction

WIRELESS communication is crucial in our society, and a surge in devices is overcrowding the frequency spectrum. To meet the demand for spectrum availability, receivers need to be flexible, leading to software-defined radio architectures that focus on digital integration [1]. However, direct digitization, where the analog-to-digital-converter (ADC) is placed at the antenna, imposes specifications that cannot be met with today's ADCs at power consumption levels comparable to analog front ends [1] (the recent work in [2] requires 750 mW to achieve a sampling rate of 24 GS/s and a spurious-free dynamic range of 76 dB). Hence, front ends implement filtering and downconversion to ease the ADC requirements. In the end, the purpose of the front end is to fit the received signal in the dynamic range of the ADC with a maximum signal-to-noise-and-distortion ratio for a given power consumption, effectively requiring optimization of the front end's intermodulation-free dynamic range (IMFDR).[1] To optimize the IMFDR, the front end's distortion, noise, and losses should all three be minimized.

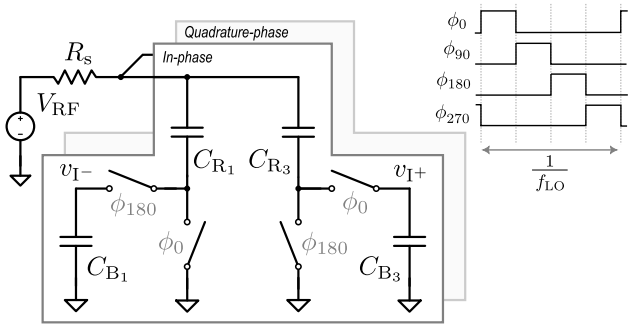

Fig. 1. Single-ended CSNPFM. In previous work, $C_R \gg C_B$. In this work, $C_R \ll C_B$, minimizing RF losses.

Distortion can be low in mixer-first receiver architectures, using a highly linear passive mixer and filtering to mitigate the impact of interference [5], [6], [7]. Linearity can further be improved through techniques such as "bottom-plate mixing" [8], bootstrapping [9], and using feedback to increase selectivity [4], [10], [11]. However, these techniques typically result in a degraded noise figure (NF) while increasing RF signal losses, power consumption, and circuit complexity. Additional filtering can also be realized by adding an N-path bandpass filter at the RF node [8], [12], but this adds considerable RF losses, limiting the receiver's usable frequency range.

To improve the noise performance, we can reduce the switch ON-resistance [6] or implement noise-canceling techniques [13], [14], [15], both at the cost of a considerable power penalty. Alternatively, low-noise transconductance amplifier (LNTA)-based implementations offer signal gain early in the receiver chain, relaxing noise constraints [16], [17]. However, the LNTA's nonlinearity forms a bottleneck in minimizing the front end's distortion, especially given today's low supply

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[1] Sometimes also referred to as "spurious-free dynamic range," but as multiple definitions exist, we prefer IMFDR [3] as used recently in [4].

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voltages, while the pole at its output limits the frequency range [18].

Recently, implicit capacitive stacking techniques have been introduced in mixer-first receivers that increase the signal through (passive) voltage gain before the noise-dominating stages [19], [20], [21], combining low distortion with an improved NF. However, these techniques introduce considerable RF losses, limiting the RF operating range. Furthermore, in capacitive stacking topologies, the increased numbers of nodes, switches, and voltage swings lead to linearity degradation. This results in diminishing benefits, especially when cascading multiple stages [22]. In [23], efforts have been made to reduce parasitic losses. However, the usable frequency range is still limited due to the harmonic rejection (HR) topology, which includes 24 relatively large C_{R} capacitors at the RF node.

In this work, we optimize the front end's IMFDR by striking a good balance between high linearity and low noise with minimal parasitics to avoid loss at high frequencies. We present a capacitive stacking N-path filter/mixer (CSNPFM) front end achieving $2\times$ passive voltage gain with low losses, to limit NF degradation. The passive nature of the circuit translates into excellent linearity performance, achieving good IMFDR at low power. Fig. 1 shows the proposed single-ended low-loss CSNPFM, in which C_{R} and C_{B} denote the RF and baseband (BB) capacitors, respectively. In previous work, the capacitance ratio $C_{\mathrm{R}}/C_{\mathrm{B}}$ was $\gg 1$ [19]. Similarly as in [23], we propose to flip this ratio, so the BB capacitor will mainly define the passband bandwidth (BW). This allows for a much smaller RF capacitor, effectively reducing the parasitic capacitance at the RF node, extending the RF operating range.

While the original CSNPFM's operation in [19] closely resembles a regular N-path filter/mixer, the proposed design with relatively small C_{R} capacitors behaves differently. In this work, we provide the detailed analysis of the consequences of using small RF capacitors and provide a comprehensive design guide for the design of the "low-loss" CSNPFM. We present an intuitive explanation of the low-loss CSNPFM circuit operation, highlighting the differences to the traditional CSNPFM and discuss the impact on the circuit's performance in Section II. In Section III, we enhance the existing adjoint network-based analysis methods and derive a transfer function (TF) and simplified design equations. Section IV provides the implementation details and measurement results. Finally, Section V concludes this article.

II. Low-Loss CSNPFM Concept

In this section, we explore the low-loss CSNPFM concept and relate its performance to that of the traditional CSNPFM and a regular top-plate N-path filter (NPF).

A. Design Exploration

Compared to non-stacking, top-plate NPFs, the CSNPFM has an improved NF due to the passive voltage gain. However, this improved NF comes at the cost of increased parasitic capacitances due to the required RF capacitors C_{R}. In the traditional CSNPFM, the parasitic capacitance from C_{R} dominates over the parasitic capacitance of the MOSFET switches, exhibiting considerable signal loss. To reduce these losses, we set out to explore the loss mechanisms caused by the parasitic capacitances associated with CSNPFMs.

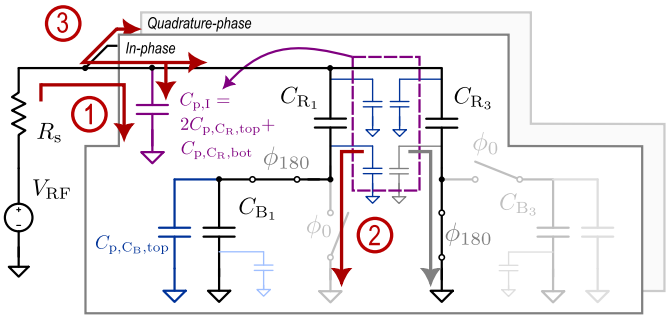

Fig. 2. Identification and lumping of parasitic capacitances in a CSNPFM, shown during clock phase ϕ_{180}, with loss mechanisms annotated: 1) $R_{\mathrm{s}}C_{\mathrm{p}}$ input pole attenuation; 2) switching loss; and 3) charge-sharing loss.

Before we start, it should be noted that, in the used technology, the parasitic capacitance for a given C_{R} is minimized by using optimized alternate polarity metal–oxide–metal (APMOM) capacitors. While a detailed discussion on the optimized implementation is provided in Section IV-A, for now, it is important to realize that an APMOM capacitor has equal parasitic capacitance from its top and bottom plates to the substrate at ground potential. Since the top-plate parasitic gives a similar loss as the parasitic at the bottom plate, we proceed with our exploration with a symmetric parasitic capacitance.

Now, we identify the parasitic capacitance associated with the capacitors of the in-phase CSNPFM kernel, Fig. 2 shows them for clock phase ϕ_{180}. We disregard $C_{\mathrm{p,C_B,bot}}$ as there is ground potential on the bottom side of all BB capacitors. We absorb $C_{\mathrm{p,C_B,top}}$ in C_{B} as they are in parallel. Since $C_{\mathrm{p,C_{R_1},bot}} \ll C_{\mathrm{R_1}}$, the parasitic capacitance associated with the bottom plate can be combined directly with the parasitic capacitance of the top plate at the RF node. The effective parasitic capacitance at the RF node for the in-phase kernel is therefore $C_{\mathrm{p,I}} = 2C_{\mathrm{p,C_R,top}} + C_{\mathrm{p,C_R,bot}}$. The total parasitic capacitance C_{p} at the RF node with $N = 4$ is obtained by adding two additional $C_{\mathrm{p,C_R,top}}$ and $C_{\mathrm{p,C_R,bot}}$ contributions from the other (inactive) quadrature-phase kernel: $C_{\mathrm{p}} = 4C_{\mathrm{p,C_R,top}} + 3C_{\mathrm{p,C_R,bot}}$. This expression generalizes to $C_{\mathrm{p}} = NC_{\mathrm{p,C_R,top}} + (N-1)C_{\mathrm{p,C_R,bot}}$ for $N \geq 4$ and an even number of phases.

We describe the parasitic capacitive loss mechanisms in more detail. Three mechanisms are at play: 1) $R_{\mathrm{s}}C_{\mathrm{p}}$ input pole attenuation; 2) switching loss; and 3) charge-sharing loss. Fig. 2 identifies these mechanisms.

The first mechanism is caused by a first-order pole at the input formed by C_{p} and R_{s}, resulting in signal loss through low-pass filtering.

The second loss mechanism is due to switching and occurs right after clock transitions. For instance, after $\phi_{90} \rightarrow \phi_{180}$, the fraction of the input signal stored on $C_{\mathrm{p,C_{R3},bot}}$ is shunted to ground, and right after $\phi_{180} \rightarrow \phi_{270}$, charge is replenished from the input again, leading to switching loss.

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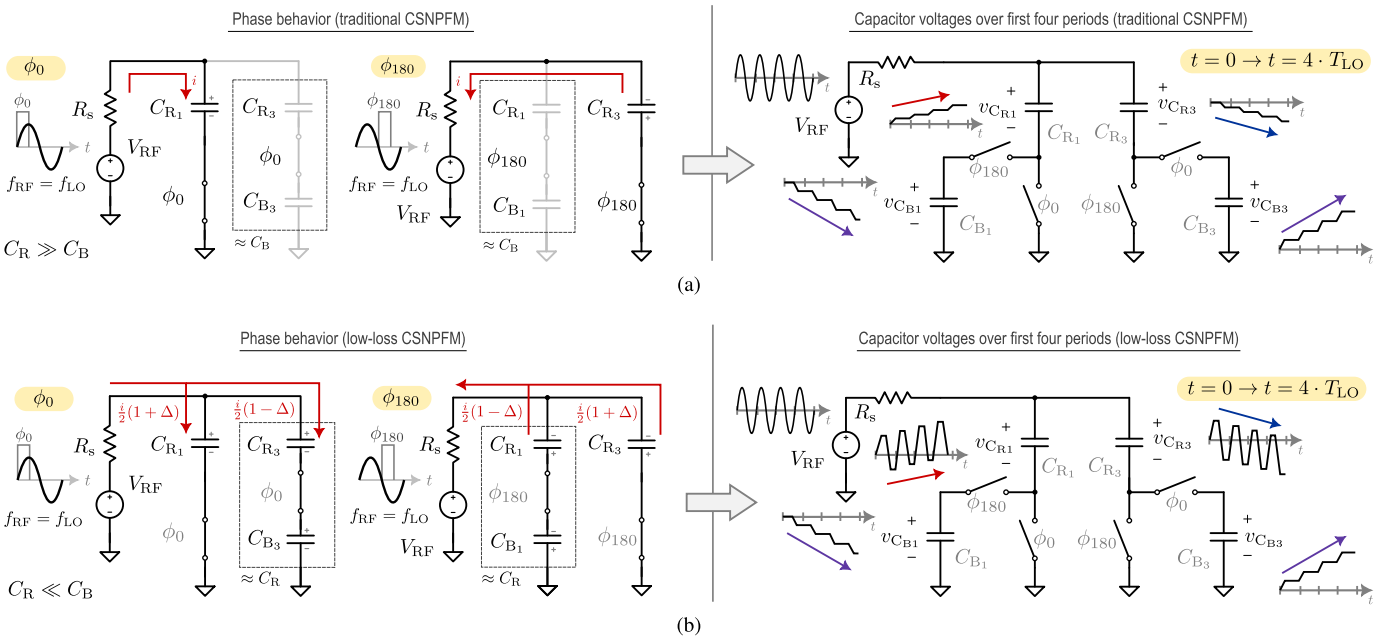

Fig. 3. Visualization of in-phase kernel start-up behavior with normalized BW for (a) traditional ($C_R \gg C_B$) and (b) low-loss ($C_R \ll C_B$) CSNPFM implementation.

The third loss mechanism can be understood from the time and frequency domains. In the time domain, the C_R capacitors of the different phases are consecutively connected to the ground. This results in charge-sharing loss between the normally isolated paths via parasitic capacitance C_p. Increasing N, for a constant C_p, reduces this loss, as the voltage difference of two consecutive C_R capacitors becomes smaller. In the frequency domain, C_p lowers the impedance at the RF node, effectively shunting the harmonic content of the upconverted BB signal to the ground. Increasing N lowers the harmonic content of the upconverted signal, resulting in lower loss [24], [25].

The loss of all three mechanisms can be minimized by reducing the total parasitic capacitance C_p. This parasitic capacitance depends on the technology, layout (see Section IV-A), and circuit design choices. We now explore how circuit design choices affect the parasitic capacitance, irrespective of technology and implementation. It is important to note that, given an optimized C_R implementation, the capacitance C_p scales linearly with C_R and is independent of C_B. Therefore, our primary goal is to minimize C_R. Solely minimizing C_R increases the (channel) BW. Nevertheless, the increase in BW can be compensated for by increasing C_B without harming C_p. This concept forms the foundation of the presented low-loss CSNPFM.

Note that the harmonic loss remains constant as f_{LO} increases, while the loss due to parasitic capacitance increases. In the proposed design with smaller C_R capacitors, the harmonic loss dominates over the capacitive loss for the lower local oscillator (LO) frequencies. Although this harmonic loss can be reduced by increasing the number of paths N, this requires additional switches and steeper clock edges, increasing power consumption and switch parasitics. Therefore, this work focuses on mitigating the parasitic capacitive loss while keeping N relatively low with four clock phases.

In the rest of this section, we describe the consequences of the presented low-loss CSNPFM for circuit behavior and performance. In the traditional CSNPFM [19], the role of C_B is limited to that of a readout capacitor. However, as shown in Section II-B, C_B plays an integral role in the circuit behavior of the presented low-loss design.

B. Intuitive Explanation

While the traditional CSNPFM's operation in [19] closely resembles that of a non-stacking NPF, the proposed design with relatively small C_R capacitors behaves differently. We will highlight the differences by analyzing the first few clock cycles of the in-phase kernel of both CSNPFMs using Fig. 3.

Consider the operation of the traditional CSNPFM [19], as visualized in Fig. 3(a). Since $C_R \gg C_B$, we find that the series combination of C_R and C_B effectively equals C_B. During each clock phase, such a C_R–C_B series combination is in parallel to a single much bigger C_R capacitor that therefore dominates the impedance connected to the source.

Let us assume that all capacitors are empty and apply an input to the circuit at $t = 0$ with a frequency equal to the clock, $f_{RF} = f_{LO}$. As we apply the input during ϕ_0, C_{R_1} will slowly charge to the average of the applied input voltage over multiple clock cycles (high-Q N-path filtering/mixing in the "mixing region" [26]: $RC \gg T_{on}$). The other C_R capacitor voltage (C_{R_3}) barely changes as the current is limited by the small series C_{B_3} capacitor. Thus, only a single (C_R) capacitor is considerably affected by the input during each clock phase, similar to non-stacking NPFs.

During the opposite clock phase of the kernel, ϕ_{180}, the capacitor roles are reversed. Now, C_{R_3} slowly charges to the average applied input, while the voltage on C_{R_1} barely changes. Because $f_{RF} = f_{LO}$ and this happens half a period

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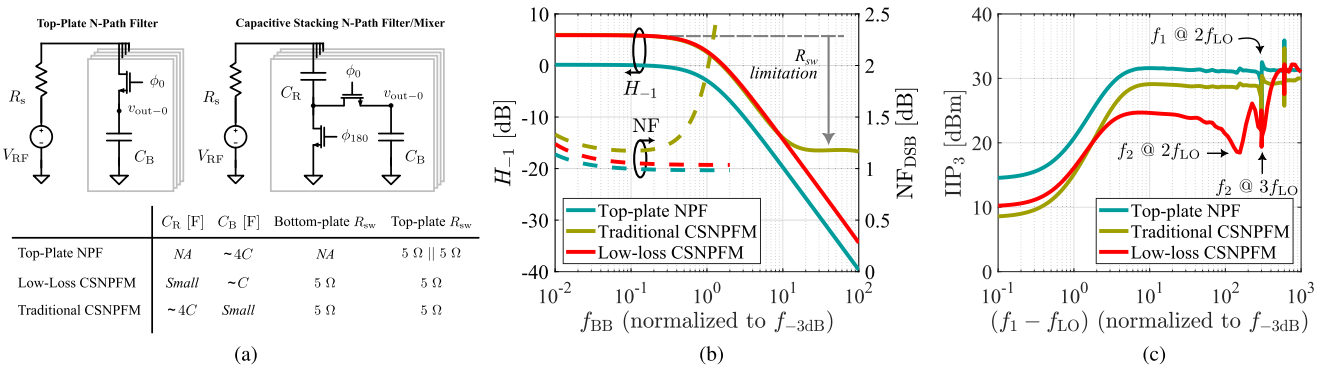

	C_R [F]	C_B [F]	Bottom-plate R_{sw}	Top-plate R_{sw}
Top-Plate NPF	*NA*	~$4C$	*NA*	5 Ω || 5 Ω
Low-Loss CSNPFM	*Small*	~C	5 Ω	5 Ω
Traditional CSNPFM	~$4C$	*Small*	5 Ω	5 Ω

(a) (b) (c)

Fig. 4. Comparison of the low-loss CSNPFM to a conventional top-plate NPF and the traditional CSNPFM [19]. (a) Topologies and component values used in simulation. Ideal and noiseless BB matching resistors were used (not shown). Switches have been implemented with 22-nm FDSOI models, and capacitors are ideal (the ˜ indicates that the actual capacitor values vary slightly to compensate for the impact of the switch resistance on the BW). Dynamic power and signal BW are constant across the three designs. (b) Simulation results for H_{-1} and DSB NF at $f_{LO} = 3$ GHz. (c) Small-signal linearity (IIP_3) simulation results at $f_{LO} = 3$ GHz.

later (ϕ_{180}), this average input is exactly opposite to the average that was applied to C_{R_1} during ϕ_0, see Fig. 3(a). Meanwhile, C_{B_1} samples the stacked combination of the C_R capacitors ($= v_{C_{R3}} - v_{C_{R1}}$), which yields 2× stacking gain. Fig. 3(a) also visualizes the circuit behavior during the first four periods.

Now, consider the case with $C_R \ll C_B$. The most important difference is that both paths present a roughly equal impedance [$\approx Z_{C_R} = 1/(sC_R)$] to the source, see Fig. 3(b). As a result, both C_R capacitors connected during a single clock phase will charge in unison when the CSNPFM is excited by the source. Again, we apply an input to the circuit with $f_{RF} = f_{LO}$. During ϕ_0, both C_R capacitors charge to the average applied input. Due to the series C_{B_3} capacitor, C_{R_3} is charged with a smaller current than C_{R_1}, namely $[(i/2)(1-\Delta)]$. The resulting voltage difference between the two C_R capacitors is stored on C_{B_3}.

As the switches close at the start of the opposite phase ϕ_{180}, the initially empty C_{B_1} capacitor connects. As a consequence, the difference in voltage on both C_R capacitors originating from the previous ϕ_0 cycle is partly canceled through charge sharing between C_{B_1}, C_{R_1}, and C_{R_3}. Then, during ϕ_{180}, both C_R capacitors charge in the opposite direction. This time, C_{R_1} charges with a slightly smaller current than C_{R_3} due to C_{B_1}, which samples the voltage difference between both C_R capacitors.

Fig. 3(b) also illustrates how this operation repeats during the first four periods. Although both C_R capacitors charge in unison, we see a net effect down on C_{R_3} during ϕ_0 due to the series C_{B_3} capacitor and a net effect up on C_{R_1} during ϕ_{180} due to C_{B_1}. The C_B capacitors sample the voltage difference between the C_R capacitors, resulting in a summation of these net effects, yielding 2× stacking gain. At the same time, the unison effect is effectively eliminated as it sums in anti-phase.

C. Impact on Performance

Let us take a step back and compare the front end performance of the low-loss CSNPFM to both the traditional CSNPFM and a regular top-plate NPF. Fig. 4(a) shows the two topologies and a table with the normalized component values in which C is the capacitance required to achieve a normalized BW f_{-3dB} in the low-loss CSNPFM. For ease of comparison, we have normalized this signal BW for all three designs. We have also normalized the required dynamic power, allowing for two switches in parallel for the top-plate NPF. Apart from the 22-nm fully depleted silicon-on-insulator (FDSOI) models we used for the switches (switch ON-resistance is approximately $R_{sw} = 5$ Ω, we provide a detailed design motivation for their sizing in Section IV), the components are ideal.

It can be seen in Fig. 4(a) that, compared to the other two designs, the low-loss CSNPFM requires a capacitor area that is approximately 4× smaller than both the other designs. We will confirm this result through analysis in Section III-B. Effectively this means that, for a normalized BW, a 4× smaller current is required to charge a single C_B capacitor in the low-loss design than would be required to charge either a single C_R capacitor in the traditional CSNPFM or a single C_B in a regular top-plate NPF. The two main effects that reduce the current can be explained using Fig. 3.

1) The total current supplied to the capacitors is determined by the voltage across the source resistor R_s, which depends on the applied signal (same for all three designs) and the voltage at the RF node. If we now focus on a single clock phase (such as ϕ_0), we see that, in contrast to the traditional CSNPFM and the top-plate NPF where the RF node simply tracks the RC step response, the voltage at the RF node charges much more rapidly due to the smaller C_R capacitors in the low-loss design. The result is a smaller voltage across R_s (especially at the end of the clock phase), reducing the total current.
2) In the low-loss design, this current splits over two branches, and hence, only roughly half of the total current is used to charge C_B. In the traditional CSNPFM and top-plate NPF, practically all current is used to charge the C_R and C_B capacitors, respectively.

Now, let us compare the performance of the designs in Fig. 4(a). Fig. 4(b) shows both the downconverted TF H_{-1} and the double sideband (DSB) NF. Though both CSNPFM designs achieve a stacking voltage gain of approximately 6 dB

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compared to the top-plate NPF, the selectivity of the traditional CSNPFM is limited by the switch resistance R_{sw}, which can be explained with the circuit insights of Section II-B. In the original CSNPFM, the voltage drop over the switch is effectively sampled on the C_{B} capacitor as interferer currents only flow through a single path. In the proposed circuit, interferer currents are divided equally over two paths, resulting in two roughly equal voltage drops over both switches that sum in anti-phase on the C_{B} capacitors.

Fig. 4(b) also plots $\mathrm{NF_{DSB}}$ for the three designs. Since, for constant dynamic power, R_{sw} in the top-plate NPF is $2\times$ lower, its NF is approximately 0.1 dB better than the low-loss CSNPFM. However, as the voltage gain is 6 dB lower, any subsequent block will be twice as critical to overall RX NF. Comparing both CSNPFM designs, it can be observed that the traditional CSNPFM suffers from an NF increase around the band edge due to the band-limiting input pole formed by R_{s} and C_{R} (as opposed to the relatively "wideband" $R_{\mathrm{s}}C_{\mathrm{R}}$-pole in the low-loss design), while the NF minima are roughly equal.

Fig. 4(c) shows small-signal linearity expressed in input-referred third-order intercept point ($\mathrm{IIP_3}$) for each of the three designs. Due to the larger in-band (IB) signal swings in both CSNPFM designs, the IB $\mathrm{IIP_3}$ is approximately 6 dB lower. Moving out-of-band (OOB), the $\mathrm{IIP_3}$ of the proposed low-loss CSNPFM is limited by a second system response centered around even harmonics that we discuss in more detail in Section III. However, we emphasize that the filter rejection limitation because of non-zero R_{sw} in the traditional CSNPFM will impose stricter linearity specifications for subsequent BB circuits as the OOB voltage swing will be larger than in the low-loss design. Depending on the BB circuitry, this could still result in a lower overall OOB $\mathrm{IIP_3}$ for the traditional CSNPFM over the low-loss design despite the better OOB $\mathrm{IIP_3}$ plotted in Fig. 4(c).

Compared to the traditional CSNPFM, the low-loss capacitive scaling technique is neutral for LO radiation effects. Furthermore, a small C_{R} results in a small parasitic capacitor C_{p}, which helps to reduce the frequency shift between the frequency at which the IB gain is maximum and f_{LO} [27]. It also reduces the shift in S_{11} minimum [6]. However, a downside of the smaller C_{R} is that the sampling region as defined by Soer et al. [26] extends to considerably higher LO frequencies than was the case in the traditional circuit, leading to an increase in noise due to folding effects at the lower side of the LO operating range. The required clearance from the sampling region puts an effective lower bound on the value of C_{R} and becomes an important part of the design strategy that we will introduce in Section III-B.

III. Eigenvalue-Based Analysis

In [19], a TF of the CSNPFM has been derived using the adjoint network (which allows for a relatively simple derivation of the impulse response of switched capacitor circuits [27], [28], [29]). Although the traditional CSNPFM in [19] is topologically identical to the low-loss CSNPFM presented in this article, the derived TF is not accurate for CSNPFM circuits where $C_{\mathrm{R}} \ll C_{\mathrm{B}}$ due to the omission of the modeling of charge sharing between the capacitors. In this section, we incorporate charge sharing and enhance the existing adjoint network-based TF analysis, leveraging a discrete-time state-space model and eigendecomposition to deal with the multiple system responses in low-loss CSNPFMs. We extract simplified design equations valid in the mixing region and finalize the section by formulating a design strategy.

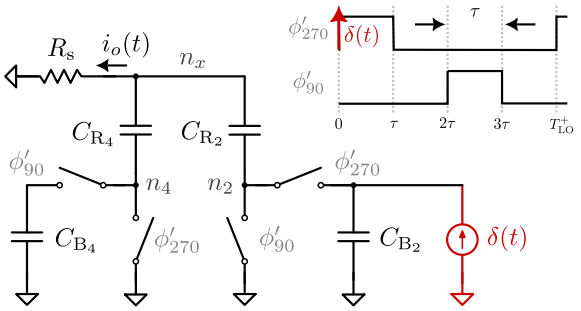

Fig. 5. Adjoint network of the quadrature-phase kernel of the CSNPFM.

A. TF Using the Adjoint Network

In this section, we will be deriving the equivalent TF $H_{\mathrm{eq}}(f)$, which is the sum of the harmonic TFs for a given input frequency f [28]. Our first step is to construct the adjoint network. The quadrature-phase kernel of the CSNPFM is our starting point. In its adjoint, we retain the passive components and reverse timing of the clock signals ($\phi \rightarrow \phi'$) [28], which means that ϕ'_{270} is the first clock phase to occur, see the inset of Fig. 5. Injecting a current Dirac pulse $\delta(t)$ at the sampling instance of the original output, we arrive at the circuit in Fig. 5. The impulse response $h_{\mathrm{eq}}(t)$ of the original circuit is equal to the output current $i_o(t)$ in Fig. 5 [28].

In three steps, we will formulate an expression for $i_o(t)$. First, we evaluate the circuit's operation step-by-step during the first full period T_{LO}. Next, we derive how this operation repeats, i.e., the circuit's periodicity. Finally, we combine the first period with the periodicity to arrive at the overall impulse response. The frequency-domain TF then follows from the Fourier transform of $i_o(t)$ [which is equal to $h_{\mathrm{eq}}(t)$].

Using a discrete-time signal-flow diagram, we evaluate the first period T_{LO} and keep track of the capacitor voltages at the switching moments, see Fig. 6(a). During each on-phase, three of the four capacitor voltages are independent; it suffices to model both C_{B} capacitors and the C_{R} capacitor in parallel to R_{s} during each on-phase (C_{R4} during ϕ'_{270} and C_{R2} during ϕ'_{90}). The other C_{R} capacitor is grayed out in Fig. 6(a).

Consider the situation at $t = 0^{+}$, as depicted in Fig. 6(b). An initial condition charge $\delta(t)$ pulse has been injected into the output node v_{CB2}, resulting in a voltage[2] on C_{B2} equal to $v_0 = 1/(C_{\mathrm{B}}+C_{\mathrm{R}}/2) = 1/C_0$. This voltage also appears across the series combination of C_{R2} and C_{R4}. Then, during ϕ'_{270}, the capacitors discharge through R_{s} with a time constant $R_{\mathrm{s}}C_{\mathrm{eq}}$, where $C_{\mathrm{eq}} = C_{\mathrm{R}}+C_{\mathrm{R}}C_{\mathrm{B}}/(C_{\mathrm{R}}+C_{\mathrm{B}})$. When the switches open at $t = \tau$, we find for v_{CR4} (which is equal to the voltage across

[2] 1 stands for 1 Coulomb, and hence, 1/C is actually a voltage.

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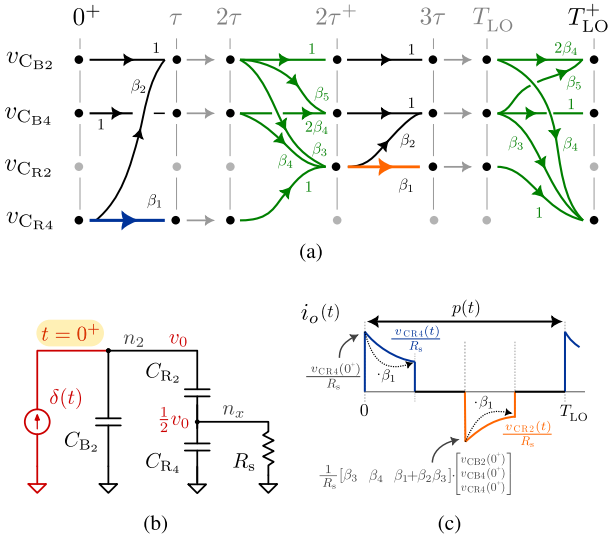

Fig. 6. Construction of the time-domain waveform of the first period of the output current $i_o(t)$. (a) Discrete-time signal-flow diagram of the capacitor voltages. (b) Overview of the capacitor voltages at $t = 0^+$, e.g., the starting values for the signal-flow graph. (c) Time-domain waveform of the first period of the output current $i_o(t)$.

C_{eq} during ϕ'_{270})

$$v_{\text{CR4}}(\tau) = v_{\text{CR4}}(0^+) \cdot \beta_1 \tag{1}$$

where $\beta_1 = \exp[-\tau/R_{\text{s}}C_{\text{eq}}]$. Using charge conservation for floating node n_2, we find for the voltage on C_{B2}

$$v_{\text{CB2}}(\tau) = v_{\text{CB2}}(0^+) + \beta_2 \cdot v_{\text{CR4}}(0^+) \tag{2}$$

where $\beta_2 = C_{\text{R}}/(C_{\text{R}} + C_{\text{B}}) \cdot (\beta_1 - 1)$. Then, during the off-phase between τ and 2τ, capacitor charge is conserved, and nothing changes. The signal-flow diagram in Fig. 6(a) summarizes these findings.

At $t = 2\tau$, the other set of switches closes (ϕ'_{90}), resulting in charge redistribution between the connected capacitors. Now, if $C_{\text{B}} \gg C_{\text{R}}$, a relatively large and initially empty capacitor C_{B4} is connected to the smaller C_{R} capacitors, leading to a significant change in the voltage across C_{R2} (and thus R_{s}). To capture this effect, we use charge conservation equations for the two floating nodes, n_{x} and n_4, and solve for the capacitor voltages. To simplify the analysis, we will assume that the charge sharing settles instantly (typically, the switch impedance is in the order of $R_{\text{s}}/10$). We find

$$\begin{bmatrix} v_{\text{CB4}}(2\tau^+) \\ v_{\text{CR2}}(2\tau^+) \end{bmatrix} = \begin{bmatrix} \beta_5 & 2\beta_4 & 0 \\ \beta_3 & \beta_4 & 1 \end{bmatrix} \begin{bmatrix} v_{\text{CB2}}(2\tau) \\ v_{\text{CB4}}(2\tau) \\ v_{\text{CR4}}(2\tau) \end{bmatrix} \tag{3}$$

where $\beta_3 = -(C_{\text{B}} + C_{\text{R}})/(2C_{\text{B}} + C_{\text{R}})$, $\beta_4 = C_{\text{B}}/(2C_{\text{B}} + C_{\text{R}})$, and $\beta_5 = -C_{\text{R}}/(2C_{\text{B}} + C_{\text{R}})$.

By virtue of topological symmetry, the circuit's behavior during ϕ'_{90} is similar to that during ϕ'_{270}. Therefore, if we interchange the "2" and "4" designators and update the timing, we find

$$\begin{bmatrix} v_{\text{CR2}}(3\tau) \\ v_{\text{CB4}}(3\tau) \end{bmatrix} = \begin{bmatrix} \beta_1 & 0 \\ \beta_2 & 1 \end{bmatrix} \begin{bmatrix} v_{\text{CR2}}(2\tau^+) \\ v_{\text{CB4}}(2\tau^+) \end{bmatrix}. \tag{4}$$

A similar strategy can be followed to model the charge sharing from $t = T_{\text{LO}}$ to $t = T_{\text{LO}}^+$, see Fig. 6(a).

We can now construct an expression for the first period of $i_o(t)$, which we will denote by $p(t)$. We do so by evaluating the current through R_{s}, which is non-zero only during ϕ'_{270} and ϕ'_{90} as the connected capacitors discharge through the resistor with time constant $R_{\text{s}}C_{\text{eq}}$. The starting values for these two discharge currents can be derived from the capacitor voltages at $t = 0^+$. During ϕ'_{270}, capacitor C_{R4} is in parallel with R_{s}, so the starting value $i_{R_{\text{s}}}(0^+)$ is $v_{\text{CR4}}(0^+)/R_{\text{s}}$, refer to Fig. 6(c). During ϕ'_{90}, C_{R2} is in parallel with R_{s}; thus, using the signal-flow graph, we can derive that the starting current for $t = 2\tau^+$ is a weighted combination of three initial capacitor voltages, refer to Fig. 6(a) and (c)

$$i_{R_{\text{s}}}(2\tau^+) = \frac{1}{R_{\text{s}}} \cdot \begin{bmatrix} \beta_3 & \beta_4 & \beta_1 + \beta_2\beta_3 \end{bmatrix} \cdot \begin{bmatrix} v_{\text{CB2}}(0^+) \\ v_{\text{CB4}}(0^+) \\ v_{\text{CR4}}(0^+) \end{bmatrix}. \tag{5}$$

Combining these starting values with the exponential discharge and subtracting a scaled and delayed version to set the current back to zero as the switches open, we obtain

$$\begin{aligned} p(t) = {} & i_{R_{\text{s}}}(0^+) \cdot (h(t) - \beta_1 \cdot h(t - \tau)) \\ & + i_{R_{\text{s}}}(2\tau^+) \cdot (h(t - 2\tau) - \beta_1 \cdot h(t - 3\tau)) \end{aligned} \tag{6}$$

where $h(t) = \exp[-t/R_{\text{s}}C_{\text{eq}}]u(t)$ and $u(t)$ is the Heaviside step function.

Now that we have an expression for the first period of $i_o(t)$, we will derive how it repeats. To this end, we leverage a discrete-time state-space representation of the capacitor voltages at multiples of T_{LO}^+. Note that this approach is different from the state-space approaches in prior art, which typically provide a continuous-time state-space representation of the complete circuit behavior and not merely its periodicity [29], [30]. The state vector $\boldsymbol{x}[kT_{\text{LO}}^+]$ is comprised of the capacitor voltages at the start of each period, as shown in Fig. 7(a). State matrix $\boldsymbol{A}$ describes how the circuit repeats

$$\begin{bmatrix} v_{\text{CB2}}[kT_{\text{LO}}^+] \\ v_{\text{CB4}}[kT_{\text{LO}}^+] \\ v_{\text{CR4}}[kT_{\text{LO}}^+] \end{bmatrix} = \boldsymbol{A} \cdot \begin{bmatrix} v_{\text{CB2}}[(k-1)T_{\text{LO}}^+] \\ v_{\text{CB4}}[(k-1)T_{\text{LO}}^+] \\ v_{\text{CR4}}[(k-1)T_{\text{LO}}^+] \end{bmatrix}. \tag{7}$$

Matrix $\boldsymbol{A}$ can be constructed using the signal-flow diagram in Fig. 6(a). An expression for the capacitor voltages at the start of each period ($t = kT_{\text{LO}}^+$) can be found by considering the initial capacitor voltages at $t = 0^+$ shown in Fig. 6(b), captured in column vector $\boldsymbol{B}$

$$\boldsymbol{x}[kT_{\text{LO}}^+] = \boldsymbol{A} \cdot \boldsymbol{x}[(k-1)T_{\text{LO}}^+] + \boldsymbol{B} = \boldsymbol{A}^k \cdot \boldsymbol{B}. \tag{8}$$

The starting value for the discharge current of the second period ($v_{\text{CR4}}(T_{\text{LO}}^+)/R_{\text{s}}$) follows from $\boldsymbol{A}$. Unfortunately, due to charge sharing, this new value is not a scaled version of its previous value, but a weighted combination of the capacitor voltages from the previous cycle. This means that $\boldsymbol{A}$ is not diagonal, and as a result, a closed-form expression of $\boldsymbol{A}^k$ becomes problematic. However, through eigendecomposition, we can decompose the periodicity captured in $\boldsymbol{A}$ into multiple separate exponential factors called the eigenvalues, greatly simplifying the transition to a closed-form expression of the TF. In addition, the eigenvalues of $\boldsymbol{A}$ directly relate to the poles of the CSNPFM, which we will leverage to extract expressions

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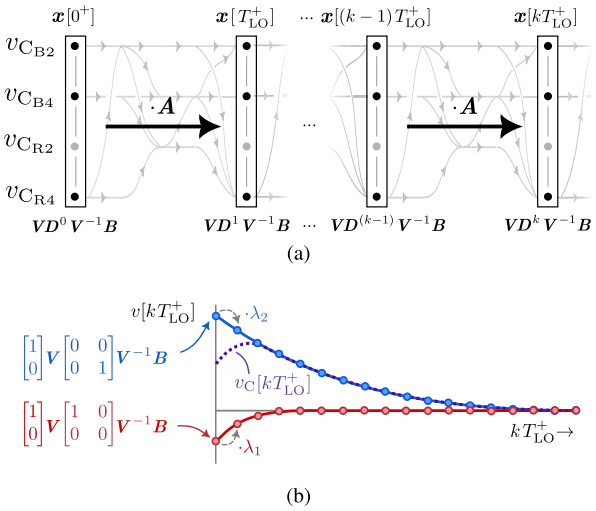

Fig. 7. Discrete state-space description models the periodicity of the adjoint network. (a) Relation between the state-space parameters and the signal-flow graph quantities. (b) Example decomposition of the first state variable (capacitor voltage) in a fictional 2×2 system.

for the BW later. Performing eigendecomposition on matrix $\boldsymbol{A}$, we find

$$\boldsymbol{x}[kT_{\mathrm{LO}}^+] = \boldsymbol{A}^k \cdot \boldsymbol{B} = \boldsymbol{V}\boldsymbol{D}^k\boldsymbol{V}^{-1} \cdot \boldsymbol{B} \tag{9}$$

in which $\boldsymbol{V}$ is the matrix containing the eigenvectors of $\boldsymbol{A}$ and $\boldsymbol{D}$ is the matrix containing the corresponding eigenvalues $\lambda_i = \boldsymbol{D}(i,i)$. Note that matrix $\boldsymbol{D}$ is diagonal.

Let us conceptualize the result in (9) using Fig. 7(b). The entries of $\boldsymbol{x}$, e.g., the capacitor voltages, now comprise a weighted combination of separate responses progressing exponentially through time with λ_i^k. The weights of these responses are captured in the combination of the eigenvector matrix $\boldsymbol{V}$ and the starting values $\boldsymbol{B}$. As an example, let us expand a 2×2 system and take the first entry in the state vector

$$\begin{aligned} x_1[kT_{\mathrm{LO}}^+] = {} & \lambda_1^k \cdot v_{11}(v_{i11}b_1 + v_{i12}b_2) \\ & + \lambda_2^k \cdot v_{12}(v_{i21}b_1 + v_{i22}b_2). \end{aligned} \tag{10}$$

Similarly, we will decompose the repetition of $p(t)$ along the eigenvalues of $\boldsymbol{A}$. Each of the capacitor voltages constituting the starting values of the discharge currents in (6) is replaced by the corresponding element of $\boldsymbol{x}[0^+]$ in (9). After substitution, we group all terms corresponding to each eigenvalue, effectively factoring $p(t)$ in its eigenvalues λ_i^0

$$p(t) = \lambda_1^0 \cdot p_1(t) + \lambda_2^0 \cdot p_2(t) + \cdots \tag{11}$$

in which the $p_i(t)$ functions are a combination of (the elements of) $\boldsymbol{V}$, $\boldsymbol{B}$, $h(t)$, and the circuit/signal-flow graph elements. Every next cycle, each $p_i(t)$ term is simply scaled with λ_i. Now, we combine $p(t)$ with the CSNPFM periodicity. Hence, to derive the impulse response of the circuit, $h_{\mathrm{eq}}(t)$, we leverage the decomposition of $p(t)$ along the eigenvalues as follows:

$$h_{\mathrm{eqi}}(t) = p_i(t) + \lambda_i h_{\mathrm{eqi}}(t - T_{\mathrm{LO}}). \tag{12}$$

The combined impulse response $h_{\mathrm{eq}}(t)$ is the sum of the individual system responses $[h_{\mathrm{eq}}(t) = \sum h_{\mathrm{eqi}}(t)]$. Applying the Fourier transform to (12), we find

$$H_{\mathrm{eqi}}(f) = P_i(f) + \lambda_i \cdot H_{\mathrm{eqi}}(f) \cdot e^{-j2\pi f T_{\mathrm{LO}}}. \tag{13}$$

Thus, the equivalent TF $H_{\mathrm{eq}}(f)$ becomes

$$H_{\mathrm{eq}}(f) = \sum H_{\mathrm{eqi}}(f) = \sum \frac{P_i(f)}{1 - \lambda_i e^{-j2\pi f T_{\mathrm{LO}}}}. \tag{14}$$

Let us apply this procedure to evaluate the TF of the CSNPFM. We do so twice: first revisiting the traditional CSNPFM in [19] (where $C_{\mathrm{R}} \gg C_{\mathrm{B}}$) and then considering the low-loss CSNPFM as presented in this article (where $C_{\mathrm{R}} \ll C_{\mathrm{B}}$). Treating both cases separately allows for a direct comparison while offering significant simplification of the algebra involved by using a simplified matrix $\boldsymbol{A}$, increasing insight into the results.

1) Traditional CSNPFM ($C_{\mathrm{R}} \gg C_{\mathrm{B}}$): We derive state matrix $\boldsymbol{A}$ using the signal-flow diagram in Fig. 6(a). We simplify the beta-factors that model charge sharing between the capacitors (β_3 through β_5) to -1, 0, and -1, respectively, by leveraging $C_{\mathrm{R}} \gg C_{\mathrm{B}}$ (i.e., taking the limit $C_{\mathrm{B}}/C_{\mathrm{R}} \rightarrow 0$). Note that we leave β_1 intact, as it directly models the discharge and, thus, the current through R_{s}. In addition, β_2 can be simplified to $(\beta_1 - 1)$. We find

$$\lim_{(C_{\mathrm{B}}/C_{\mathrm{R}}) \rightarrow 0} \boldsymbol{A} = \begin{bmatrix} \beta_1 & 0 & 0 \\ -\beta_1 & 0 & 0 \\ 0 & 0 & \beta_1 \end{bmatrix}. \tag{15}$$

Performing eigendecomposition yields

$$\boldsymbol{V} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad \boldsymbol{D} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \beta_1 & 0 \\ 0 & 0 & \beta_1 \end{bmatrix}. \tag{16}$$

Evaluating (11) and (14) using the result in (16), we find

$$\begin{aligned} P(f) \approx {} & \frac{C_{\mathrm{eq}}}{2C_0} \cdot \frac{1}{1 + j2\pi f R_{\mathrm{s}} C_{\mathrm{eq}}} \\ & \cdot \left[\left(1 - \beta_1 e^{-j2\pi f \tau}\right) - \left(e^{-j2\pi f 2\tau} - \beta_1 e^{-j2\pi f 3\tau}\right) \right] \end{aligned} \tag{17a}$$

$$H_{\mathrm{eq}}(f) = \frac{P(f)}{1 - \beta_1 e^{-j2\pi f T_{\mathrm{LO}}}}. \tag{17b}$$

The TF in (17) conforms to the result found by Purushothaman et al. [19] if we recognize that, in their publication, $\beta_2 \approx 1$ for $C_{\mathrm{R}} \gg C_{\mathrm{B}}$.

2) Low-Loss CSNPFM ($C_{\mathrm{R}} \ll C_{\mathrm{B}}$): The operation of the adjoint network of the low-loss CSNPFM relies on charge sharing, leading to more involved algebra due to the multiple system responses. Again, we simplify β_3 through β_5 in matrix $\boldsymbol{A}$. We find $-\frac{1}{2}$, $\frac{1}{2}$, and 0 by taking the limit $C_{\mathrm{B}}/C_{\mathrm{R}} \rightarrow \infty$. We leave both β_1 and β_2 intact this time to avoid over-simplification (β_2 describes the impact of $v_{C_{\mathrm{R}}}$ on $v_{C_{\mathrm{B}}}$, see Fig. 6(a), which is important for determining an accurate BW expression). After performing eigendecomposition on matrix $\boldsymbol{A}$, we leverage that $C_{\mathrm{R}} \ll C_{\mathrm{B}}$ and use the binomial approximation to eliminate the square root in the resulting

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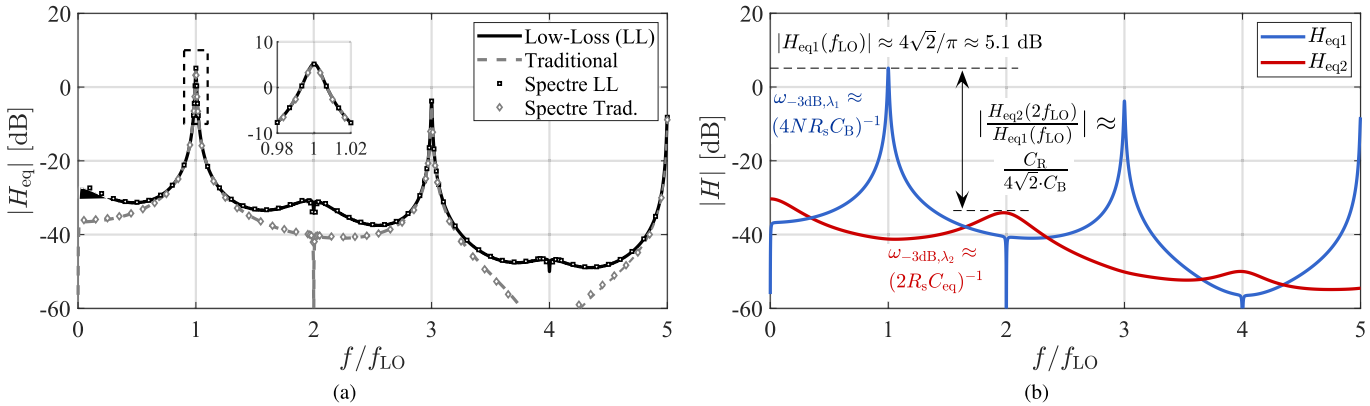

Fig. 8. Analysis results for the low-loss CSNPFM with C_R = 2 pF, C_B = 20 pF, and f_{LO} = 2 GHz. (a) Analytical versus Spectre comparison of the traditional CSNPFM in [19] (with C_R = 80 pF and C_B = 2 pF) and the low-loss CSNPFM. (b) Decomposition of the TF in the terms corresponding to each eigenvalue with simplified design equations for the mixing region annotated.

expressions. Evaluating (11) and (14) using these results yields

$$\begin{bmatrix} P_1(f) \\ P_2(f) \end{bmatrix} \approx \frac{C_{eq}}{2C_0} \cdot \frac{(\beta_1+1)^{-1}}{1+j2\pi f R_s C_{eq}} \cdot \left(\begin{bmatrix} 1 \\ \beta_1 \end{bmatrix} (1-\beta_1 e^{-j2\pi f\tau}) + \begin{bmatrix} -1 \\ \beta_1^2 \end{bmatrix} (e^{-j2\pi f 2\tau} - \beta_1 e^{-j2\pi f 3\tau}) \right) \quad (18a)$$

$$\begin{bmatrix} \lambda_1 \\ \lambda_2 \end{bmatrix} \approx \begin{bmatrix} 1+\beta_2/(\beta_1+1) \\ \beta_1 \cdot [\beta_1+\beta_2/(\beta_1+1)] \end{bmatrix} \quad (18b)$$

$$H_{eq}(f) = \frac{P_1(f)}{1-\lambda_1 e^{-j2\pi f T_{LO}}} + \frac{P_2(f)}{1-\lambda_2 e^{-j2\pi f T_{LO}}}. \quad (18c)$$

Note that the TF in (18c) contains two system responses, as described by the eigenvalues in (18b).

Fig. 8(a) compares the TFs in (17) and (18) to Spectre simulation results for some typical component values, and good agreement can be seen. The traditional and low-loss CSNPFM TFs show strong similarity; the two major differences are that: 1) the traditional CSNPFM needs a 4× larger C_R capacitor to achieve the same BW and 2) the low-loss implementation has worse OOB rejection around even harmonics. We will later show that this even response can be eliminated by reading out the circuit differentially.

As we have decomposed the TF of the low-loss CSNPFM in its system responses, we can evaluate those separately and gain additional insights. Fig. 8(b) shows that the fundamental CSNPFM response and the other odd harmonics are almost solely dictated by λ_1. The second system response (λ_2) gives rise to additional responses at even harmonics.

B. Simplified Design Equations Low-Loss CSNPFM

The result in (18) is valid for both the mixing and the sampling region and therefore still quite general. The boundary between these regions is determined by the effective ON-time of the switches and the RC time of the pole as seen by the RF input [26], which in this case is R_sC_{eq}. By constraining the use of the low-loss CSNPFM to the mixing region ($f_{LO} \gg (2NR_sC_{eq})^{-1}$, resulting in high-$Q$ filtering), we derive a set of simplified design equations of key performance characteristics. It is important to note that the circuit as analyzed in this section, in line with prior work on adjoint network analysis [19], [28], does not contain a matching network. As practical CSNPFMs are typically matched through a set of BB impedances (e.g., a resistor in parallel with the C_B capacitors), we discuss the impact of including such a matching network on the design equations in Section III-C.

1) Gain of the Fundamental Response: The effective stacking gain of the low-loss CSNPFM can be determined by evaluating the magnitude of H_{eq1} in (18) at f_{LO}. Since we are considering the mixing region, we can accurately approximate β_1 by the first two terms in its Maclaurin series: $\beta_1 = \exp[-\tau/(R_sC_{eq})] \approx 1-\tau/(R_sC_{eq})$. Using $C_R \ll C_B$ for simplifications, we find

$$|H_{eq1}(f_{LO})| \approx 4\sqrt{2}/\pi \approx 5.1 \text{ dB}. \quad (19)$$

2) BW of Odd (λ_1) Responses: The −3-dB BW (the distance between f_{LO} and the frequency at which the response is 3 dB lower, e.g., the BB BW, when considering the downconverted output frequencies) of the fundamental and the other odd responses is determined by λ_1. Recognizing that $\exp[-sT_{LO}] = z^{-1}$ in the denominators of (18c), we find a pole in the z-domain $p_{z1} = \lambda_1$. Through a simple forward Euler transform, we can evaluate this pole in the s-domain: $p_{s1} = f_{LO}(p_{z1}-1)$. Using similar simplifications as in deriving the gain, we find for the BW of the odd responses ($\omega_{-3\text{ dB},\lambda_1}$)

$$\omega_{-3\text{ dB},\lambda_1} \approx (4NR_sC_B)^{-1}. \quad (20)$$

Compared to the traditional CSNPFM where the BW of the response is evaluated to $\omega_{-3\text{ dB}} \approx (NR_sC_R)^{-1}$, the low-loss implementation requires a 4× smaller capacitance.

3) BW of Even (λ_2) Responses: In a similar fashion as for the λ_1 responses, we can evaluate the BW of the even (λ_2) responses as

$$\omega_{-3\text{ dB},\lambda_2} \approx (2R_sC_{eq})^{-1}. \quad (21)$$

4) Relative Strength of λ_2 Response: As discussed in Section II, the even system responses limit the low-loss CSNPFM OOB rejection and therefore linearity and are thus

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undesired. The relative strength of the second harmonic with respect to the fundamental can be approximated as

$$|H_{\text{eq2}}(2f_{\text{LO}})/H_{\text{eq1}}(f_{\text{LO}})| \approx C_{\text{R}}/(4\sqrt{2}\cdot C_{\text{B}}). \tag{22}$$

The result in (22) shows that, for a given BW of the fundamental response (determined by C_{B}), the clearance of the second harmonic with respect to the fundamental can be maximized by minimizing C_{R}.

The complete set of simplified design equations has been annotated in Fig. 8(b) and verified through Spectre simulations. These show that they are already accurate within 20% (2 dB) at $C_{\text{B}} > 3C_{\text{R}}$ and $f_{\text{LO}} > 3(2NR_{\text{s}}C_{\text{eq}})^{-1}$ and accurate within 10% (1 dB) at over 4×.

C. Impact of BB Matching on the Design Equations

The result in (18) is the TF from the RF source in Fig. 1 to one of the BB capacitors (without matching network). In measurements, one typically assumes a matched RF input and refers the gain at the BB outputs to this RF node. To provide matching, practical CSNPFMs rely on a set of BB resistors (R_{B}) in parallel to the BB capacitors. These resistors lower the effective impedance seen at the RF node to 50 Ω [practically absorbing the 0.9-dB harmonic loss in (19)]. As the effective resistance at BB decreases due to the parallel R_{B} resistors, the BW increases. Hence, in a low-loss CSNPFM with BB matching resistors, (20) updates to $\omega_{-3\text{ dB},\lambda_1} \approx ([(4NR_{\text{s}})\|R_{\text{B}}]C_{\text{B}})^{-1}$.

It is important to note that, when using BB resistors for matching in the low-loss CSNPFM, the input is properly matched only for the odd system responses (λ_1) where the parallel BB resistors drain part of the source current used to charge the C_{B} capacitors. In contrast, around even harmonics (the λ_2 response), the RF capacitors instead of the BB capacitors track the downconverted RF signal (Fig. 3 shows how, instead of seeing the opposite phase of the input signal during ϕ_0 and ϕ_{180}, the RF capacitors see the same part of the signal every cycle), effectively shielding the impact of the BB resistors from the RF source as any current through the matching resistors also contributes to charging the series C_{R}. This observation has several consequences. First, the second system response in the low-loss CSNPFM is not matched and will see approximately double the voltage gain. Second, as a result, the clearance of the second harmonic with respect to the fundamental response given by (22) will be roughly 2× smaller. Third, since matching has no impact on the input pole formed by $R_{\text{s}}C_{\text{eq}}$, the boundary between the sampling and mixing regions is not affected.

D. TF for the Differential Output

The TF in (18) describes the transfer from the RF input to a single C_{B} capacitor. Alternatively, the output can be differentially obtained using two anti-phase C_{B} capacitor voltages. The state matrix $\boldsymbol{A}$ derived before is agnostic to the output (and input) connection and can directly be applied to derive a TF to a differential readout of two capacitor voltages of opposing phase. Only vector $\boldsymbol{B}$ has to be updated to include a negative $\delta(t)$ pulse injected into C_{B4}. Fig. 9 compares the analytical differential output TF to Spectre simulations. Compared to the single-ended case in Fig. 8(b), the gain of the fundamental increases by 6 dB, while the even responses have effectively been eliminated, as the first and second system responses have equal magnitude and sum in anti-phase at the even harmonics.

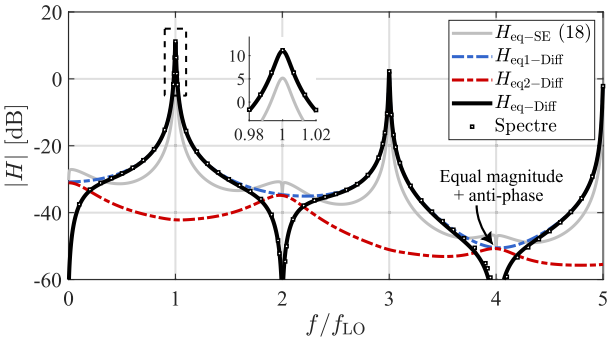

Fig. 9. TF to a differential readout of two outputs of opposing phase of the low-loss CSNPFM ($H_{\text{eq-Diff}}$) with C_{R} = 2 pF, C_{B} = 20 pF, and f_{LO} = 2 GHz. The TF to a single capacitor [see (18)] has been added for reference.

E. Integration of HR Techniques

Though reading out the circuit differentially eliminates the even harmonics, a strong response at $3f_{\text{LO}}$ (and $5f_{\text{LO}}$, $7f_{\text{LO}}$, and so on) remains. This response can be suppressed by extending the circuit to eight paths and applying HR techniques at the BB outputs [31]. When extending the circuit to $N = 8$, both the total C_{B} and C_{R} capacitances remain constant. The former becomes clear from evaluating (20); doubling N results in 2× smaller C_{B}, but the total number of capacitors doubles. The latter is related to the clearance to the sampling region, e.g., $C_{\text{R}} \gg (4NR_{\text{s}}f_{\text{LO-min}})^{-1}$. With $N = 8$, the switch ON-time halves, and thus, C_{R} can be twice as small, though the total number of capacitors doubles. Since also the total number of switches doubles and switch parasitics constitute a significant part of the total parasitic capacitance at the RF node (see Section IV), the total loss due to parasitic capacitance will increase. In contrast, harmonic loss will be lower in an eight-phase design.

The downside of applying HR at BB is that the BB circuitry still suffers from harmonic blockers. Recently, capacitor stacking has been used to integrate HR directly into the mixer-first receiver front end [23], [32], before any active circuitry. For instance, the work in [32] relies on an appropriate capacitor ratio and a combination of charge sharing and capacitor stacking to implement HR, but this comes at the cost of a lower maximum voltage gain compared to the low-loss CSNPFM. Weinreich and Murmann [23] proposed an N-path 1:4 "transformixer," which, when combined with an appropriate mixing sequence, provides HR before any active blocks. The low-loss CSNPFM as presented in this work, including the C_{R}-scaling technique, can readily be extended to the topology in [23] at the cost of increased parasitic capacitance due to the doubling of both the number of RF capacitors and switches in each kernel. Depending on the application, the designer should find the optimal tradeoff between increased parasitic capacitance in capacitive stacking

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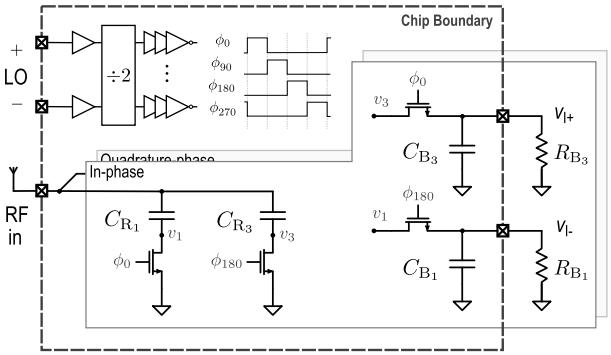

Fig. 10. Chip overview of the implemented low-loss CSNPFM. The switch ON-resistance, R_{sw}, is 5 Ω. A clocking network generates the four clock phases. Off-chip BB resistors provide RF port input matching.

HR techniques, and the increased vulnerability of BB circuitry to harmonic blockers in the case of HR at BB.

F. Low-Loss CSNPFM Design Procedure

We finalize this section by formulating a low-loss CSNPFM design procedure. Minimizing C_R reduces parasitic losses and maximizes OOB rejection for a given BW and is, therefore, the first objective. Since the CSNPFM needs to operate in the mixing region to avoid an NF penalty due to noise folding [26], there is a lower limit to the C_R value dictated by sufficient clearance from the sampling region. The exact value of this lower limit is application-dependent and determined by the tradeoff between lower parasitic losses and a higher NF at lower LO frequencies. The second step is to set C_B to achieve the desired BW. The following conditions hold.

1) Minimize the C_R capacitor. The lower limit is defined by sufficient clearance from the sampling region, e.g., $C_R \gg (4NR_s f_{LO\text{-}min})^{-1}$.
2) Set the desired BW of the fundamental response by choosing $C_B = (4NR_s\omega_{-3\ dB})^{-1}$, or, in case of a design with BB matching resistors: $C_B = ([(4NR_s)\|R_B]\omega_{-3\ dB})^{-1}$.

IV. Implementation and Measurement Results

In this section, we describe a proof-of-concept implemented in the 22-nm FDSOI CMOS process from GlobalFoundries and provide the measurement results of the low-loss CSNPFM. We will also verify the analysis results.

A. Implementation Details

Fig. 10 shows the chip overview of the low-loss CSNPFM. Input matching at the RF port for lower f_{LO} frequencies is predominantly provided by off-chip BB resistors R_B [33]. Since the BB resistors are transformed to the RF node with the same impedance transformation factor as the C_B capacitors [e.g., $4N\times$, refer to (20)], one would need approximately 800 Ω for an effective 50 Ω. However, the harmonic loss of the CSNPFM can be modeled as a parallel shunt impedance, which, according to simulations, is approximately 160 Ω and has to be absorbed into the matching resistors by making them bigger. Therefore, for a 50-Ω match at f_{LO}, larger 1.1-kΩ BB resistors are required. In addition, the minimum in $|S_{11}|$ is slightly offset from f_{LO}, i.e., a conjugate match is achieved at a frequency lower than f_{LO}. In our design, we have dimensioned R_B for the lowest $|S_{11}|$, effectively realizing a 50-Ω input impedance at the frequency where $|S_{11}|$ is minimum, requiring slightly larger 1.5-kΩ resistors. As a consequence of this design choice, the voltage gain at f_{LO} will be 0.9 dB higher than in the case of an ideal 50-Ω match at f_{LO}.

Next, using the design procedure in Section III-F, we set out to design a 10-MHz BB BW low-loss CSNPFM operating from 1 to 10 GHz. We choose a factor 1.5 clearance from the sampling region at 1 GHz, yielding a (rounded) C_R value of 2 pF. Then, according to the design equation under a matched condition, C_B needs to be approximately 30 pF to achieve a BB BW of 10 MHz with $R_B = 1.5$ kΩ. In the actual implementation, we absorb the parasitic capacitance due to the C_B capacitor, the bondpad, the printed circuit board, and the differential probe used in measurements into the design. Hence, we choose a smaller value for C_B of 16 pF. Together with roughly 6-pF probe capacitance and a combined 8-pF parasitic capacitance due to the PCB trace, the bondpad, and the electrostatic discharge protection network, the BB capacitance totals to 30 pF.

In addition to minimizing the C_R capacitors, the parasitic capacitance for a certain C_R capacitance is minimized through careful implementation. By making the substrate high resistive underneath the capacitors, exclusively using metal layers 4 up to and including 7, and using the type with the lowest voltage rating to achieve the highest capacitance density, the total parasitic capacitance is limited to 1% with respect to C_R.

The RF input trace is strategically positioned directly above the C_R capacitors. This avoids undesired parasitic capacitive coupling from the RF trace to the substrate while slightly increasing the desired C_R due to coupling from the RF trace to the C_R capacitors.

When large switches with low R_{sw} are used, the NF increases as the loss caused by switch parasitics becomes more dominant. Conversely, when small switches with high R_{sw} are employed, the NF increases as the switch thermal noise becomes dominant. In this design, the switches are sized such that, in the case of no input matching, the NF is minimized at an f_{LO} frequency of 6 GHz, roughly the center of the tuning range, resulting in regular V_{TH} switches with a switch ON-resistance of 5 Ω.

Given the aforementioned component values, C_p is estimated with a parasitic extraction simulation to be 395 fF. Fig. 11 features a bar graph illustrating the contribution of each element to C_p. In the traditional CSNPFM, the dominant C_p contribution are the C_R capacitors. However, in the low-loss CSNPFM, the switches contribute most to C_p.

The passive matching through R_B resistors results in an NF penalty of approximately 3 dB. As f_{LO} increases with fixed R_B resistors, the increasing parasitic capacitive loss would add to the NF and result in a lower gain. By exploiting this loss as part of the RF input matching, we can avoid an additional 3-dB NF penalty due to the parasitic capacitive losses. Therefore, we use higher values for R_B as f_{LO} increases, resulting in good matching characteristics across the entire LO frequency

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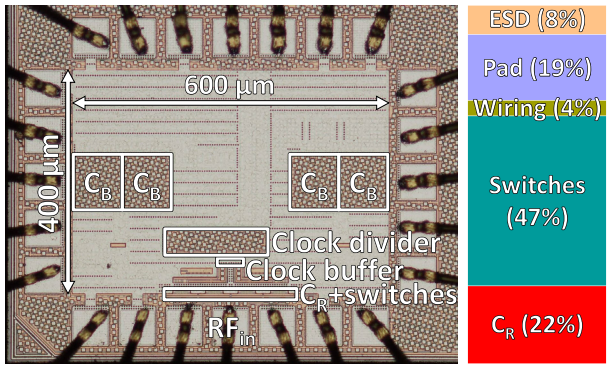

Fig. 11. Die micrograph and parasitic capacitance. The active area is 0.05 mm^2. The bar graph shows the breakdown of the parasitic capacitance at the RF node (C_p).

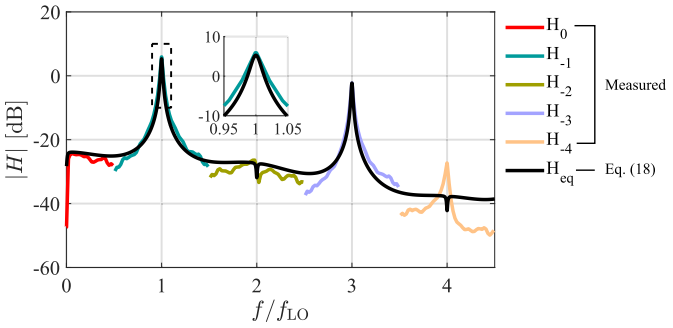

Fig. 12. Verification of the TF in (18) at f_{LO} of 1 GHz through measurements of the harmonic TFs to a single-ended output that yield an output component at BB.

range, allowing for a meaningful comparison to other works. We use three different R_B values for different frequency ranges: 1.5 kΩ for 1–4 GHz, 3.9 kΩ for 5–7 GHz, and 20 kΩ for 8–10 GHz.

The clock divider and phase generation in this design are similar to the topology used by Soer et al. [34]. The output stage of the clock divider has been skewed so that over process corners, an acceptable overlap at 10 GHz is achieved. Four clock buffers, one for each clock phase, are used. Each clock buffer is driving two N-path switches with 0.9-V gate swing. The clock buffer consists of three cascaded inverters scaled with a fan-out factor of 2, which have been optimized for acceptable rise and fall times at f_{LO} of 10 GHz. Pushing beyond 10 GHz will require much steeper edges and considerably increase the dynamic power consumption.

Fig. 11 shows the die micrograph, including markers indicating the block positions and relative size. These blocks represent the "active area" of 0.05 mm^2 for the prototype. The power breakdown of the prototype is given as follows. The clock divider and phase generation consume 1.8 mW/GHz, and the clock buffer driving the N-path switches consumes 1.3 mW/GHz. Consequently, the total power consumption is 3.1 mW/GHz at 0.9 V with negligible static power.

B. Analysis Verification

Using the implemented low-loss CSNPFM prototype, we set out to verify the analysis results in Section III, specifically the set of design equations and the TF in (18). The latter expresses $H_{eq}(f)$ as the sum of all harmonic TFs given an input frequency f: $H_{eq}(f) = \sum_k H_k(f)$ [28]. Note that k indicates a frequency shift, i.e., $f_{out} = f + k \cdot f_{LO}$. As we are considering a downconversion mixer here, we focus especially on H_{-1} and other harmonic TFs that yield an output component at BB. Also, for a correct comparison between the matched circuit in measurements and the unmatched circuit used in the analysis, the C_B value used in evaluation of (18) is set to 20 pF (the value needed for 10-MHz BB BW). In addition, following the discussion in Section III-C, the second system response, H_{eq2} (separately shown in Fig. 8b), is made twice as strong in (18).

Fig. 12 compares the analytical response for $H_{eq}(f)$ to the measured harmonic TFs for a single-ended output that yield an output component at BB: $H_0(f)$ through $H_{-4}(f)$. Except for the spur at $4f_{LO}$ due to non-ideal clock phases, (simulations indicate the spur strength corresponds to approximately 2% phase mismatch between two opposite phases), the agreement between analysis and measurements is within 5 dB up to at least $f = 4f_{LO}$. The inset in Fig. 12 shows that the measured gain is equal to 5.8 dB, whereas (19) predicted 5.1 dB. The measured channel BW of the fundamental is 20 MHz as was designed using the design procedure. The measured relative strength of H_{-2} just next to $2f_{LO}$ with respect to $H_{-1}(f_{LO})$ is −29 dB, equal to what (22) evaluates to after matching correction.

C. Gain, S_{11}, and NF

Fig. 13(a) shows $|S_{C21}|$, $|S_{11}|$, and NF results over the full 1–10 GHz frequency range. Matching has been realized through off-chip BB resistors in the three distinct ranges as discussed above. $|S_{11}|$ is < -10 dB across the LO range. As shown in Fig. 13(b), the gain at 10 GHz is only 1.4 dB lower with respect to the 11-dB gain at 1 GHz, due to the minimal parasitic RF capacitance. Around 10 GHz, the losses due to parasitic capacitance are too large to absorb using the matching resistors, resulting in a relatively poor match with a measured $|S_{11}|$ minimum of −10 dB. Hence, to improve the matching at high frequencies, the loss must be lowered further, for instance, by using smaller switches. Fig. 13(c) shows the $|S_{C21}|$ response at 3 GHz with the output frequency on the x-axis. A BB BW of 10 MHz has been achieved by an appropriate choice of C_B. Beyond the band edge, first-order filtering can be seen up to the 500-MHz BW of the differential probe used in measurements.

As the circuit output noise is about 4 nV/$\sqrt{\text{Hz}}$, the input-referred noise of the measurement setup dominates at the circuit output. Therefore, NF measurements make use of the cross correlation functionality of the Rohde & Schwarz FSWP50, to measure noise performance accurately. Fig. 13(a) shows that the NF varies between 4.7 and 7.0 dB across the LO range. This can be improved by avoiding purely passive resistive matching, see Section IV-E. Since the matching has been done in three distinct ranges, but the losses increase gradually with increasing f_{LO}, the NF curves in Fig. 13(a) have a characteristic shape where the NF increases slightly within a single matching range. At the transitions from 1.5 to 3.9 kΩ

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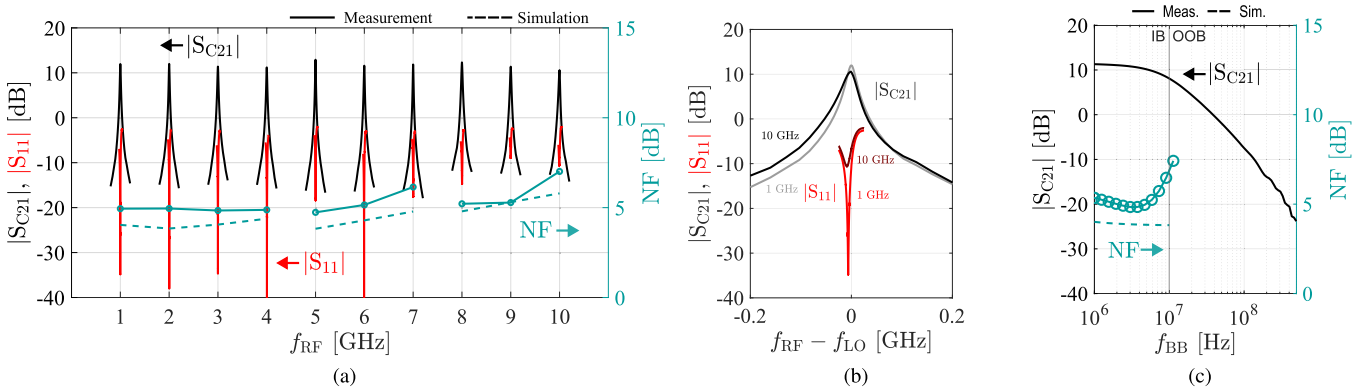

Fig. 13. (a) Measured $|S_{C21}|$, $|S_{11}|$, and NF versus input frequency over the full RF range (LO frequency has been swept in steps of 1 GHz). (b) Measured $|S_{C21}|$ and $|S_{11}|$ at 1 and 10 GHz, zoomed. (c) Measured $|S_{C21}|$ and NF versus output frequency at $f_{LO} = 3$ GHz.

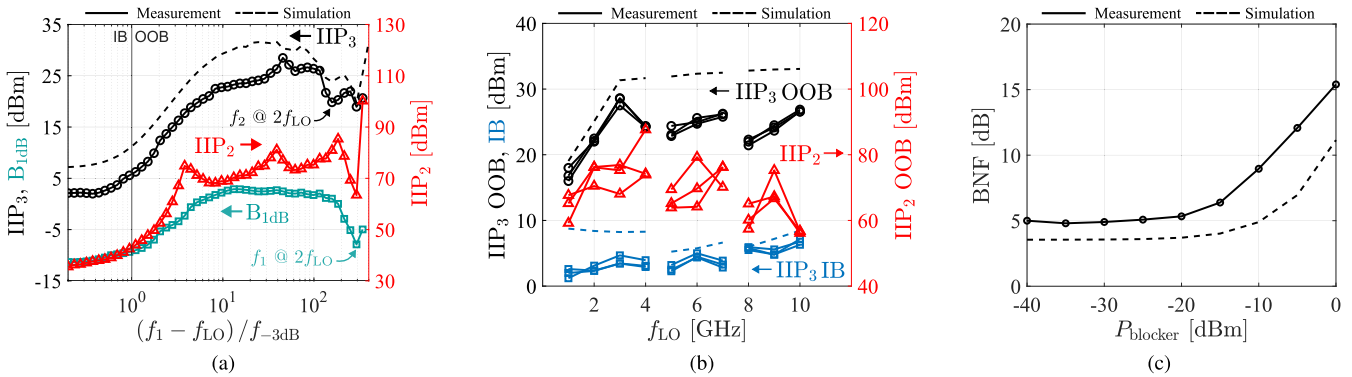

Fig. 14. (a) Measured IIP_2, IIP_3, and B1dB versus offset frequency of the first tone normalized to the BB BW at f_{LO} of 3 GHz. (b) OOB IIP_3 and IIP_2 measurements of three samples with the first tone at 50 BWs' offset (except for the 1-GHz OOB IIP_3 measurement, which has been measured at an offset of 10 BWs to avoid f_2 coinciding with $2f_{LO}$) and IB IIP_3 measurements with the first tone at 0.5 BWs' offset versus RF frequency. (c) Blocker NF versus blocker power of two samples with a blocker at an offset of 20 BWs at f_{LO} of 1.4 GHz.

and from 3.9 to 20 kΩ, the NF improves due to the increased compensation of the parasitic capacitive losses through the matching network as R_B is increased. Fig. 13(c) shows the BB NF curve for f_{LO} of 3 GHz, and LO-RF coupling of uncorrelated LO phase noise degrades the NF at lower BB frequencies. A differential implementation would prevent this degradation as the coupled noise becomes a common mode and can be rejected after downconversion [35].

D. Blocker Tolerance

Fig. 14 shows blocker tolerance measurements. The IIP_3 has been measured using a two-tone test. The offset of the first tone (f_1) with respect to the LO frequency has been normalized to the BB BW ($f_{-3\ dB}$) in Fig. 14(a). The second tone is placed at $f_{LO} + 2(f_1 - f_{LO}) - 1.5$ MHz such that the third-order intermodulation product always falls IB at 1.5 MHz. The 20-dB/decade filtering slope of the CSNPFM can be observed in Fig. 14(a) starting at the transition to OOB frequencies and saturates, for an f_{LO} of 3 GHz, at around 50 BWs' offset at a maximum OOB IIP_3 of 28 dBm. As can be observed in Fig. 14(a), the second system response (λ_2) translates into a dip in IIP_3 of about 10 dB when the location of the second tone (f_2) coincides with $2f_{LO}$. Fig. 14(b) shows how the OOB IIP_3 varies between 17 and 28 dBm over the LO range and across the three measured samples. Except for an f_{LO} of 1 GHz where f_1 has been placed at 10 BWs' offset to avoid f_2 coinciding with $2f_{LO}$, the offset of f_1 is fixed at 50 BWs for this OOB IIP_3 measurement. The IB IIP_3 evaluates to approximately 1 dBm, slightly increasing to 5 dBm at RF frequencies above 8 GHz, see Fig. 14(b). The measured IB IIP_3 varies less than 5 dB for both the IB and maximum OOB values for the three measured samples and across the LO range [see Fig. 14(b)].

The input-referred second-order intercept point (IIP_2) has also been measured with two tones: f_1 and $f_2 = f_{LO} + (f_1 - f_{LO}) - 1.5$ MHz, resulting in an OOB IIP_2 of >50 dBm across the LO range and for the three measured samples [see Fig. 14(b)]. The blocker 1-dB compression point (B1dB) has been determined by measuring the required interferer power at the blocker frequency f_1 [offset normalized to the BB BW ($f_{-3\ dB}$)] such that there is 1-dB gain degradation in an IB tone applied at f_{LO}+1.5 MHz. The B1dB can be seen in Fig. 14(a) and saturates around 4 dBm at an interferer offset of 20 BWs and shows a similar degradation around the second system response as the IIP_3 showed, as the blocker tone (f_1) coincides with $2f_{LO}$.

Fig. 14(c) shows the blocker impact on the design's NF. The blocker NF (BNF) has been measured at an f_{LO} of 1.4 GHz with a blocker present at $f_{LO}+20\cdot f_{-3\ dB}$. The NF degrades by 4 dB at a blocker power of −10 dBm and by 10 dB at 0 dBm, yielding a 0-dBm BNF of 15 dB, predominantly caused by reciprocal mixing.

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TABLE I
RESULTS' SUMMARY AND COMPARISON WITH STATE-OF-THE-ART MIXER-FIRST RECEIVERS

	This Work			Weinreich et al. JSSC 2023 [23]	Bhat et al. JSSC 2021 [14]	Krishnamurthy et al. SSC-L 2021 [11]	Purushothaman et al. JSSC 2020 [19]	Lien et al. JSSC 2018 [10]
CMOS Technology	22 nm FDSOI			22 nm FDSOI	22 nm FDSOI	28 nm	22 nm FDSOI	45 nm SOI
RF Input	Single-ended			Single-ended	Differential	Single-ended	Differential	Differential
Frequency Range [GHz]	1 – 4	5 – 7	8 – 10	0.3 – 3.0	1 – 6	0.2 – 3.5	0.6 – 1.3	0.2 – 8
R_B [kΩ]	1.5	3.9	20	-	-	-	-	-
Gain [dB]	11 – 12 [1]	12 – 13 [1]	10 – 12 [1]	35 – 40	22	16	9 – 14	21
BB BW [MHz]	10	10	10	1	175	15	16	10
NF [dB]	4.8 – 5.0	4.7 – 6.1	5.2 – 7.0	3.4 – 4.8	2.5 – 5.0	6.6 – 12 [4]	5 – 9	2.3 – 7.1
0 dBm BNF [dB] (@ $(f_1 - f_{LO})/f_{-3dB}$)	15 (20)	-	-	13 (85)	-	9 (6) [4]	14 (10) (@ - 10 dBm) [4]	4.7 (8)
OOB IIP_3 [dBm] (@ $(f_1 - f_{LO})/f_{-3dB}$)	17 (10) [2], 21 (50)	23 (50)	21 (50)	14 – 18 (40)	18 (6) [4]	23 (2) [4]	20 – 25 (10)	39 (8)
IB IIP_3 [dBm]	1	2	5	-12 [4]	9 – 11 [4]	3 [4]	12 [4,6]	0 [4]
OOB IIP_2 [dBm] (@ $(f_1 - f_{LO})/f_{-3dB}$)	59 (50)	64 (50)	56 (50)	65 – 73 (40) [4]	-	-	50 – 66 (10)	88 (8)
OOB B_{1dB} [dBm] (@ $(f_1 - f_{LO})/f_{-3dB}$)	3 (10)	2 (10)	2 (10)	0 (40)	2 (6) [4]	10 (3) [4]	1 (10)	12 (8)
IB-IMFDR$_3$ [♦] [dB]	73	73 – 74	72 – 74	65 – 66	79 – 82	70 – 74	75 – 78	71 – 75
OOB-IMFDR$_3$ [▽] [dB]	84 – 87	86 – 87	85 – 87	82 – 86	85 – 86	83 – 87	84 – 88	97 – 101
LO Radiation [dBm]	< - 65	< - 53	< - 50	< - 63	-	-	< - 70	< - 65
Supply [V]	0.9			0.8	0.83	1.2 / 1.4	0.8	1.2
Active Area [mm²]	0.05 [3]			0.064	0.48 [5]	1.5 [5]	0.23 [3]	0.8
Static Power [mW]	0 [3]			0.43	162.4	86	0 [3]	50
Dynamic Power [mW/GHz]	3.1			0.47	1.7	17	0.6	30

♦ IB-IMFDR3 = 2/3 (IB-IIP3 + 174 – 10 $\log_{10}$(1 MHz) – NF) ▽ OOB-IMFDR3 = 2/3 (OOB-IIP3 + 174 – 10 $\log_{10}$(1 MHz) – NF)
[1] As harmonic losses were absorbed into RF input matching, the expected gain is approx. 12 dB; variations are due to imperfect matching and parasitic losses.
[2] Offset at 1 GHz is lower to avoid f_2 coinciding with $2f_{LO}$. [3] No integrated baseband. [4] Estimated from plots. [5] Complete die area. [6] Data only available at the band edge.

E. Comparison With Prior Art

Table I summarizes the measurement results and compares the presented low-loss CSNPFM to state-of-the-art wideband and low-power mixer-first receivers [10], [11], [14], [19], [23]. As we present the low-loss CSNPFM as a filter/mixer building block, this design does not contain additional BB amplification or channel filtering. Still, we benchmark against mixer-first receivers, stressing that an additional gain block can easily be implemented. Using similar reasoning as in [19], a 3-dB NF can be achieved at less than 2-mW additional power consumption as the voltage gain allows using higher matching resistors placed in feedback, lowering their noise contribution. The static power required to achieve a similar IIP_3 is harder to estimate. The work in [36] allows for a rough estimate as it uses a similar front end while achieving an IB IIP_3 that is 2–3 dB lower and an approximately equal NF. The static power in [36] is just under 10 mW, but this includes the power consumed in the feedback network.

Compared to the other designs in Table I, this work achieves the largest LO range, spanning 1–10 GHz, and achieves both high linearity (>17-dBm OOB-IIP_3) and a modest NF (5 dB), even at high RF frequencies. Compared to the other designs, the front end's gain is only 1.4 dB lower at 10 GHz. For instance, the work in [14] has been implemented in the same technology and achieves a maximum RF frequency of 6 GHz, where it has a 3-dB lower gain with respect to the gain at 1 GHz. Although implemented in an older technology, the work in [10] achieves 8 GHz, where the gain is 4 dB lower with respect to the gain at 0.2 GHz.

As discussed in Section I, we use $IMFDR_3$ to benchmark the designs, combining noise and distortion in a single quantity. For a fair comparison, both the design's power consumption and LO range should also be considered when benchmarking using $IMFDR_3$. Therefore, we plot the IB and OOB $IMFDR_3$ versus power and LO frequency in Fig. 15 for the designs in Table I. The minimum and maximum f_{LO}'s

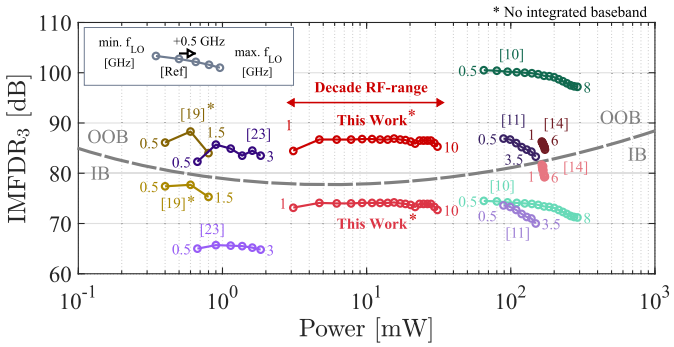

Fig. 15. $IMFDR_3$ versus power consumption and LO frequency (rounded to multiples of 0.5 GHz) for the designs in Table I. Both IB and OOB $IMFDR_3$ have been plotted, and a dashed line indicates the boundary between these sets.

for each design have been annotated, allowing for a quick estimation of the degradation of $IMFDR_3$ over the LO range.

This work achieves the widest LO range and has low losses, therefore showing a relatively constant $IMFDR_3$ over a decade of RF frequency range. Other works show stronger degradation in $IMFDR_3$ at higher RF frequencies. The works in [10] and [11] show a degradation of 4 dB at 8 and 3.5 GHz, respectively, while the work in [19] already degrades by 2 dB at f_{LO} of 1.5 GHz. When considering IB $IMFDR_3$, this work achieves 73 dB, which is in line with most designs spanning more than 3 GHz, except for the work in [14], which has a 6-dB higher $IMFDR_3$ but at the cost of at least 9× more power. OOB, the performance of this work, is comparable to the other designs, except for the work in [10], which achieves a 14-dB higher $IMFDR_3$ at the cost of higher power consumption: over 25× higher at 1 GHz and over 11× higher at 8 GHz. This work outperforms [23] in terms of $IMFDR_3$ but requires higher dynamic power to realize shorter rise and fall times in the clock path to support a maximum 10 GHz f_{LO} frequency.

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V. Conclusion

In this article, a fully passive CSNPFM with low parasitic capacitive losses was proposed. The low-loss design, implemented in 22-nm FDSOI, achieves a passive voltage gain of more than 10 dB over a wide RF frequency range of 1–10 GHz with only a 1.4-dB lower gain at 10 GHz with respect to 1 GHz. The circuit was analyzed using an adjoint network-based analysis, which was enhanced with a discrete state-space model and eigendecomposition to deal with the multiple system responses. Simplified design equations describe key performance characteristics of the design and show that choosing small RF capacitors can save a factor of 4 in area. The circuit achieves 17–28-dBm OOB IIP_3 at a competitive NF of 4.7–7.0 dB for the 1–10 GHz RF range. With a low dynamic power consumption of 3.1 mW/GHz and negligible static power, this design achieves an $IMFDR_3$ of over 72 and 84 dB for IB and OOB, respectively, spanning a decade of RF frequency range.

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