Editorial Interview

The Future of Optical Modulation

The PGE Engages With an Interdisciplinary Panel of Industry and Academic Experts

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1. Could you provide a brief overview of your research experiences on advanced optical modulators?

Response: The authors possess a broad spectrum of expertise with commonly strong interest and experience in advanced optical modulators and integrated photonics. Prof. Di Liang has been doing research and product development on silicon photonics (SiPh) and heterogeneous photonic integration for over 17 years in UC-Santa Barbara, HP Labs, and Alibaba Cloud Computing, and now with the University of Michigan. Dr. Mengyue Xu is an established researcher specializing in $LiNbO_3$ devices and silicon photonics at the University of Michigan. Dr. Long Chen, currently a Distinguished Engineer at Cisco, and previously at Acacia, has led the development of SiPh coherent photonic integrated circuits (PICs) for module products from 100 Gbps (30 Gbaud) to 1200 Gbps (140 Gbaud). Dr. Haisheng Rong, a Senior Principal Engineer and R&D Manager at Intel Labs, is a renowned leader in silicon photonics with over 20 years of experience in the field. Dr. Andreas Bechtolsheim is a globally well-respected technical and industrial leader who co-founded Sun Microsystems and Arista Networks.

2. Silicon photonic modulators have become matured through decades of extensive research and development, what do you think is the bottleneck of current technology?

Response: Indeed, SiPh modulator is arguably the mostly studied pure silicon active photonic device which has achieved the largest technical progress since Soref et al. studied the electro-optic effect in silicon [1]. Due to centrosymmetric crystal structure, silicon lacks strong nonlinear electro-optic effects seen in many III-V compounds. Based on the plasma dispersion effect, non-stop innovations in both academia and industry at a global scale enabled three orders of magnitude improvement in data rate for the past 25 years. Modulation speed has increased from 100 Mb/s level in non-return-to-zero (NRZ) format, to now 224 Gb/s with 4-Level Pulse Amplitude Modulation (PAM4), to over 300 Gb/s with 8-Level Pulse Amplitude Modulation (PAM8) [2], [3], and 1 Tb/s in coherent dual-polarization (DP)-64 Quadrature amplitude modulation (QAM) [4]. Among three major modulator configurations, i.e., p-i-n carrier injection, p-n carrier depletion, and metal-oxide-semiconductor capacitor (MOSCAP) carrier accumulation/inversion [5], the dominant one is depletion type for its fast drift velocity and simple fabrication.

In the meantime, millions of volume produced SiPh modulators, dominated by MZI configuration, up to 200 Gb/s (100 Gbaud) have been deployed for Intra-Data Center (IDC) applications with Intensity-modulation Direct-detection (IMDD) format, and up to 1.2 Tb/s (coherent) for data center interconnect (DCI) and long-haul communication with coherent 16QAM format [6]. Microring-based modulators up to 256 Gb/s in both NRZ and PAM4 format are being developed towards volume deployment by Intel, Ayar Labs, Nubis Communications, and others.

The bottleneck of silicon modulators is that its bandwidth will be unable to keep up with continued baud rate scaling in optical transceivers to 200+ Gbaud. Both the p-n depletion modulator and the MOSCAP modulator rely on charging and discharging of capacitors with electrical current flowing through doped silicon, which cannot be too heavily doped to avoid excessive optical loss and thus access resistance leads to strong attenuation of the electrical current or RF driving signal. This, unfortunately, is dictated by the fundamental material properties of silicon. For MZI modulators, the increasing demand for higher speeds presents significant challenges in balancing bandwidth, modulation efficiency, footprint, insertion loss, and energy efficiency. Typical silicon MZI modulators can have a bandwidth of around 40 GHz. The modulation response roll-off at higher frequencies is relatively gentle since the RF loss scales with the square of frequency. So, it is adequate for 224 Gb/s PAM4 (112 Gbaud)

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with modest amount of equalization on SiPh chip or from the driver [7], [8], [9]. Higher modulator bandwidth can be achieved with a shorter modulator length or other equalization techniques, however, all at the expense of higher driver power consumption.

Resonator-based modulators, such as microring resonators, generally do not suffer the bandwidth limitation dictated by the RF loss. However, to support higher baud rate modulation, the resonance linewidth must increase proportionally, and the enhancement factor from the resonator becomes smaller, requiring a stronger driving signal to achieve the same level of intensity modulation. So, it faces a similar uphill battle for higher baud rates as the MZI modulator. In addition to that, another challenge is the operation robustness since modulation bandwidth, insertion loss, extinction ratio, and TDECQ, especially in PAM4 formats, are all highly dependent on the precise alignment between the resonance wavelength of the modulator and the incoming laser wavelength. Therefore, a well-designed, agile control algorithm that continuously monitors and locks the alignment of the laser wavelength and modulator resonance is crucial for practical commercial applications. An alternative approach involves cascading multiple microrings, each operating at a moderate data rate (e.g., 10–64 Gb/s) and using NRZ formats. By leveraging the intrinsic wavelength division multiplexing (WDM) capabilities of microrings, it is possible to achieve an aggregated bandwidth at the Tb/s level [6], [10], [11]. However, this approach also necessitates precise resonance control for each microring and between adjacent ones.

3. Do we need new materials and integration techniques other than the traditional platforms such as bulk Si, InP and regular $LiNbO_3$? Could you highlight any groundbreaking innovations or breakthroughs in this emerging field?

Response: Yes. Diversity in materials, fabrication processes, and device/photonic integrated circuit (PIC) design is an inherent characteristic of photonics and optoelectronics. This diversity will continue to drive innovation and serve as a key product differentiator, provided that a balance between technical performance and solution cost can be achieved. Expanding applications beyond optical interconnects, such as in sensing, metrology, quantum and other fields, will further support the adoption of varied solutions. If the advantages of silicon photonics, such as high integration density and precise CMOS manufacturing, can be harnessed to incorporate new materials and integration techniques, it could lead to a mutually beneficial strategy.

If we confined our definition of "regular $LiNbO_3$ (LN)" as the bulk LN, then the thin-film $LiNbO_3$ (TFLN) is probably the most promising high-speed modulator platform. TFLN inherits great physical properties from bulk LN, such as a wide transparency window, a large electro-optic coefficient ($r_{33} =$ 31 pm/V), and a linear Pockels effect. The rapid development of TFLN photonics benefits from advances in low-loss etched TFLN waveguides (dry etching, 0.2 dB/m [12]; 4 dB/m [13]; chemo-mechanical polish lithography, 2.7 dB/m [14]), which have a much higher refractive-index contrast ($\Delta n \sim 0.7$) compared to proton-exchanged and titanium-diffused waveguides in traditional LN ($\Delta n \sim 0.2$). The well-confined fundamental optical mode in TFLN waveguides allows electrodes to be placed closer without introducing significant metal absorption loss. As a result, TFLN modulators can achieve higher modulation efficiency, enabling shorter modulation regions and larger bandwidths.

Recent advances in monolithic and heterogeneous TFLN modulators have been rapid and groundbreaking. Due to its simplicity in processing and maturity, various high-performance intensity modulators [15], [16] and complex coherent optical modulators [17], [18], up to 260 Gbaud [19] and 1.96 Tb/s per lane [20], have already demonstrated on the monolithic TFLN platform. Compared with silicon and III-V modulators, the most competitive aspect of TFLN modulators is the design freedom to simultaneously achieve low half-wave voltage, high electro-optic bandwidth without penalty on optical loss, plus the potential to operate over a wide range of wavelengths. COMS-compatible driving voltage and 100 GHz 3-dB bandwidth modulator in C band [16], [20], O band [21] and near-visible [22] had been successfully demonstrated.

Heterogeneous TFLN/silicon and TFLN/Si_3N_4 modulators were demonstrated using die-to-wafer bonding technology with both etched [23] and etchless LN [24], [25], or through transfer printing technology, which do not require further processing after printing [26]. The heterogeneous integration showed competitive performance including a modulation efficiency of 2.2 V·cm, over 110 GHz bandwidth and a modulation rate of up to 112 Gbit/s [21], [23].

What is particularly exciting from another perspective is the much faster commercialization pace of thin-film lithium niobate (TFLN) modulators compared to their silicon and III-V counterparts. This acceleration is largely due to the simplicity of the LN material, the overall fabrication process, and the significantly lower investment and operational costs associated with production infrastructure. Fujitsu has already commercialized 128 Gbaud coherent TFLN modulators [6]. Additionally, 100 Gb/s and 200 Gb/s PAM4 modulator chips and modules with linear drive scheme have been showcased at major industry events like OFC and ECOC over the past two years, highlighting their suitability for IMDD applications.

The III-V external modulated laser (EML), which integrates a III-V electro-optic absorption modulator (EAM) with a monolithically integrated laser, has been a major competitor to silicon photonics transmitters in the market. The large bandwidth, compact form factor, and mature fabrication technology of EAMs make them highly competitive and appealing. Back in 2012, a high-speed heterogeneously integrated EAM on silicon demonstrated over 67 GHz bandwidth [27]. OpenLight [6] is currently commercializing this technology, along with other building blocks, at Tower Semiconductor, another CMOS foundry capable of fabricating heterogeneous III-V-on-silicon devices at large wafer levels.

Developments of new modulator materials have also been reported. Polymer modulators operating 200 Gb/s or above in PAM4 by Lightwave Logic [6] and SilOriX [28] were demonstrated recently with decent material stability. Compact 200 Gb/s thin-film BTO-based modulators operating at sub-V drive voltage was developed by Lumiphase [29] last year, which positions itself a competitive position to TFLN counterparts. Moreover, a whooping 176 GHz EO bandwidth on plasmonic modulators supports over 400 Gb/s operation in PAM8 format by Polariton Technologies [30], which is extremely exciting as well. The market is testing the maturity of these technologies presently. Devices based on MOSCAP structures, either using high-mobility transparent conductive oxide [31], high-k dielectrics [32], [33], or a vertical MOSCAP configuration [34] also embodied impressive design and performance merits in different aspects.

4. What's the most critical requirement of these new materials and integration technologies? Can you name one or two points?

Response: Performance, reliability, and cost are always closely intertwined factors, requiring solution vendors to carefully balance these elements to find the optimal trade-offs for different applications. Typically, these factors are influenced by materials, device and chip design, fabrication, packaging, and testing processes. Additionally, market demand and the feasibility of volume manufacturing, including both chip fabrication and packaging, play significant roles in determining overall costs.

For monolithic TFLN modulators and PICs, 150 mm wafer is the largest size for product presently. Limited wafer size, large device footprint, relatively high material cost, and thin-film uniformity contribute a large portion of the chip cost. Although the chip fabrication is not overly complex, uniform waveguide formation for ultra-low loss operation is not trivial, which necessitates optimized photolithography, etching technology, and post-fabrication processes. Additionally, long-term DC drift remains a challenge for TFLN. To make these modulators commercially viable and reliable, thermally or electrically phase control is a must.

TFLN modulators heterogeneously integrated with silicon or Si3N4 are still in the R&D stage. Similar to III-V-on-silicon heterogeneous integration, TFLN integration occurs towards the back-end-of-line (BEOL) process and requires specialized processing tools along with stringent cross-contamination controls, especially if large-wafer scale processing is involved. The TFLN transfer step is critical for achieving high yield and optimal device performance. In the case of heterogeneous EAMs on silicon, Intel's high yield and laser lifetime records have already demonstrated the feasibility of volume production for heterogeneous III-V-on-silicon devices. However, the process becomes more complex when two or more different III-V epitaxial structures are integrated on the same substrate.

5. How could new modulator materials and configurations impact various emerging applications, such as data centers, AI, quantum information processing, or LIDAR systems?

Response: With the unprecedented surge in generative AI technology, AI compute interconnects have rapidly become a major driving force in the development and deployment of next-generation products, such as 800G and 1.6T pluggable transceivers, with 3.2T systems currently under active R&D. This sector is poised to become the largest market for high-speed modulators in the next 3–5 years. Interestingly, as standards specifically for AI and general high-performance compute interconnects lag deployment demands, there has been a shift towards more innovative designs, with interoperability now considered a secondary requirement.

Emerging applications like quantum information processing, neuromorphic computing, frequency-modulated continuous-wave (FMCW) LIDAR, and microwave photonics certainly will benefit from high-speed modulation. But modulation speed is not necessarily the main technical challenge or key technical specification. For TFLN modulators, they can function as a photonic processing engine or tensor core for optical computing [35], [36], benefiting from TFLN's fast and low-power modulation, which is crucial for accelerating and conserving power in machine learning, AI, and cloud services. Hybrid integration of lasers with TFLN electro-optic tuning enables fast chirp repetition frequency, large chirp bandwidth, and linear tuning, making it an excellent option for frequency-modulated continuous-wave FMCW LiDAR [37], [38]. Frequency-angular resolving LiDAR has been realized through acousto-optic beam steering, utilizing the strong piezoelectricity of LN [39]. Over 1 THz wide flat-top frequency combs have been demonstrated based on the electro-optic effect and parametric amplification of an EO resonator with periodically poled LN [40], indicating great potential for metrology and spectroscopy applications. Additionally, TFLN modulators can operate at cryogenic temperatures, making them ideal for quantum-classical interfaces in superconducting circuits [41].

Heterogeneous III-V-on-silicon modulators, along with this general integration approach, are applicable to a wide range of photonic applications mentioned above. For instance, Intel also leverages their heterogeneous PIC platform for more other applications, including FMCW Lidar technology. Hewlett Packard Labs further advanced MOSCAP modulators to demonstrate non-volatile, sub-nanosecond optical memory effects for photonic neuromorphic computing [42]. Heterogeneous InP microring modulators on silicon, exhibiting a 10 mV modulation voltage and aJ/bit energy efficiency at 4 K, have also been fabricated in the lab [43] for cryogenic PIC applications, such as quantum computing. Additionally, the AlGaAs-on-insulator structure has proven valuable in quantum technology and nonlinear photonics, thanks to its highly competitive nonlinear properties in strongly confined AlGaAs single-mode waveguides [44], [45].

6. What are some of the biggest challenges that researchers and engineers are currently facing in this field? How do you see these challenges being addressed, both from a technical and a market perspective?

Response: Several major technical challenges for silicon MZI and microring modulators were discussed above. One of the biggest challenges—and opportunities—for ultra-high-speed modulator-based optical interconnect solutions is the development of a comprehensive co-design capability and platform. This requires seamless collaboration among designers of photonic and electrical chips, EDA vendors, foundries, packaging, and testing service providers. As we push the material and fabrication physical limits of both optical modulators and electronic circuits, even tiny flaws at each stage can significantly impact device bandwidth, signal integrity, power consumption, and more.

Fortunately, there is growing academic research focused on developing co-design methodologies and machine learning solutions for smaller-scale problems. Additionally, multiple large government-funded R&D programs are addressing this challenge. Leading industrial players with in-house expertise are also working on comprehensive co-design solutions. It is hoped that future-generation EDA tools will feature more powerful capabilities to simulate complex multiphysics systems, considering RF, optical, thermal, nanofabrication processing, and packaging all within a unified framework.

In addition, the progress of SiPh PICs, particularly in their leading application of optical communication, is heavily dependent on the advancement of silicon modulators. A significant challenge, both technological and market-related, facing the entire silicon photonics industry is worth highlighting. The substantial financial and time investment required for product development still hampers the fulfillment of silicon photonics' promise of low cost. While the overall design and processing of silicon PICs are not as complex as advanced CMOS electronics, where a 45 nm-node process is more than sufficient, focus and priorities are fundamentally different. It still takes years of learning for a CMOS foundry to offer basic silicon photonic fabrication services and enhance the product/process design kit (PDK) competitiveness.

Furthermore, the wafer volume dictated by global market demand for silicon photonics is still much smaller compared to microelectronics. The freedom to customize processes in high-volume CMOS foundries is limited, as maintaining process repeatability and uniformity is necessary to consolidate volume. However, this standardization often works against the intrinsic diversity of photonics. Significant efforts are also required to develop more robust and cost-effective packaging solutions, as well as efficient automatic static and RF testing at the wafer scale, especially for edge-coupled chips. Ultimately, every phase of the silicon photonics ecosystem - from R&D to deployment - plays a crucial role in the advancement of next-generation silicon modulators.

To advance TFLN technologies for volume deployment, reducing costs is essential by scaling the state-of-the-art 200 mm TFLN wafers with good film thickness uniformity for volume production. Achieving high yield is crucial with necessity of a foundry-level fabrication with reproducible and high-yield processes. Standardizing the process design kit (PDK) at the foundry level is also required to make TFLN more multi-functional and market-ready. Additionally, we need to reduce TFLN MZI modulators to few mm or sub-mm in length to be feasible and competitive for future co-packaged optics (CPO). Modulators based on ring-assisted designs [16] and slow-light structures [46], [47] have made LN more efficient, achieving lengths in the hundreds of micrometers, although this sometimes requires compromising on operating wavelength or bandwidth. Therefore, future optimization to find the best balance among these figures of merit is crucial.

7. How can industry and academia collaborate to overcome these challenges?

Response: The unprecedented surge in AI and the current global geopolitical situation have led to increased investment in semiconductor technology by governments, industries, and private sectors across all major economic regions in the world. This has resulted in more funding opportunities for collaboration between academia and industry. While differing interests in IP ownership and publications between these sectors are a reality, the industry should be more open to sharing specific challenges they currently face or anticipate in the future. Conversely, academia should be more proactive in understanding and addressing these challenges.

To bridge the gap, more interdisciplinary courses and R&D programs are needed in academia to spark interest in the younger generation, enhance student training in state-of-the-art microelectronics and photonics, and encourage more research in electronics-photonics co-design, integration, and advanced packaging. Additionally, expanding internship and co-development programs will facilitate innovation and workforce development.

Many academic research groups already use EDA tools that are widely adopted in the industry for device and PIC designs. Silicon photonics and general CMOS foundries should continue to develop and upgrade their PDKs and lower the cost barriers for academic customers, particularly for access to the most advanced node processes, to encourage greater academic participation in shuttle runs. Increased collaboration in ultra-high-speed device testing is also critical due to the prohibitive cost of high-speed equipment for most academic groups.

We firmly believe that now is the best time to work on photonic devices and semiconductor technology in both academia and industry. By overcoming the technical and interest barriers between these sectors and preparing young minds for the challenges ahead, we can ensure a continuous flow of innovations to propel the technology forward.

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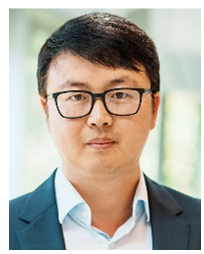

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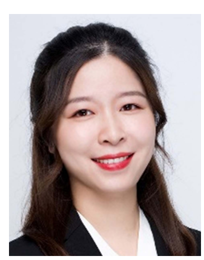

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