A Radiation-Tolerant 25.6 Gbps High-Speed Transmitter in 28 nm CMOS with a tolerance of 1 Grad

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***Abstract*—This paper presents a 25.6 Gbit s^{-1} high-speed transmitter (HST) manufactured using 28 nm CMOS technology. The HST macro-block includes an all-digital phase-locked loop (ADPLL), duty cycle corrector (DCC) circuit, data pattern generator, serializer, and a driver capable of driving the differential 100 Ω line as well as a silicon photonics (SiPh) ring modulator (RM). The design adopts various radiation hardening techniques, such as triple modular redundancy (TMR), physical circuit spacing, and protection against radiation-induced leakage. The circuit achieves a total ionizing dose (TID) tolerance above 1 Grad, which aligns with the future large hadron colider (LHC) detector upgrade requirements. In this paper, the architecture of the HST based on the LC tank-based ADPLL, half-rate serializer, and the source-series-terminated (SST) output driver included in the prototype chip is described. The experimental results are reported, including general evaluation as well as the radiation characterization of the HST.**

***Index Terms*—CMOS integrated circuits, high-speed transmitters, radiation-tolerant electronics, Radiation hardening, Total Ionizing Dose**

I. Introduction

THE dynamic developments in the field of high energy physics (HEP) experiments entail a strong demand for harsh-environments electronic components. Radiation environments foreseen in the high luminosity LHC (HL-LHC) experiments and future accelerators can be characterized by TID levels approaching 1 Grad. Commonly available commercial off-the-shelfs (COTSs) components are not suitable for such applications since they lack any radiation tolerance. Even space-grade integrated circuits (ICs), typically qualified for hundreds of krads, usually do not survive in a particle accelerator environment. This motivates R&D efforts in the field of radiation-tolerant application specific integrated circuit (ASIC) for HEP.

Each new generation of HEP colliders tends to increase either the beam energy and/or the interaction rate to explore the boundaries of physics further. Raw data produced in the LHC experiments approaches levels of 1 PB per second of the run. That amount of data must be transmitted over tens to hundreds of meters to radiation-free environments for further processing and storage. High data volumes combined with a tight material budget require the use of high-speed optical transmitters, which aggregate detector data and transit it out of the experimental areas. This data can then be received by COTS components and further processed in computing centers.

Many radiation-tolerant ASICs have been developed for the LHC experiments. A recent design in the field of radiation tolerant HST is the low power gigabit transceiver (lpGBT) chip [1], which was designed in a 65 nm CMOS technology and serializes data from 40 Mbit s^{-1} to 10.24 Gbit s^{-1} or 5.12 Gbit s^{-1} depending on the chosen transmission mode, and is designed for a radiation tolerance of 200 Mrad. The electrical signals provided by lpGBT are converted into an optical signal transmitted over fiber by the low-power radiation-hard 10 Gb/s VCSEL driver array (LDQ10) co-packaged with a vertical-cavity surface-emitting laser (VCSEL) [2] in Versatile Link+ Transceiver (VTRX+) [3]. Those chips were successfully produced and will be deployed in the detectors during the high luminosity upgrade of the LHC.

CERN's strategic experimental physics R&D program on technologies for future experiments [4] focuses on advancing technologies for future HEP experiments. Within work package 6 (WP6), efforts are concentrated on high-speed links, targeting data rates of 25.6 Gbit s^{-1} and radiation tolerance exceeding 1 Grad. The envisioned system integrates the HST chip with the SiPh chip [5] designed at CERN. Utilizing deep sub-micron CMOS technologies, particularly the 28 nm bulk CMOS node, is the foundation for this endeavor due to its proven radiation resilience and high-speed performance [6–11]. The Demonstrator ASIC for radiation-tolerant transmitter in 28 nm CMOS (DART28) chip, designed within WP6, adopts this sub-micron CMOS technology to meet the requirements of a multi-gigabit transmitter design and facilitates co-integration with the SiPh chip to demonstrate the system performance and radiation immunity. This paper presents a detailed exploration of the circuit architecture (Section II), characterization setup, and results (Section III), followed by discussions on the

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circuit's radiation response (Section IV) and a summary of measurement outcomes (Section V).

II. Circuit Architecture

The DART28 test chip consists of four identical HST replicas and therefore provides four independent outputs. The architecture of the HST is shown in Fig. 1. The primary function of that circuit is to serialize a 640 bit parallel stream provided by the data generator and the data path up to the target output data rate of 25.6 Gbit s^{-1}. Serialization is performed by the half-rate topology serializer using TMR 12.8 GHz clocks received from the DCC (adjusted high-speed phase-locked loop (PLL)s clock) and the TMR clock divider. The driver then transmits serial data over a 100 Ω differential line or an RM.

A. PLL and Dividers

The DART28 PLL is an LC-tank-based ADPLL design generating a 12.8 GHz differential clock from a 40 MHz reference. The circuit includes an oscillator, digital loop filter (DLF), Phase Detector (PD), and an output buffer providing triplicated clock output for successive blocks. The PLL circuit exhibits a random jitter below 300 fs root mean square (RMS) at the power expense below 8 mW.

Its loop incorporates the DCC, which will be further discussed in section II-D, that drives the serializer and the chain of the clock dividers. Dividers derive clock divisions for the serializer and digital logic as well as the feedback 40 MHz clock. The divider is partitioned into three stages: The first stage prescales the clock frequency by 2, providing a 50 % duty cycle clock for the serializer. The second divide-by-5 circuit provides a 20 % duty cycle 1.28 GHz. Finally, the clock signal is further divided in a synchronous divider, generating lower frequencies spanning from 40 MHz and all multiples of powers of two up to 640 MHz. The described frequency plan was motivated by the project requirement of providing all mentioned clock frequencies from 1.28 GHz down to the LHC clock frequency (40 MHz) [12].

B. Data Generation and Control Logic

The DART28 HST features both a data generator and a data path circuit, facilitating the generation of a 640 bit frame at 40 Mbit s^{-1} for serialization. The frame length was chosen so that its repetition rate corresponds to the time between subsequent bunch crossings in the LHC detector, which is 25 ns. Consequently, detector data collected for different collision batches will always be transmitted in separate frames. The frame consists of 560 data bits, 70 error correction code (ECC) bits, and 10 bit frame header. The forward error correction (FEC) implemented in the DART28 is the Reed–Solomon code, capable of correcting up to 35 consecutive bits in a single frame. The length of the FEC was determined to enhance design flexibility and facilitate the efficient reuse of existing hardware blocks rather than being strictly limited by its error correction capabilities. The number of bits allocated for data was determined to ensure compatibility with 16-bit words, resulting in 560 bits for data, while the remaining bits were used for header information and are expected to be used for other functions in the final application. The data generator, included for testing purposes, produces a 560 bits stream of data, representing the front-end chips' data in a practical application, while the data path circuit frames that data. The data path includes a data scrambler that is used to avoid undesirable periodic sequences, which lead to problems in clock data recovery (CDR) on the receiver site, while the FEC encoder and interleaver increase the robustness of the link to transmission errors.

These modules were designed against radiation effects. Specifically, single event effect (SEE) immunity was ensured by using TMR mitigation, while TID tolerance was achieved by putting conservative timing margins to account for anticipated radiation degradation.

C. Serializer

Data generated in the 40 MHz clock domain must be serialized up to the target data rate of 25 Gbit s^{-1}. The serializer circuit is subdivided into low- and high-speed partitions having serialization ratios of 640:20 and 20:1, respectively. The low-speed serializer is based on a single-stage architecture utilizing 32:1 multiplexers with resampling flip-flops at the output. That partition was designed using foundry-provided standard cells and a digital design flow, while the high-speed part design entails a custom approach. Custom cell design and manual placement were employed to balance loads on the clock and data paths and limit the space between clocks, limiting the skew of the clocks. That will result in increasing timing margins of the serializer.

The high-speed partition incorporates three serializing stages, as shown in Fig. 2. The first stage is composed of four 5-bit shift registers, which use the 1.28 GHz clock received from the divide-by-5 circuit as a load signal, while the flip-flops are clocked at 6.4 GHz. A high state of the load signal indicates the loading phase, during which data received from the low-speed serializer is sampled by the flip-flops, while the low state enables the shifting phase, during which the data is shifted towards the circuit output.

Two subsequent 2:1 stages, each consisting of two sampling flip-flops, a delay latch, and a multiplexer, provide two parallel data streams at 12.8 Gbit s^{-1} for the final serialization stage.

The final 2:1 stage generates a pseudo-differential 25.6 Gbit s^{-1} signal and incorporates the capability of providing additional pre- and post-cursor signals used for feed-forward equalization (FFE). As shown in Fig. 3 FFE taps are generated by the 12.8 GHz clocked flip-flops that delay the data input by 1 unit interval (UI). The role of latches is to delay one of the multiplexer's inputs by half a clock cycle to prevent bit changes that may occur when the multiplexer actively selects it.

The generation of pseudo-differential signals is accomplished by integrating a serialization stage replica that operates in parallel but receives an inverted version of the data stream. That decision was dictated by the lowest mismatch between polarities across all process, voltage, and temperature

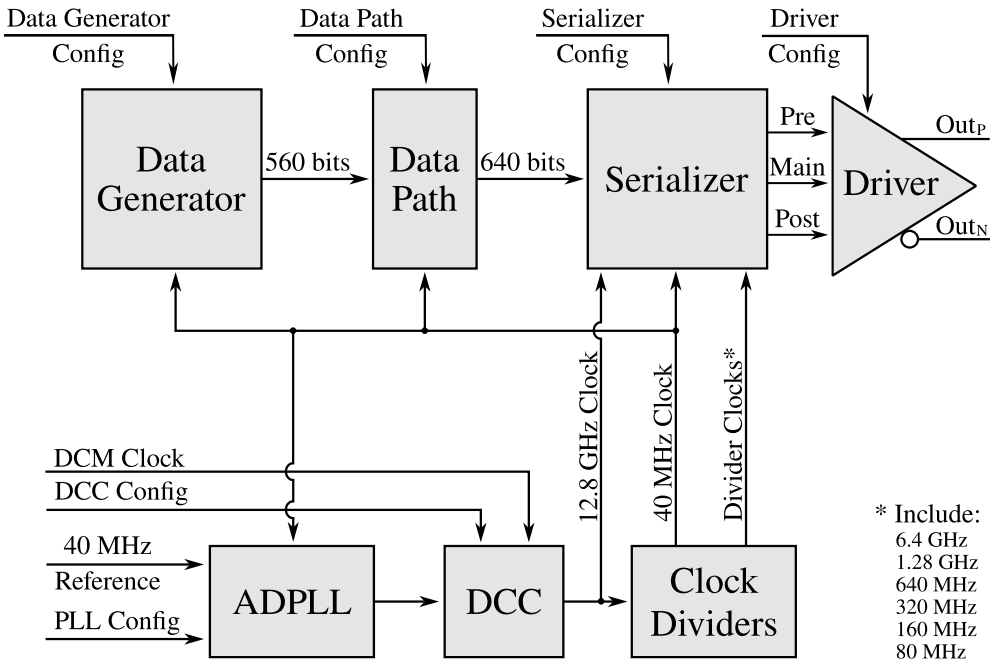

Fig. 1. Block diagram of the DART28 HST

(PVT) corners offered by that method of generating a pseudo-differential signal.

The radiation-induced degradation of the serializer circuits (flip-flops, multiplexers, buffers) increases propagation delay. Based on the radiation characterization, a TID induced slowdown was estimated to be around 20 % [7, 10, 13]. Due to the radiation-induced slowdown of these circuits, the setup margin will be affected, while the hold margin degradation depends on the radiation-induced skew between clocks (difference in degradation of clock trees), thus being less affected. Therefore, to guarantee the correct operation of the circuit at ultra-high doses, the setup margin for the final 2:1 stage was designed to be 38 ps, which is three times higher than the obtained hold margin. In the case of proceeding serializer stages, these times are proportionally larger. These significant timing margins leave a reserve for setup and hold times for TID-induced degradation.

The clock-gating incorporated into the serializer clock distribution can disable the generation of the pre- and post-cursors when not needed to save power. A simplified schematic of the clock gating (see Fig. 3) shows the logical equivalent of the designed circuit.

All latches in the high-speed partition are based on true single-phase-clock (TSPC) logic and are equipped with minimum size pull-down transistor at the output node to settle its state when clock gated, which, together with the use of a dynamic TSPC architecture with anti-leakage mitigation, guarantees that all internal nodes are defined [14]. Used TSPC flip-flops with leakage current protection do not require keeper transistors as they use pre-charge logic, and the proper state of the clock settles the state at all their nodes.

For 1.28 GHz and 6.4 GHz clock signals, gating with the enable signal for the corresponding serializer replica was implemented at the higher level of the hierarchy. The intermediate 2:1 stages of the serializer, due to the use of latches inside their circuits, need the SER EN signal as a KEEP signal. For shift register stages incorporating only flip-flops and multiplexers, clock gating is enough to ensure correct off-state behavior.

The TMR is implemented in the high-speed serializer by instantiating 3 replicas of the 20:1 serializer, with output signals voted by successive voters. For testing purposes, voting can be bypassed. The data TMR block circuit either provides the voted outputs from the serializers or bypasses the non-voted data stream of the A serializer replica, thus disabling TMR. A spacing of 10 µm between each serializer instance ensures a proper operation of TMR, thus guaranteeing SEE immunity of the serializer. No voting of the internal signals of the 20:1 serializer is performed because no internal feedback loops inside the serializer are present. Internal voting would thus not further improve SEE immunity but would rather significantly affect the serializer's power consumption, timing margins, and complexity.

The capability of enabling TMR protection of the serializer provides the capability of switching the protection during the test to compare its efficiency.

D. Duty Cycle Corrector

The TID-induced degradation of buffers and gates in the serializer clock distribution affects its duty cycle, which leads to an increase of even-odd jitter (EOJ) that may reach levels exceeding commonly used interface specifications for electro-optical communications systems [15]. In order to minimize EOJ at the serializer output and to meet the requirements across the entire TID range, a DCC circuit was designed [16]. This circuit, by reducing the duty cycle distortion (DCD) of the 12.8 GHz clock, limits out of EOJ at the serializer output.

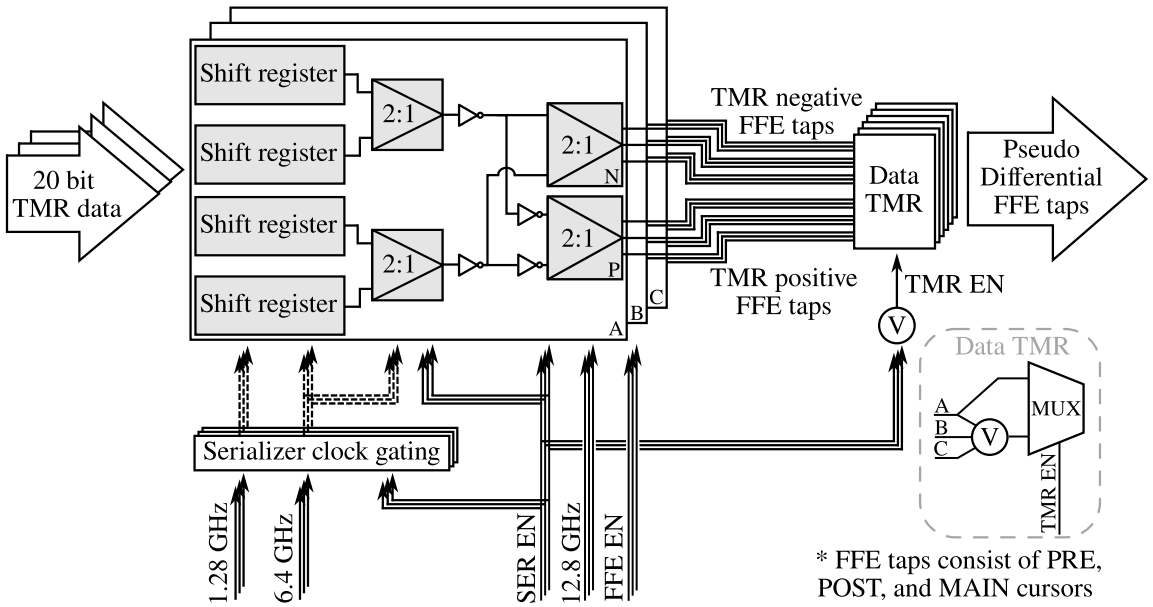

Fig. 2. Structure of the high-speed 20:1 serializer.

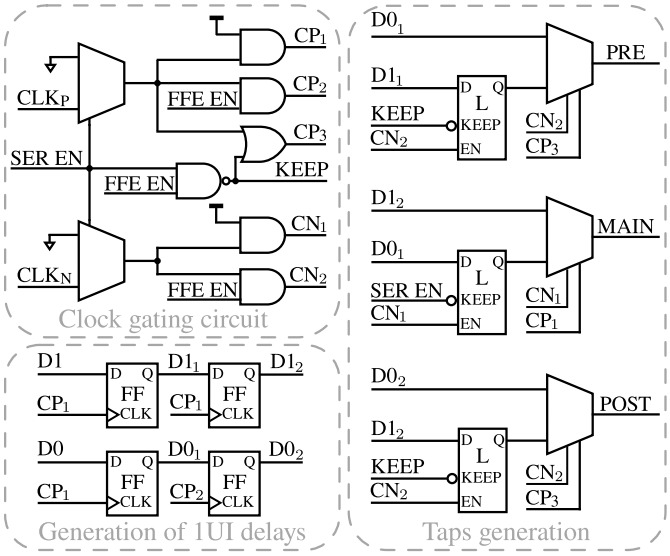

Fig. 3. Simplified schematic of the final 2:1 serializing stage with capability of FFE taps generation.

The DCC circuit consists of two main parts: the duty cycle adjustor (DCA) to correct the clock duty cycle and the duty cycle measurement (DCM) circuit, which monitors the duty cycle and provides feedback to perform adjustments.

The DCA is a set of four cascaded digitally controlled current-starved inverters (DCCSI) performing a precise duty cycle adjustment by controlling the rise and fall times of the applied signal. This is achieved by controlling the control word of the DCCSI, limiting the amount of current flowing through the circuit, resulting in the corresponding change of time needed to charge or discharge the load capacitance. The output clock is then provided to the high-speed serializer, clock dividers, and the DCM circuit.

The DCM circuit adopting the random sampling method consists of a sampling D flip-flop (DFF) and two counters [17]. The basic principle is that the flip-flop clocked by the DCM clock samples the state of the 12.8 GHz clock and forwards the result to the counters. Counters count the number of high states captured by the sampling flip-flop and the number of all samples collected, respectively. The counter values are used to calculate the clock's duty cycle. That value is then used during the DCA calibration, minimizing the difference between the measured duty cycle of the output clock and set target values. The sampling DFF has a hysteresis below 10 fs and thus does not introduce any measurement bias. The DCM clock operates asynchronously relative to the measured signal and, for the DART28 prototype, is sourced from laboratory instrumentation. For DART28 prototype purposes, the DCM clock is provided with laboratory instrumentation.

Since the clock is the most crucial signal for a reliable transmitter operation, a TMR is incorporated in the entire clock path, including triplicated circuits of the DCC. The TID response of the DCA was evaluated with simulations in [16], showing only limited degradation of 0.3 % at 700 Mrad. Furthermore, the DCM measurement error is not expected to increase noticeably due to a matched radiation-degradation of input differential NMOS pair in StrongARM latch-based sampling flip-flop [18].

The designed DCA circuit has the capability of tuning the duty cycle in the range of $\pm$ 6 % with a resolution of 0.5 % extending the margin for radiation degradation.

E. Dual Use Driver (DUDE)

The DART28 prototype design facilitates co-integration with a photonics integrated circuit (PIC) to showcase an optical data link. However, to perform electrical characterization of the ASIC and demonstrate optical transmission with the same driver, an output driver capable of driving both loads was designed [19].

The DUDE can drive a 100 Ω differential transmission line as well as SiPh RM (capacitive load). The designed driver is an SST based architecture designed to operate at 25.6 Gbit s^{-1}, providing a pseudo-differential non-return-to-zero (NRZ) output signal.

Three-tap FFE is implemented in the circuit to overcome the potential bandwidth limitations of transmission line channels. Moreover, an edge pre-emphasis feature is implemented in the circuit by temporarily increasing the current during the signal transition to boost the transition times. Both features are programmable, providing control over emphasis amplitude and edge pre-emphasis pulse duration.

III. Experimental Results

A. Test Bench Setup

To conduct tests of the ASIC, it was wire-bonded to a printed circuit board (PCB) [20]. A low jitter 40 MHz reference clock was provided to the on-chip PLL externally. A Keysight 81134A pulse pattern generator was used to generate the DCM clock to test the DCC circuit.

A wide-bandwidth (33 GHz) Keysight UXR0334A oscilloscope with a sampling rate of 128 GS s^{-1} was used to capture eye diagrams of the DART28 output data stream and evaluate the link bit error rate (BER) under various operating conditions. The same instrument was used to observe the influence of the DCC system on the output data during the tests. The power consumption of the device under the test (DUT) was measured by onboard voltage and current monitors ICs.

B. Measurement Results

During the evaluation of the DART28, it was assessed that the chip operates in a range of ±10 % variations from the nominal voltage supply of 0.9 V. The power domain of the HST macro includes many components. Therefore, the capability of selectively enabling or disabling different blocks was used to assess the power consumption of individual blocks shown in Table I. The power consumed by the serializer for all operating modes includes the power dissipated by the DCC circuit consuming ∼ 20 mW. The total power consumption of the HST is dominated by the output driver contribution, which, depending on the operating mode, varies from 77 mW to 141 mW.

TABLE I
Power consumption of the serializer (including DCC) and driver for various modes of operation at the nominal power supply voltage.

HST settings		Power consumption [mW]		
TMR	FFE	Serializer	DUDE	Total
No	No	33	77	110
No	Yes	43	141	184
Yes	No	53	77	130
Yes	Yes	67	141	208

During the tests, all serializer operating modes have been validated and characterized, demonstrating its operation at 25.6 Gbit s^{-1} (see Fig. 4). During the prototype evaluation, a high level of data dependent jitter (DDJ) for pseudo random bit sequence (PRBS) data transmission having a destructive influence on horizontal eye-opening was noticed. An error-free transition of PRBS7 sequence was achieved, while for longer patterns, higher DDJ values lead to transition errors.

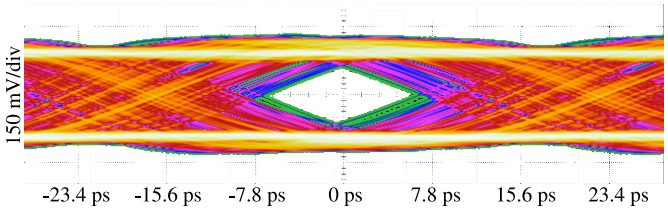

Fig. 4. Eye diagram for the PRBS7 sequence transmitted over one HST channel while the rest of the on-chip channels are disabled.

An in-depth analysis of the problem showed that it is related to power delivery issues. Even for short wire bonds used, the connections manifest inductance of approximately 500 pH. The non-negligible inductance of the power delivery network (PDN), comprised of wire bond interconnect and the PCB impedance, and the limited on-chip decoupling capacitance being around 1.3 nF, creates the PDN that may limit the current flow to the chip. The supply voltage fluctuation may affect the propagation delay of the circuits appearing at the output as a DDJ. The contribution in the data jitter coming from the output driver and serializer was analyzed by simulating their supply sensitivity. Both circuits showed similar sensitivity at a level of 250 fs mV^{-1}. This, together with the jitter value obtained from the eye diagram, indicates the maximum dynamic voltage drop of around 50 mV.

The time interval error (TIE) spectrum measurement shown in the Fig. 5 gave information about the PDN characteristic, highlighting its resonance around 180 MHz. The obtained response frequency matches with the simulated resonance peak of the PDN impedance for the ASIC power grid, interconnect, and PCB. The spectrum obtained combines the current spectrum of the operating HST and the PDN impedance. The impedance of the PDN is primarily constrained by the limited on-chip capacitance and interconnect inductance, both of which are expected to be addressed in the following design revision by using interconnects with lower inductance and increasing on-chip decoupling. However, for the current design, the chip's current profile can be altered to reduce the observed issues.

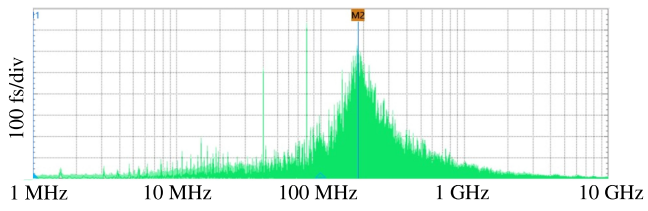

Fig. 5. TIE spectrum obtained from chip measurement showing the peak at 180 MHz.

A method of suppressing this problem was devised to evaluate the signal quality. On an adjacent channel, a specially

crafted sequence was transmitted to equalize the on-chip transition density over time. This way, the internal supply voltage remains constant regardless of the data transmitted on the primary output channel, suppressing the DDJ observed before at the cost of increased power consumption. The improvement in DDJ achieved by using this technique is shown in Fig. 6. The eye horizontal opening improved by 20 ps, while the vertical opening remained the same.

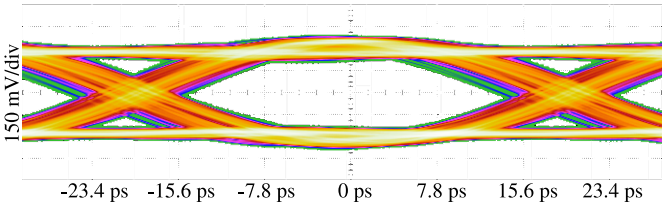

Fig. 6. Eye diagram for the PRBS7 sequence transmitted over one HST channel with an additional channel transmitting a sequence that equalizes power consumption.

IV. Radiation Tolerance

An extensive characterization of the circuit's radiation response was performed in the context of the TID tolerance and the SEEs immunity.

A. Total Ionizing Dose

To evaluate the TID tolerance of the chip, the CERN X-ray facility was used [21]. A Seifert RP149 X-ray machine providing a dose rate of 12.5 Mrad h^{-1} was used to accumulate a dose of 1 Grad in ∼80 hours of irradiation. The Huber Unistat 705 thermal cooling system has been used to ensure that the DUT temperature remains at 25 °C throughout the irradiation process.

During the irradiation, BER measurements were continuously performed using a high-bandwidth Keysight UXR0134A oscilloscope equipped with built-in CDR. PRBS7 data was transmitted for BER measurement, whereas a short data pattern with reduced run length was used for eye diagram measurements. During the measurements, the serializer was operating in non-TMR mode without pre-emphasis tap generation, while the output driver was configured to 100 Ω line driver mode with moderate driving strength.

The DCC circuit was characterized during the same campaign. A DCM measured the duty cycle by collecting statistics of 2^{16} samples, guaranteeing error levels below 0.5 % in all measurement points.

Fig. 7 shows the evolution of the duty cycle error as a function of the TID for the two cases - when calibrating the device only once before the irradiation ("Raw") and with periodic calibration over its life span ("Corrected"). Data for DCC calibrated once shows that an acceptable difference between the output duty cycle and target duty cycle value may be exceeded at a level of 100 Mrad. The total degradation of the DCC, calibrated only before irradiation, reaches levels above 1 % at higher TID, revealing a degradation higher than predicted by simulations using post-irradiation transistor models [16]. The discrepancy is possibly due to the radiation modeling of the transistors, which was based on a limited number of transistors. Therefore, these models may not include the whole spectrum of possible degradation affecting the simulation results for the DCC.

The DCC plays a crucial role in extending the TID-tolerance of the serializer, assuring the output clock's duty cycle remains within an accuracy of 0.5 %. This means that performing only one calibration of the circuit in a pre-rad state is not a practical solution. Therefore, to maintain the duty cycle at the desired level throughout the entire TID range, performing calibration of the DCC settings over TID is necessary and should be done after each power-up of the chip during its lifetime. A circuit operating under that scheme is able to keep the duty cycle error within the desired range for both adjustment targets throughout the irradiation period. Moreover, in this case, the DCC settings were corrected more than once to keep the output duty cycle at the desired levels, highlighting the need for frequent calibration of the circuit over its lifetime.

The eye diagram parameters, including its width and height, were monitored over the whole TID range (see Fig. 8). For high and nominal power supply voltages, the eye width shows a total degradation of ∼2 ps, while the eye height showed much higher dynamics of the degradation, resulting in a final degradation of 18 % compared with the values before irradiation. Nonetheless, this degradation has not affected the PRBS data transmission reliability of the DART28 chip, which, for the whole period of irradiation, remained error-free.

The situation is different for the lowest power supply voltage, for which transmission failures were observed at TID levels above 1.4 Grad. They manifest as a significantly reduced swing of the pseudo-differential outputs of the chip. This may indicate failures in the serializer or inside the DUDE. Therefore, a deeper analysis was performed on the irradiated chip. The recorded data stream for 0.81 V supply for the irradiated chip showed the corruption of only two bits in the entire 640 bit frame. The position of those bits in the frame is constant, and the spacing between them is precisely 320 bits apart, suggesting that the root of the failure may be related to the 40 or 80 MHz clock domain. Since the measurements excluded coupling with the 40 MHz reference clock, an in-depth analysis of the dynamic voltage drop in the DART28's HST was performed. Through measurements, it was possible to approximate the delay between the circuit leading to failure and the chip output, being way below the DUDE delay discarding the serializer, leading to the conclusion that part of the circuit is responsible for the failure. Possibly, this misbehavior is caused by the combination of the radiation-induced degradation of the circuit driving strength and the peak of the voltage drop at 40 MHz induced by the operation of all circuits inside the HST including high-speed serializer, DCC, all clock dividers and the DUDE itself.

The power consumption of the domain, including four HST copies, has been monitored over the irradiation process. All replicas are operating in TMR mode with the enabled FFE feature. The evolution of HST power consumption over TID for nominal and ± 10 % variations of power supply voltage is shown in Fig. 9. The missing points for the highest supply at low dose levels were caused by the test bench communication

Fig. 7. Evolution of the duty cycle error a the output at the DCC circuit within the tested TID range for the fixed settings of the circuit based on the calibration performed before irradiation ("Raw") and the continuous calibration over the TID evolution ("Corrected").

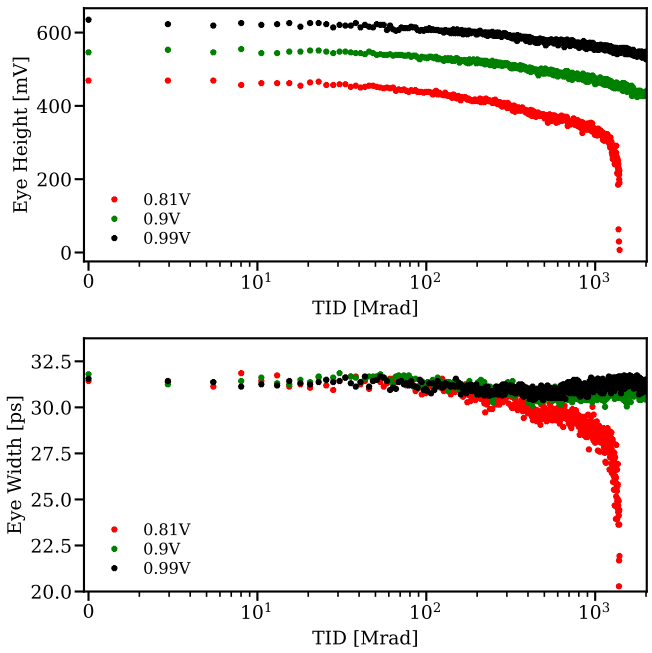

Fig. 8. The TID-induced degradation of main eye diagram parameters.

issues, which resulted in a non-valid readout. The power consumption for the nominal power supply voltage nominal power supply remained unchanged within the specified dose range (1 Grad). For this supply, meaningful degradation has been seen above this dose, approaching 5 % at 2 Grad TID. For a 0.81 V supply, the degradation process may already be observed above 500 Mrad, exceeding 6 %. Moreover, it can be seen that the TID-induced degradation has a lower impact on overall power consumption than the power differences caused by the supply voltage variation.

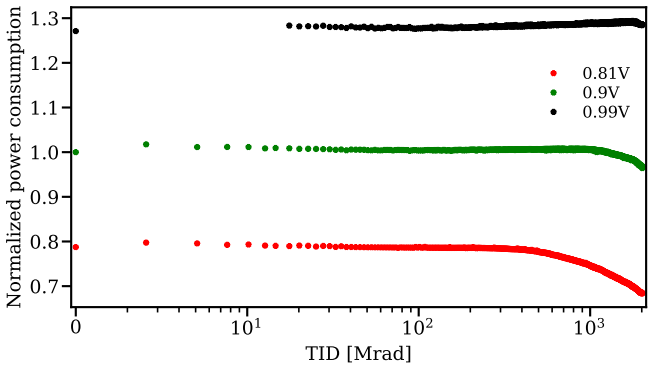

Fig. 9. The evolution of the power consumption of the DART28 HST transmitter for three power supply voltages over TID. Power consumption was normalized with the pre-rad measurement for the nominal power supply voltage (0.9 V).

B. Heavy Ion Tests

The SEE immunity was assessed by exposing the chip to heavy ions in a radiation effects facility (RADEF) in Finland. The heavy-ion cocktail used, together with the ion energy and the linear energy transfer (LET), is shown in Table II.

The test bench setup consists of the DART28 chip wire bonded to the test PCB, field programmable gate array (FPGA), Intel QSFP transceivers, and high precision timing clock (HPTC) board providing a reference clock for the chip. The QSFP modules are used to convert electrical high-speed data (framed PRBS7) produced by DART28 to an optical signal transmitted over fiber to the receiver on the FPGA side.

TABLE II
RADEF HEAVY ION COCKTAIL USED DURING THE CHIP TESTS WITH OBTAINED FLUENCE FOR EACH PERFORMED TEST

Ion	Energy [MeV]	LET [MeV cm^2 mg^{-1}]	TMR	Fluence [ion cm^{-2}]
$^{126}Xe^{44+}$	1217	60.0	0	1.54×10^7
			1	1.14×10^7
$^{83}Kr^{29+}$	768	32.2	0	2.8×10^7
			1	3.02×10^7
$^{57}Fe^{20+}$	523	18.6	0	3.48×10^7
			1	3.31×10^7
$^{40}Ar^{14+}$	372	10.1	0	7.74×10^7
			1	8.28×10^7
$^{20}Ne^{7+}$	186	3.63	0	1.21×10^8
			1	2.37×10^8

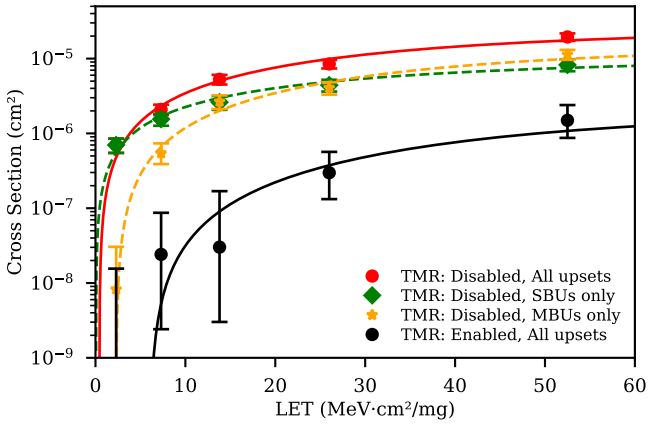

Fig. 10. Cross section of the single HST in function of the LET with fitted Weibull curve for protected and non-TMR protected circuit. Dashed curves illustrate the cross-sections of the HST considering only SBUs or MBU exclusively for the circuit with the disabled TMR. For TMR protected circuit, no errors for the lowest LET ion have been observed.

Fig. 10 shows the experimentally obtained cross-section for the HST circuit, both with TMR protection enabled and disabled. The Weibull model was fitted to both data sets using the procedure described in [22]. For the HST operating with TMR protection disabled, the cross-section includes components coming from both serializer partitions, DUDE, and the data path. This is due to the way the TMR was implemented in the HST disabling the TMR in the serializer independently from the data path is not possible. Moreover, during both protection cases, the interleaving feature was disabled, significantly reducing the effectiveness of FEC encoding. Therefore, analyzing FEC-protected data is futile. Data demonstrates a significant improvement achieved using the implemented TMR strategy, reducing the limit cross section by at least an order of magnitude and substantially increasing the upset threshold LET. The cross-section of the TMR protected circuit does not reach zero because ions still can generate the single event transient (SET) in the serializer's TMR multiplexer or DUDE, resulting in data corruption. The obtained cross-section values align with the expectation of the sensitive area of DUDE.

The SEE data for enabled TMR has been used to analyze SEE inside DUDE. The TMR protection of the data path and serializer masks any bit upsets originating in these circuits, leaving only the driver sensitive to SET. The longest observed SET inside the driver had a length of 7 bits, being equivalent to 274 ps. This was observed only for the most energetic ion, while for the $^{83}Kr^{29+}$ the length of the burst was halved, and for the $^{20}Ne^{7+}$, no errors were observed. Nonetheless, all of these error bursts are shorter than the correction capability of the employed FEC. Therefore, they can be corrected, ensuring error-free data transmission. With TMR protection disabled, errors can be spaced even 205 bits apart, which cannot be corrected by the implemented FEC, leading to errors on the receiver side. Moreover, for that configuration, it was possible to separate MBUs originating from the single particle affecting vertically abutted registers (based on mapping errors with corresponding registers positions) in the data path and the low-speed partition of the serializer. The occurrence of this specific type of MBU arising from adjacent registers is relatively low, corresponding to only 5 out of a total of 82 MBUs across all tested ions. The meaningful fraction (around 34 %) of MBUs is related to the upsets in high-speed serializer shift registers. The rest of the multi-bit errors are caused by SETs in the driver, transient on the clocks in the data path and serializer. This is supported by a significantly higher threshold of the cross-section observed when considering only MBUs compared to SBUs.

The heavy-ion data is useful for estimating cross-section in the HL-LHC experiment environment. For that purpose, the procedure described in [23] was used to estimate the expected error rate in the environment of a pixel detector positioned very close to the interaction region, where the largest fluxes occur [24]. When operating the circuit without TMR protection, it presents a cross-section of 6.76×10^{-12} cm^2, indicating almost 8760 data errors per day of operation, while the protected circuit shows a cross-section reduced by more than two orders of magnitude to 2.33×10^{-14} cm^2, which results in 30 bit errors per day. In the case of TMR protected design, the number of errors is within the range that will certainly corrected by implemented FEC, ensuring error-free operation, while for the circuit without protection, errors may be observed at the receiver side due to their characteristic (error spacing).

V. CONCLUSIONS

The design of a radiation-tolerant HST capable of operating at 25.6 Gbit s^{-1} in 28 nm CMOS was presented. The circuit incorporates all components required for stand-alone operation: ADPLL, DCC, dividers, serializer, and output driver able to drive differential line or SiPh ring modulator. The circuit can operate at the nominal data rate, even though issues in power delivery currently degrade the signal integrity. The correct operation of the designed high-speed transmitter macro was confirmed for the power supply voltage variation of ±10 % from nominal 0.9 V and over the specified TID range. The assessed SEE immunity confirmed the effectiveness of the implemented TMR strategy, guaranteeing error-free operation of the designed HST in the LHC environment, making it

suitable for use in future HEP experiments. The comparison with other designs emphasizes the success of the DART28 prototype design, showing a significant improvement in the field of radiation-tolerant high-speed transmitter, being the first to demonstrate TID tolerance exceeding 1 Grad. The initial chip evaluation revealed the power integrity issue that will be addressed in the next revision of the chip.

TABLE III
COMPARISON OF THE GENERAL PERFORMANCE OF THE DART28 HST WITH THE MOST RECENT DESIGNS IN THE FIELD OF RADIATION-TOLERANT TRANSMITTERS

	This work	[25]	[26]	[27]	[28]
Technology	28 nm	28 nm	65 nm	65 nm	130 nm
Supply (V)	0.9	0.9	1.2	1.2	1.2
Data rate (Gbit s^{-1})	25.6	8	4.8	12.5	5.12
FFE	3-taps	3-taps	No	No	No
TID (Mrad)	1400	1.2	200	-	-
Power (mW)	225	80	30*	113	120
Efficiency (pJ bit^{-1})	8.79	10	6.25*	9.04	23.44

* only serializer power consumption

Table III compares the work described in this paper with recent designs of radiation-tolerant transmitters for HEP. The comparison is made against several designs using 130 nm, 65 nm, and 28 nm CMOS technologies. DART28 HST displays significant improvement in terms of data rate and radiation tolerance compared to another recent design fabricated in the same technology node [25].

The driver's reconfigurability was required for characterization purposes. Renouncing this feature in favor of enhancing power efficiency could lead to further reductions in power consumption in the final application.

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