A Multifunction Radiation-Hardened HV and LV Linear Regulator for SiPM-Based HEP Detectors

Paolo Carniti, Claudio Gotti, and Gianluigi Pessina

***Abstract*— The use of silicon photomultipliers (SiPMs) to detect light signals in highly radioactive environments presents several challenges, particularly due to their sensitivity on radiation, temperature, and overvoltage, requiring proper management of their bias supply. This article presents the design and performance of ALDO2, an application-specific integrated circuit (ASIC) and power management solution tailored for SiPM-based high-energy physics (HEP) detectors. The chip's functions include adjustable and point-of-load (PoL) linear regulation of the SiPM bias voltage (10–70 V, 50 mA), monitoring of SiPM current, shutdown, and overcurrent and overtemperature protection. The same functions are also available for the low-voltage (LV) regulator (1.6–3.3 V, 800 mA) used to generate the power supply of SiPM readout chips that often demand stable and well-filtered input voltages while consuming currents of up to several hundred milliamperes. The chip is intended to operate in radioactive environments typical of particle physics experiments, where it must withstand significant levels of radiation (total ionizing dose (TID) and 1-MeV-equivalent neutron fluence in the range of Mrad and 10^{14} n_{eq}/cm^2, respectively). The article provides a comprehensive description of the chip design as well as experimental measurements, offering insights into the chip's performance under various conditions. Finally, radiation hardening, radiation qualification, and reliability are discussed.**

***Index Terms*— Application specific integrated circuits (ASIC), low dropout (LDO) regulators, photodetectors, power integrated circuits, radiation hardening (electronics), semiconductor detectors.**

I. Introduction

SILICON photomultipliers (SiPMs, also known as multipixel photon counters or MPPCs) [1] have gained widespread use in various high-energy physics (HEP) experiments, primarily due to their excellent photon counting performance, compactness, and immunity to magnetic fields. Despite being more practical and durable than vacuum-based photosensors, integrating SiPMs into experiments still presents several challenges, particularly concerning their power supply. Radiation damage, in fact, leads to a significant increase in the dark current, reaching up to a few milliamperes per device, and a shift in the breakdown voltage, which can deviate by several hundred millivolts from the typical value of a few tens of volts. To mitigate the effects of radiation, SiPMs are typically cooled below 0 °C [2], [3], adding further drifts due to temperature variations. All these shifts in the breakdown voltage, in addition to the intrinsic production spread, must be compensated by the bias supply generator throughout the experiment lifetime, since SiPM performance depends strongly on the overvoltage (the excess bias over the breakdown voltage).

The ALDO2 is an application-specific integrated circuit (ASIC) specifically designed to handle the power management of detectors using SiPMs (usually grouped in arrays of 8–16 devices). Its primary functions are summarized in the following.

1) Adjustable regulation of the SiPM bias voltage.
2) Point-of-load (PoL) regulation of SiPM bias voltage to enhance stability and noise filtering.
3) Monitoring of SiPM current for on-detector I–V curve characterization.
4) Shutdown, and overcurrent and overtemperature protection.
5) PoL regulation and filtering for the low voltage supply of front-end ASICs.

The chip has to operate in highly radioactive environments, typical of HEP experiments. Given the chip proximity to the SiPMs, the maximum radiation levels are constrained by the capabilities of currently available SiPM models, specifically a 1-MeV-equivalent neutron fluence of a few 10^{14} n_{eq}/cm^2, and a total ionizing dose (TID) of a few Mrad.

This article will start with a general overview of the ALDO2 chip and its architecture (Section II). Sections III–V will describe in more detail the circuit solutions for the various parts of the chip, each complemented by experimental measurements of key parameters. This article will then discuss the chip layout and radiation hardening (Section VI), followed by results of radiation hardness qualification (Section VII) and, finally, assessments of yield and reliability (Section VIII).

In addition to being the first all-in-one SiPM and front-end powering solution for HEP experiments, the ALDO2 ASIC stands out for a number of original contributions, notably the development of a high-voltage (HV) error amplifier using voltage-limiting techniques inherited from digital level shifters (Section III-A), the application of the "composite" MOS topology as a radiation-harded temperature sensor (Section V), and the detailed description of a radiation-hardened layout for the HV n-type MOSFET (Section VI).

II. Chip Overview

ALDO2 is fabricated using onsemi I3T80 0.35-μm CMOS technology. I3T80 was specifically selected since it provides

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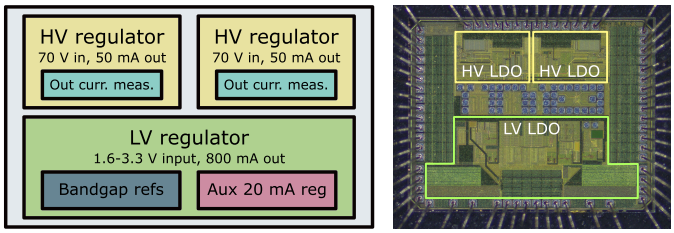

Fig. 1. General block schematic of the chip (left). Photograph of the ALDO2 die with outlines of the HV and LV sections (right). Die dimensions are 2.5×2 mm^2.

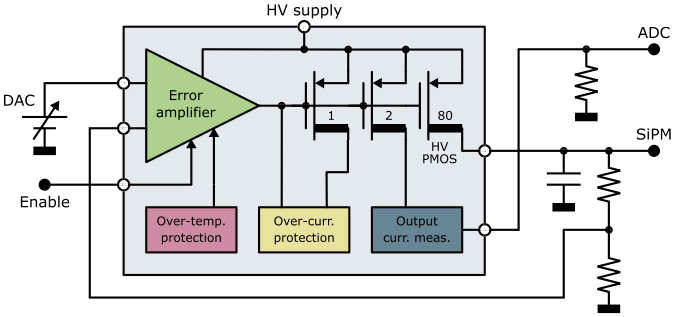

Fig. 2. Simplified block schematic of the HV regulator (two identical ones are included in each ALDO2). Devices with thick drain are HV DMOSFETs.

both low-voltage (LV) and HV MOSFETs, as well as adequate radiation tolerance [4] with respect to the target radiation levels discussed above. Only devices with thin gate oxide and maximum V_{gs} of 3.3 V are used in the ASIC as they are the only ones suitable for the target radiation levels. I3T80 includes lateral and vertical double-diffused MOSFETs (DMOSFET) that can operate with V_{ds} up to 70 V, as well as floating wells, diodes, matched resistor arrays, and bipolars. Both the LV and HV n-type devices require specific custom layout modifications to attain the target radiation tolerance, as detailed in Section VI. It is also known that DMOSFETs experience an increase in on-resistance as a result of displacement damage in the drift regions, although this effect is expected to become significant for I3T80 only beyond the specified radiation levels [4].

The chip consists of two completely stand-alone sections, HV and LV, as illustrated in Fig. 1 with the general block schematic (left), and a photograph of the chip die (right).

The HV section comprises two identical low dropout (LDO) linear regulators. Each one can regulate an input voltage of maximum 70 V down to an adjustable value and deliver up to 50 mA to the load (an array of SiPMs). The block schematic for this section is presented in Fig. 2. During the preliminary design phase, various topologies were considered. Ultimately, high-side active linear regulation was deemed the most suitable, as it offers superior stability and noise characteristics compared with passive trimming, while maintaining >90% efficiency (provided that dropout is in the ∼V range).

To adapt the SiPM bias voltage during detector operation, the output voltage of the regulator is adjusted by applying a programmable voltage to the reference input of the regulator using an external DAC. The DAC is integrated in the SiPM front-end ASIC or in other slow-control ASICs present in the system. Typically, the DAC adjustment range is from

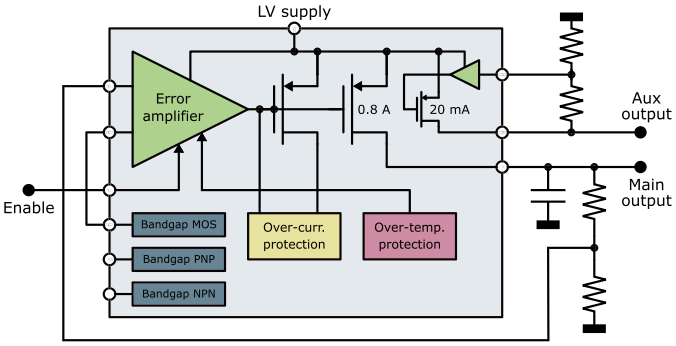

Fig. 3. Simplified block schematic of the LV regulator.

0.75 to 1 V, although values up to 3.3 V can be used. The feedback resistors are external, and the gain is usually between 30 and 50 V/V, depending on SiPM specifications. The regulator can be disabled with a digital signal, useful in case of a malfunctioning SiPM. It is also protected by an output current-limiting circuit (without foldback), which operates alongside an overtemperature block that disables the error amplifier when the die temperature exceeds a fixed threshold. The output current is measured by copying it through current mirrors, then converted into a voltage using an external resistor, and finally fed to an external ADC.

The LV section incorporates a high-current (maximum 0.8 A) primary LDO regulator, a low-current (20 mA) auxiliary LDO regulator, and integrated bandgap voltage references, as illustrated in the block schematic in Fig. 3. This section's design is similar to ALDO2 predecessor, ALDO1 [5]. Both the main and auxiliary LDOs are adjustable using external feedback resistors. The LV section adopts only LV devices, thereby limiting the maximum input supply to 3.3 V. A linear topology is preferred to achieve the best possible filtering of the input supply, which is typically generated by DCDC regulators. Similar to the HV section, the regulators are protected with overcurrent and overtemperature circuits. Three bandgap voltage reference circuits are included, each based on the same topology but with different devices to generate the proportional and complementary to absolute temperature (PTAT and CTAT) voltages (PNP bipolars, NPN bipolars, and dynamic-threshold MOS transistors or DTMOSTs [6]). The bandgap selection depends on the final application and is made externally by connecting the bandgap output to the voltage reference input of the error amplifier. Bipolar-based bandgaps are expected to have better thermal stability and uniformity. DTMOST-based one has higher radiation tolerance and lower reference voltage (0.63 V).

The chip is packaged in QFN64 (9×9 mm^2) and has been produced in large quantities (45 k chips from 26 wafers) for use in two detectors of the CMS experiment at CERN, the Barrel Timing Layer (BTL) [7], [8], and the High-Granularity Calorimeter (HGC) [9].

III. High-Voltage Section

A. Circuit Description

The core parts of ALDO2 are the two HV LDO regulators. Fig. 4 shows their complete schematic. The regulator is

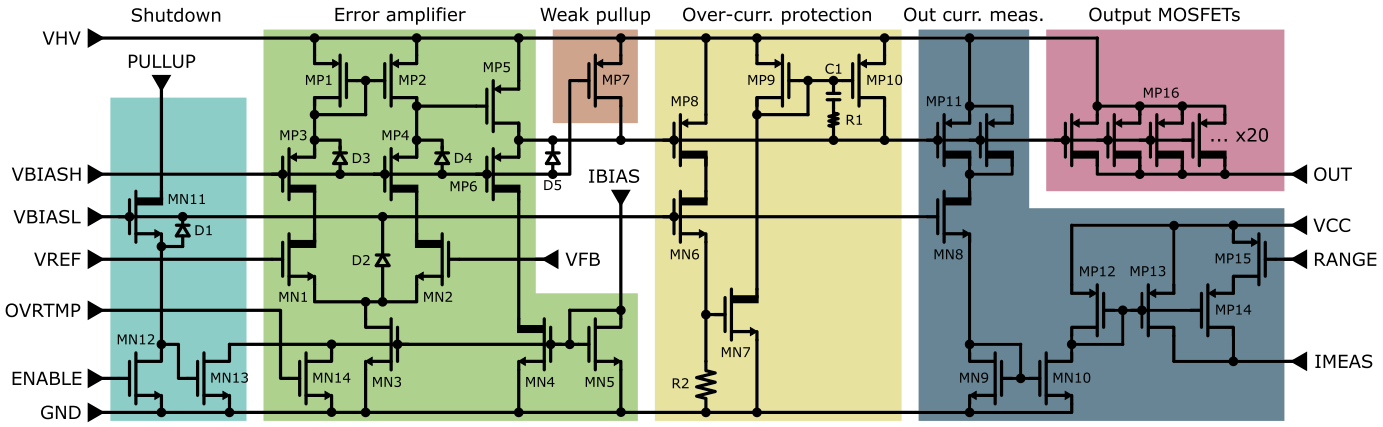

Fig. 4. Full schematic of the HV regulator. All the MOSFETs have the substrate connected to their source. Devices with thick drain are HV DMOSFETs. Diodes are made with diode-connected MOSFETs.

required to be powered between the HV rail and ground, while using only thin-oxide transistors with a maximum gate voltage of 3.3 V. The p-type pass element and its driving circuitry operate close to the positive rail to minimize the dropout, while the input pair and other circuits operate close to the ground rail since they must interface with external LV components (SiPM readout ASIC, DAC, and ADC). More details are discussed in the following.

The error amplifier (green block) is a two-stage n-type-input opamp. The circuit uses a voltage-limiting solution using cascode p-type DMOSFETs (MP3, MP4, and MP6) with gates biased by the external voltage VBIASH (2–3 V below the HV rail) to protect regular LV p-type MOSFETs (MP1, MP2, and MP5). The role of these DMOSFETs is twofold: they can withstand the full HV drop between the source and the drain in case of significant input pair imbalance and they limit the drop across LV p-type MOSFETs in various conditions where the drain of the LV pMOS would be pulled below $V_{\mathrm{BIASH}} + V_{\mathrm{th,pDMOS}}$ (such as saturation or OFF-state). A similar approach is commonly used in level shifters for digital circuits and DCDCs [10].

The concern of exceeding the maximum rating also extends to the input pair (MN1–2), whose drain voltage can range up to the positive rail in normal use (weak or moderate saturation). For this reason, MN1–2 are implemented with HV n-type vertical DMOSFETs. The main drawback of this choice is that some electrical parameters (e.g., transconductance, matching) are worse than standard LV n-type devices. An alternative solution involving LV input MOSFETs, protected using a similar concept as the one used for the active load, was considered but ultimately discarded due to area occupation. Despite the tradeoff of using a DMOSFET-based input pair with limited control over area (due to fixed channel length of DMOSFETs) and bias current (due to power budget constraints), the design achieves a random offset below 0.5-mV rms (assessed with Monte Carlo simulations over process and mismatch). This offset is considered acceptable for the application as it is lower than the offset of the DAC that provides the voltage reference to the regulator.

MN1–2 have a width of 500 μm, while their length is fixed by technology. The protection p-type DMOSFETs also have fixed channel length and a width of 40 μm. The active load has dimensions (in μm) of 4800:1 and the second gain stage (MP5) of 800:0.35. The input pair is biased with 370 μA and the second stage with 160 μA, with a total current consumption of 730 μA (35 mW at 48-V supply).

The regulator can be disabled by the shutdown block (light blue), which sinks the bias current of the error amplifier if the ENABLE signal is above the MN12 threshold. Transistors MN11–13 implement the default condition (off) when the ENABLE is pulled to ground, without requiring an additional power rail apart from the HV one. MN11 is used as a voltage-limiting element, similar to MP3–4 of the error amplifier, with VBIASL set to 2–3 V above ground. An off-chip 10-MΩ resistor is connected to PULLUP. The OVRTMP signal from the overtemperature protection circuit functions in a similar manner to the shutdown circuit. The default state of the regulator (off) is also granted by MP7, which pulls the output of the error amplifier to the HV rail when the bias current is interrupted by the shutdown block. The pull-up is weak (100 nA) compared with the bias current of the second stage (160 μA) and does not interfere with normal operation.

Diodes D1–5 ensure that no sensitive nodes are driven below (above) VBIASH (VBIASL) by more than a diode drop due to leakage of OFF-state voltage-limiting DMOSFETs.

The output pass element of the LDO regulator is a p-type HV DMOSFET (MP16, magenta block) made up of 80 fingers, with a total width of 2000 μm.

The overcurrent protection circuit (yellow block) operates by mirroring the output current with a 1:80 ratio (MP8) and then comparing the voltage drop of the mirrored current (developed over the internal resistor R2, 700 Ω) with the threshold voltage of transistor MN7. If the output current exceeds approximately 55 mA, MP9 and MP10 pull up the output of the error amplifier, causing the regulator to enter a regime of constant output current.

The output current measurement (OCM) circuit (dark blue block) follows a similar concept by mirroring (i.e., attenuating) the output current with a 1:40 ratio (MP11), then a 1:1 ratio (MN9-10), and finally a programmable (with RANGE pin) 1:1 or 1:20 ratio (MP12-13/14), achieving a total attenuation ratio of 1:40 or 1:800. The mirrored output current can be converted

into a voltage with an external resistor of the desired value and read with an external ADC. The final p-type mirroring stage is powered by an LV power rail (VCC), the same as the ADC.

Voltages VBIASH and VBIASL can either be internally generated using a series of diode-connected MOSFETs or be applied externally by using a voltage divider between the HV rails. The former method is preferred as it ensures more stable voltages when changing the input HV supply, thereby providing a wider input supply range.

The ALDO2 uses the standard technique for LDO stabilization with an external low-ESR tantalum capacitor connected to the output node [11]. Polymer tantalum capacitors do have the required radiation hardness [12], but are limited in terms of voltage rating (50 or 63 V), capacitance (below 10 μF), and ESR (about 100 mΩ). The design had to cope with these constraints.

The dominant pole of the LDO is the one at the output node, determined by the output capacitance (few μF) and the output resistance, which consists of the parallel combination of the output pMOS R_{DS} (9.7 kΩ), the feedback resistors (about 200 kΩ), and the load resistance (1 kΩ in the worst case). Its frequency thus ranges between 10 and 100 Hz. With a loop gain of 83 dB, the unity-gain bandwidth (UGB) is about 500 kHz.

The second pole in the feedback loop is at the output node of the error amplifier (gate of MP16). The capacitance at that node is 5.5 pF, the output resistance is 100 kΩ, and the pole frequency is 290 kHz (smaller than the UGB). However, the low-ESR capacitor stabilizes the loop by introducing a zero at a frequency of $1/(2\pi C_O R_{ESR})$. The selected capacitor (Kemet T521, rated 50 V, 1.8-mm thick) has C_O of 10 μF and R_{ESR} of 90 mΩ, resulting in a zero at 180 kHz, which cancels the second pole in any operating corner. Other poles are well above the UGB.

When the overcurrent protection is engaged, a local loop from MP8 to MP10 is also active. C1 and R1 (3 pF and 3 kΩ) compensate the regulator in this condition.

The rms noise (1 Hz–10 MHz) of the HV LDO is 370 μV, with the dominant contribution at the typical maximum load (20 mA) originating from the input pair. It is important to note that due to the relatively high gain of the regulator (30–50 V/V), the contribution of the DAC noise can be even more significant. Therefore, ensuring proper design of the DAC, along with adequate *RC* filtering, is essential for optimal performance.

The power supply rejection (PSR) is better than -70 dB from dc to 1 kHz, thanks to the high loop gain of the regulator. It reaches a minimum of -28 dB at 200 kHz, where the path through the gate capacitors of the pMOS pass transistor becomes most relevant.

B. Experimental Measurements

The performance of the ALDO2 ASIC has undergone comprehensive laboratory qualification across various operating conditions (input and output voltages, load, temperature, etc.). Preliminary measurements have been previously presented [13].

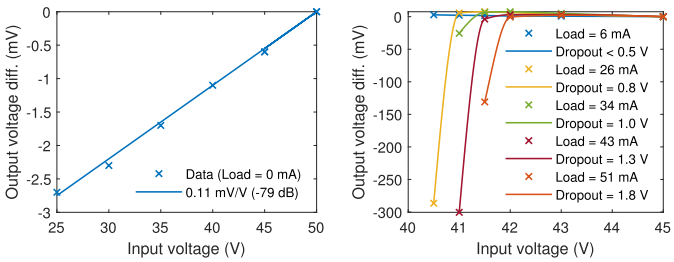

Fig. 5. Line regulation (dc PSR) with no output load and output voltage set at 20 V (left). Measurement of the minimum dropout at different loads with the output voltage set at 40 V (right).

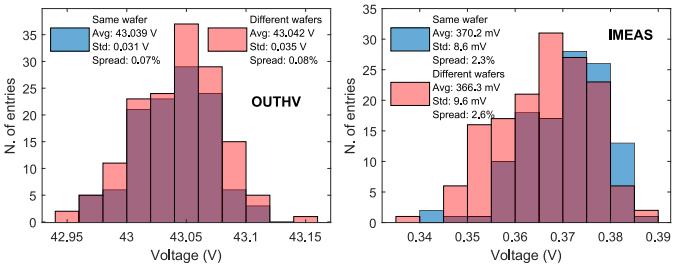

Fig. 6. Distributions of the HV regulator output voltage (OUTHV, left) and OCM (IMEAS, right) for 117 chips on the same wafer (blue) and 152 chips randomly picked from eight different wafers (red).

In Fig. 5, the left plot depicts the line regulation (dc PSR) measurement with no load current aside from that through the feedback network (100 μA) and the output voltage set at 20 V. The measured value of -79 dB matches the simulation. The plot on the right shows the measurement of the minimum dropout, ranging from below 0.5 V at 6 mA load to 1.8 V at 51 mA. The ALDO2 achieves a load regulation of 0.015% (6 mV change at 40 V output) with a load current step of 20 mA, or 7.5 ppm/A.

The left plot of Fig. 6 shows that the rms spread of the output voltage is 0.07% (0.7-mV input-referred), highlighting that the contribution of the error amplifier (due to offset and finite gain) is negligible compared with the spread of the feedback resistors and DAC, which are typically 1%. The two distributions represent samples of chips from the same wafer (blue) or randomly picked from different wafers (red). No appreciable difference was measured between the two. The histograms on the right plot show the spread of the OCM output (with 20 mA load), amounting to 2.6% in samples from different wafers.

Fig. 7 presents the characterization of the OCM circuit. The left plot shows the output current as a function of the output voltage with no load apart from the feedback resistors, exhibiting excellent linearity, as expected for a resistive load, and matching the ideal curve (black). The range of the circuit is set to low (1:40 ratio). The right plot demonstrates a practical application of the OCM circuit, measuring the *I*–*V* curve of an irradiated SiPM with an ADC. The measured value is the sum of the feedback current and the dark current of the SiPM. This property can be used to further calibrate the OCM circuit when radiation damage accumulates and possible drifts occur. By setting an output voltage lower than the breakdown of the SiPM, in fact, the only output current is due to the

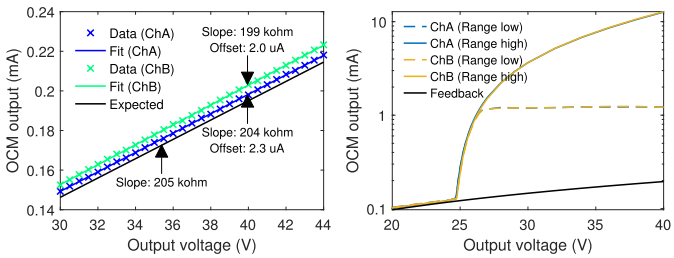

Fig. 7. OCM characterization with only feedback resistors, low range (left). ChA and ChB refer to the two regulators within the same chip. The slope measured by the two regulators (199 and 204 kΩ) matches within 2.9% from the expected value (205 kΩ). Feedback resistors have 0.1% tolerance. OCM characterization with irradiated SiPM (SensL MicroFC), low range (dashed line), and high range (solid line) (right). The low range saturates just above 1 mA.

feedback, which is fixed and known from the value of the feedback resistors and of the output voltage (both not changing with radiation damage).

Noise measurements have confirmed the simulation results, indicating 350-μV rms noise at the typical maximum load.

IV. Low-Voltage Section

The low-voltage section of ALDO2 comprises the two LDOs (primary and aux), the protection circuits, and the bandgap voltage references.

A. Low-Voltage LDOs

The two LV regulators (0.8-A and 20-mA ones) share identical designs, differing only in the width of output p-type MOSFET (the length is 0.35 μm). The high-current LDO features a 32-mm-wide one, while the low-current LDO has a 1-mm-wide one.

The complete schematic of the high-current regulator is presented in Fig. 8. The error amplifier (green block) is a single-stage nMOS-input opamp with a mirrored topology and a gain of 44 dB. The use of an n-type input pair is essential as the error amplifier needs to accommodate all the three types of bandgaps, each with different output voltages (1.2 V for the BJT-based ones and 0.63 V for the MOS-based one), while minimizing the input voltage (which can be as low as 1.5 V if the required load is moderate, i.e., below 200 mA). A p-type input pair would not be suitable with BJT-based bandgaps, as V_{gs} of the input pair would be below 300 mV at 1.5-V supply. This compromise, although mandatory, results in increased overall noise (due to the higher flicker noise of n-type devices) and worse matching when the regulator is used with the DTMOST-based bandgap (due to the operation of the input pair in moderate inversion). The input pair (MN1–2) has a size of 1000:0.7, MP1–2 of 2000:5, MP3–4 of 1000:5, and MN3–4 of 1000:2 (sizes in μm). The mirrored topology provides a larger output swing of the error amplifier toward the ground rail, and thus larger overdrive capability for the output pMOS transistor.

The regulator can be externally disabled (light blue block) by pulling down the EN input. The overtemperature protection (not shown) also operates in the same way. The overcurrent protection circuit (yellow block) features a similar architecture

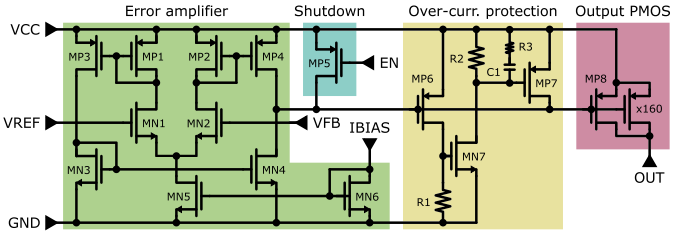

Fig. 8. Full schematic of the LV regulator. All MOSFETs have the substrate connected to their source.

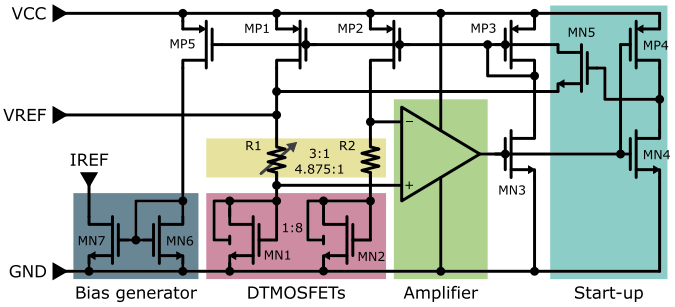

Fig. 9. Schematic of the DTMOST-based bandgap. The BJT-based ones are identical, except for the resistor array, which is not trimmable. All MOSFETs have the substrate connected to their source (except MN1–2). VREF node is the output of the bandgap.

as the HV one, but with the R2 resistor (40 kΩ) instead of a p-type mirror and adopting a different compensation scheme (C1 2.4 pF, R3 10 kΩ). The sense resistor R1 is 200 Ω.

Both the LV regulators are stabilized with external tantalum capacitors. In the case of the high-current regulator, the gain of the error amplifier is lower (44 dB) than the HV counterpart, and the gate capacitance of the 32-mm-wide pass transistor is significantly higher (45.4 pF). At the maximum output current, the output impedance of the amplifier is 220 kΩ, placing the second pole at 16 kHz. The combination of C_O and R_{ESR} must introduce a zero approximately in the same range (e.g., 10 μF and 250 mΩ or 100 μF and 25 mΩ). The availability of LV tantalum capacitors is much larger than the HV ones, so the specific model selection is not critical in this case.

B. Bandgap Voltage Reference

Fig. 9 shows the schematic of the DTMOST-based bandgap, which adopts the modified Kuijk's topology presented in [14]. MN1–2 (red block) are the DTMOSTs used for generating the PTAT/CTAT voltages. MN1 is sized 570:0.7 (in μm), while MN2 is eight times larger. Unlike most CMOS technologies, I3T80 permits the implementation of DTMOSTs using n-type devices within isolated P-wells. This feature is advantageous for radiation hardness due to the utilization of hardened layout for n-type devices, as discussed in Section VI.

The resistor pair (yellow block) uses an array of matched polisilicon resistors. The ratio of R1/R2 is externally trimmable to compensate for wafer or device spread, ranging between 4.875:1 and 3:1 with 4 bits (0.125 LSB). The amplifier (green block) is a dual-stage compensated pMOS-input opamp. The current mirrors that bias the DTMOSTs also generate the current reference (dark blue block) used in other parts of the LV section.

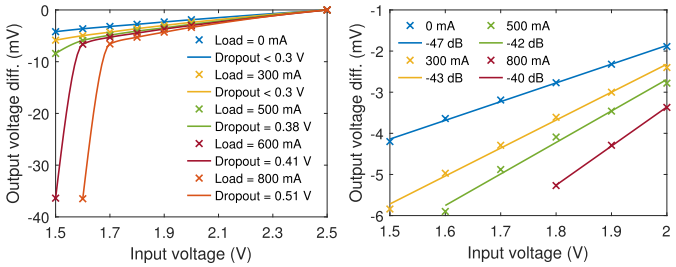

Fig. 10. Measurement of the minimum dropout at different loads and output voltage set at 1.2 V (left). Zoom of the previous plot above the minimum dropout and measurement of the line regulation (dc PSR) (right).

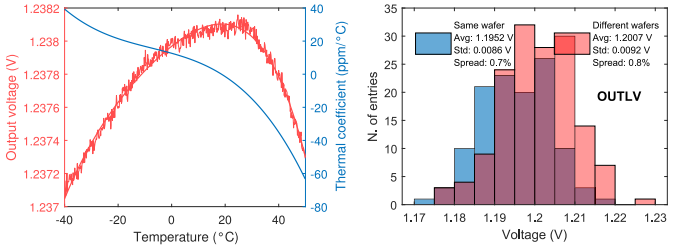

Fig. 11. Temperature drift of the LV LDO while using DTMOST-based bandgap (left). This measurement is performed on an irradiated chip so the measurement stops at 50 °C to prevent annealing (which is already clearly visible above 25 °C, when the curvature abruptly changes). Distributions of the LV output voltage for 117 chips on the same wafer (blue) and 152 chips from eight different wafers (red) (right). All devices have the same bandgap trimming.

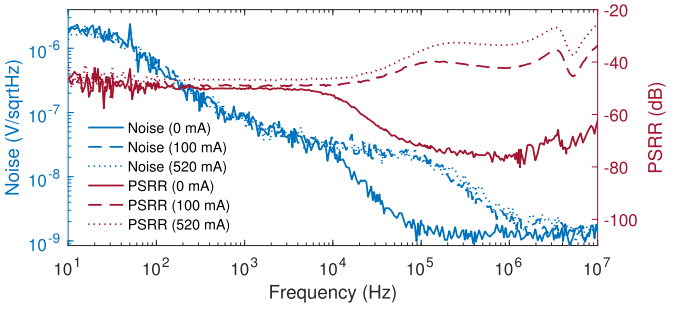

Fig. 12. Noise (left axis) and PSRR (right axis) of the LV regulator at different output loads. Input and output voltages are 1.8 and 1.2 V, respectively.

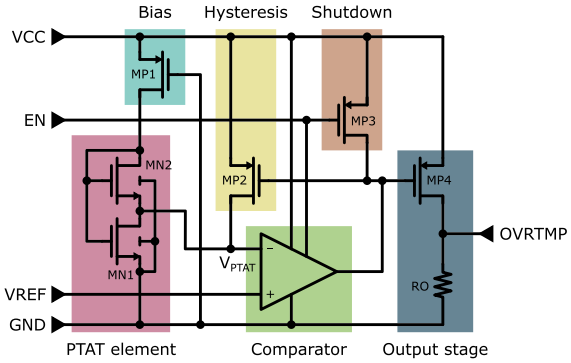

Fig. 13. Schematic of the overtemperature protection circuit. The comparator is a simple p-type-input opamp in open-loop configuration.

The bipolar-based bandgaps, either NPN and PNP, share most of the design, but the resistor pairs are not trimmable.

C. Experimental Measurements

Fig. 10 presents the measurements of the minimum dropout (left plot) and line regulation (right plot) at different loads. The minimum dropout is defined as the dropout at which line regulation gets worse than −34 dB. At the typical load of 500 mA, the minimum dropout is 0.4 V and the line regulation above that is −42 dB (8 mV/V). The load regulation is 5 mV/A (0.42%/A with 1.2-V output), evaluated using a current step of 0.5 A.

Measurements of the bandgaps' thermal stability indicate that PNP-based one performs better than the others, exhibiting a maximum drift of 20 ppm/°C in the temperature range from −40 °C to 80 °C. The DTMOST-based bandgap displays a maximum drift of 50 ppm/°C after trimming, due to the higher quadratic slope. The NPN-based one performs worse than expected, with a drift of about 120 ppm/°C. The thermal drift at the output of the regulator is dominated by the contribution of the bandgap and no other effects are introduced by the error amplifier. The left plot of Fig. 11 shows the drift and thermal coefficient of the ALDO2 LV output voltage when the reference is provided by the DTMOST-based bandgap.

The right plot of Fig. 11 presents the distribution of the output voltage within the same wafer (blue data) or between different wafers (red data), highlighting an rms spread of 0.7% and 0.8%, respectively. All these samples adopted the same trimming configuration of the bandgap.

Fig. 12 shows the measurement of the noise at the output of the regulator (left axis) at different output loads. The rms noise at 500 mA is 27 μV (integrated from 10 Hz to 100 MHz). The PSR measurement (right axis) shows that ALDO2 is capable of rejecting input supply noise better than −40 dB up to 50 kHz and better than −26 dB up to 10 MHz.

V. Overtemperature Protection Circuit

The overtemperature protection circuit is shown in Fig. 13. Unlike other solutions that use a differential or ratiometric temperature sensor to compensate for process variation and radiation effects [15], [16], the one adopted in ALDO2 uses the weak inversion "composite" MOS topology (MN1–2, red block) [17], which provides a PTAT voltage that remains independent of any technology or working parameter (e.g., V_{TH}, I_{DS}) as long as MN1 and MN2 are operated in the weak inversion region and neglecting second-order dependencies on source–drain and source–bulk potential. The PTAT voltage is defined by the following equation:

$$V_{PTAT} = \frac{kT}{q} \ln\left[\frac{(W/L)_{MN2}}{(W/L)_{MN1}}\right]. \quad (1)$$

The independence from technology parameters is anticipated to be advantageous for radiation hardness, as these parameters (e.g., V_{TH}, carrier mobility) change as TID accumulates.

MN1 and MN2 are sized with a channel length L of 1 μm to minimize short-channel and mismatch effects, and an aspect ratio W/L of 20 and 4980, respectively. The devices are

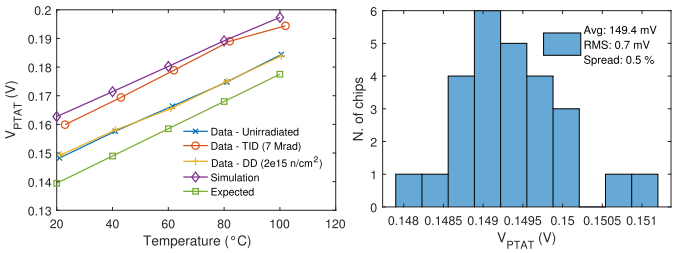

Fig. 14. Temperature sensor voltage (V_{PTAT}) as a function of temperature for the expected case from (1), for simulation and for measured chips (unirradiated and irradiated with TID and neutrons) (left). Distribution of V_{PTAT} in 26 chips at ambient temperature (right).

arranged in a matrix (25 × 10), with MN1 at the center, further minimizing mismatches and thermal gradients. The composite MOS device is biased by MP1 with 600 nA, resulting in a power consumption of approximately 1.1 μW at 1.8-V supply. The expected V_{PTAT} from (1) is 143 mV at 27 °C, with a thermal slope of 476 μV/°C. Simulations in the nominal corner give a PTAT voltage of 166 mV and a slope of 435 μV/°C. Monte Carlo simulations over process and mismatch give a spread of 1.2 mV rms (0.7%). The difference between the simulated and theoretical values can be explained by the choice of operating the composite MOS device in a region closer to moderate inversion for radiation hardness concerns. If the bias current of the composite MOS is lowered to about 10–30 nA, the simulation agrees with the theoretical value within a few millivolts.

The PTAT voltage is then compared with an external threshold by a comparator (green block). MP2 provides a hysteresis of 140 nA, which corresponds to 8.7 mV, or 18 °C. The overtemperature protection can be deactivated by pulling down the EN pin.

Direct measurements of V_{PTAT} are not possible since the voltage is not available outside of the chip. An indirect measurement was performed by operating the chip in a climatic chamber at different temperatures and decreasing the comparator threshold with a DAC, until the regulator would switch off. This measurement, thus, includes offsets and other nonidealities of the comparator itself. The results are presented in Fig. 14. The left plot shows V_{PTAT} versus temperature for the expected case from (1), and for simulated and measured (unirradiated and irradiated) chips. The measured slope is (450 ± 8) μV/°C. Neutron irradiation (up to $2 \cdot 10^{15}$ $\mathrm{n_{eq}/cm^2}$) does not affect the temperature sensor, while a 7-Mrad TID causes a shift of about 10 mV (+22 °C), but no change in the temperature slope. On the right, an histogram of V_{PTAT} measured in 26 chips shows a good uniformity of 0.5% rms, confirming the results of Monte Carlo simulations.

Thermal measurements with an infrared camera showed that protection kicks in at 105.4 °C (comparator threshold at 189 mV) and then keeps the chip at 96.6 °C, confirming that the hysteresis is 17.6 °C (assuming a linear heating–cooling profile).

The excellent uniformity and only moderate sensitivity to TID prevent any need of calibration or adjustment of the threshold during the operation of the chip in the detectors.

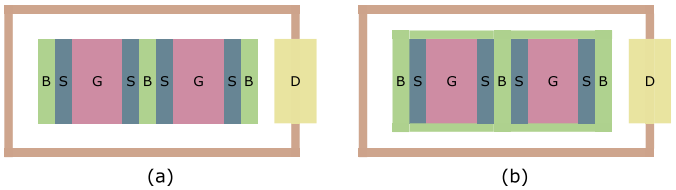

Fig. 15. Top view of (a) standard and (b) radiation-hardened layout of the HV vertical n-type DMOSFET. The bulk P+ diffusion (B, green) surrounds the device and prevents the thick oxide from facing the top and bottom edges of the source diffusions (S, dark blue).

VI. Radiation Hardening Techniques and Layout

To reduce the sensitivity to radiation-induced threshold voltage shifts and attain the required radiation hardness, weak inversion and subthreshold operating regions were avoided in the whole design, with the exception of few components such as the DTMOSTs used in the bandgap (operating necessarily in weak inversion to get the required exponential I–V slope) and the input pair of the LV error amplifier (operating in moderate inversion as discussed in Section IV-A). Neither of these two circuits, however, proved to be excessively affected by the radiation levels required, as shown later in Section VII.

The I3T80 technology is not radiation-hardened on its own and requires specific hardening techniques in the layout of the chip. All the regular LV n-type transistors use the enclosed layout (annular gate) [18], where the channel does not interface with any thick oxide (grown with the LOCOS process). Moreover, the HV n-type vertical DMOSFETs adopt an original modified layout, as illustrated in Fig. 15. An additional P+ diffusion (bulk contact, in green) surrounds the device, preventing the thick oxide used by spacers and passivation from facing the top and bottom edges of the source (in dark blue). This solution effectively reduces the leakage between drain and source resulting from the TID-induced accumulation of charges in the thick oxide. The ELT-like structure as the one adopted in this work was suggested in [4], although the actual implementation was not disclosed.

Additional hardening solutions implemented in the design of ALDO2 include the use of abundant wells and bulk contacts, as well as guard rings, aimed at efficiently removing any charge deposited in the substrate and reducing the risk of single-event effects (SEEs) (transients and latch-ups).

Being a power device, particular attention was also dedicated to controlling the maximum current density and minimizing the series resistance of high-current metal traces. Traces were sized with large overprovisioning (over three times the I3T80 rules). No power integrity software (e.g., Cadence Voltus) was used for this purpose.

Dummy structures and interleaving techniques are used in all the devices where matching is critical, except for DMOSFETs, as the penalty in area would be too large.

VII. Radiation Hardness Qualification

The chip's radiation hardness underwent comprehensive testing in several laboratories (including CERN and Karlsruhe for TID irradiation with X-rays, Ljubljana and Pavia for displacement damage irradiation with neutrons, and Legnaro for SEE irradiation with heavy ions).

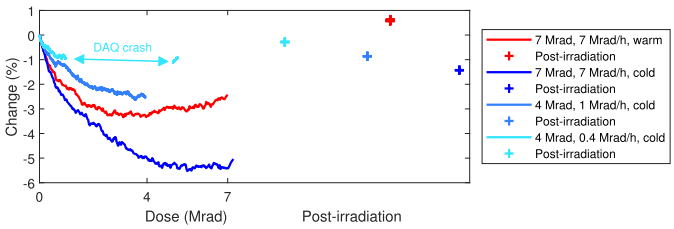

Fig. 16. Online monitoring of the LV output during TID irradiation at different dose rates and temperatures. The red curve is taken at high dose rate (7 Mrad/h) and 30 °C. Blue curves are taken at 0.4, 1, and 7 Mrad/h at −30 °C. Postirradiation data (cross markers) are taken after three days at ambient temperature.

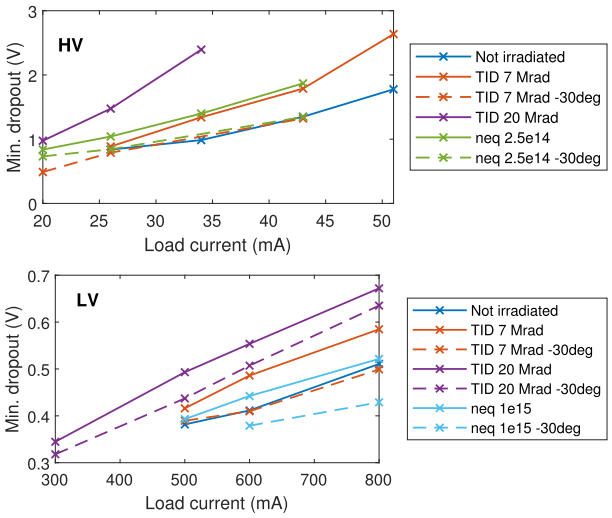

Fig. 17. Minimum dropout as a function of load current of the HV regulator (top) and LV regulator (bottom) for chips irradiated with X-rays and neutrons. Dashed lines are measurements performed at the operating temperature (−30 °C).

The targeted radiation levels correspond to those encountered by the chip in the most demanding detector (CMS BTL), specifically 3.2-Mrad TID, 1.9×10^{14} cm^{-2} 1-MeV-equivalent neutron fluence, and 1.5×10^{13} cm^{-2} charged hadron fluence.

The TID radiation hardness of certain CMOS technologies can be sensitive to irradiation temperature, especially at the low temperatures experienced in particle physics experiments, and dose rates [19]. Previous studies on onsemi I3T80 (made by CERN for the FEASTMP DCDC) confirm this observation for the technology used by ALDO2. Consequently, the X-ray irradiation for TID was conducted at both ambient and low temperatures, and varying the dose rate.

Fig. 16 presents the data of the online monitoring of the LV output during TID irradiation (using DTMOST-based bandgap) up to 4 and 7 Mrad. A comparison between the red data (7 Mrad/h, 30 °C) and the dark blue data (7 Mrad/h, −30 °C) clearly reveals that the output voltage change is significantly greater (almost double, 5% versus 3%) for the chip irradiated at low temperature. A similar difference persists even after annealing at ambient temperature for three days (cross markers). The impact of dose rates at fixed temperature (blue data, from 0.4 to 7 Mrad/h) is even more pronounced, with lower dose rates resulting in less output voltage change (<1%) both during irradiation and after annealing.

TID irradiation does not significantly affect the temperature drift of the bandgaps.

The effects of TID on the HV regulator have a similar trend to the LV one shown in Fig. 16, but the change is smaller (<0.2%). The OCM circuit within the HV section is the most affected part, with a measurement change up to 10% at 7 Mrad (twice the maximum radiation level expected in the working environment). However, as discussed in Section III-B, the OCM circuit can be easily recalibrated by measuring the output current through the feedback network. The lower radiation sensitivity of the HV LDO with respect to the LV LDO is mainly due to the fact that the HV one uses an external reference, while the LV one uses the internal bandgap (which gives the dominant contribution).

The most relevant ALDO2 performance changes due to TID and neutron irradiations concern the line regulation and the minimum dropout. Both types of irradiation diminish the output current capability of the HV and LV regulators at a given input voltage due to an increase in the on-resistance of the pass transistor, necessitating the use of higher dropout to maintain adequate line regulation and supply rejection. Fig. 17 shows the minimum dropout as a function of load current at different radiation levels and working temperatures. In this test, all irradiations were conducted at ambient temperature. Operating the irradiated chips at low temperature (dashed data), when the on-resistance of the pass element is lower, allows for the nearly complete restoration of the performance of the unirradiated chip (solid blue data) for both the HV and LV regulators, with the exception of the chip irradiated at 20 Mrad. The impact of displacement damage from a neutron fluence of 10^{15} n_{eq}/cm^2 (five times above the expected levels) results in an increase in the on-resistance of the pass element of the HV regulators, reaching up to 500 Ω. This increase subsequently limits the output current to a maximum of 10 mA and cannot be fully recovered by operating the chip at low temperature.

Another part of the ALDO2 that is potentially sensitive to radiation damage is the VBIASH and VBIASL internal generation circuit described in Section III-A, which makes use of diode-connected MOSFETs sensitive to threshold voltage drifts. There is indeed a significant drift of the voltages generated by this block, up to 700 mV, but this remains low enough to ensure the operation of ALDO2 at the radiation levels required and with an input voltage range of approximately 1:1.6 (e.g., 32–50 V).

Among the three bandgaps included in the ALDO2, the DTMOST-based one was deemed the most suitable, as it offers the best compromise between thermal stability and radiation hardness, with changes in the bandgap voltage below 1.5% at the target radiation levels. Conversely, the PNP-based one exhibits a drift of up to 4% with neutron irradiation and 2% with X-rays.

Finally, SEEs were studied with heavy ion irradiation.

No single-event latchup (SEL) was found after a cumulative fluence of $1.7 \cdot 10^{10}$ ions/cm^2 with linear energy transfers (LETs) between 8.6 and 54.7 MeV cm^2/mg. This allowed for

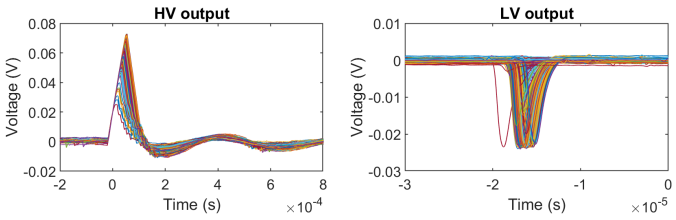

Fig. 18. Data acquisitions with an oscilloscope of SETs. The trigger was set on the HV output (level 20 mV). SETs are synchronous between HV and LV regulator approximately 50% of the triggers. SETs are always synchronous between the two HV regulators.

the computation of a SEL cross section upper limit of $2.3 \cdot 10^{-9}$ cm^2 at an LET of 8.6 MeV cm^2/mg and $1.2 \cdot 10^{-10}$ cm^2 at 28.4 MeV cm^2/mg (following ESA-ESCC 25 100 guidelines and with 68% confidence level). The absence of SELs proved that the radiation hardening techniques adopted, especially the extensive use of guard rings and wells contacts as discussed in Section VI, are sufficient for the target radiation levels.

Single-event transients (SETs) were observed, as shown in Fig. 18. The sensitive circuit was identified in the overtemperature protection, which triggers synchronous transients in the three protected regulators (the HV ones and the main LV one). The transients exhibit moderate amplitude and duration (70 mV and 150 μs on the HV output, 22 mV and 5 μs on the LV output). Introducing an external filtering capacitor on the comparator threshold (VREF node in Fig. 13) significantly reduced the rate of SETs by almost two orders of magnitude. The cross section with this mitigation in place is $2.1 \cdot 10^{-7}$ cm^2 at an LET of 28.4 MeV cm^2/mg. Due to limited beam time availability, it was not possible to measure the full Weibull curve of the SET cross section as a function of LET. Nevertheless, even assuming a very conservative threshold LET of 1 MeV cm^2/mg, the SET cross section with protons would be $4.6 \cdot 10^{-12}$ cm^2 (computed from the heavy ion cross section as discussed in [20]), translating to 10.3 SETs per year per chip in the region of the BTL detector closest to the endcaps. Considering also the amplitude and duration of the observed SETs, this amount is well within acceptable limits. Other on-silicon mitigation techniques (possibly even more effective) could not be implemented since SETs were observed at a stage where chip design was already finalized and a further tape-out was not compatible with the detector schedule.

VIII. Production Yield, Reliability, and Chip Testing

The ALDO2 chip was designed complying with most of the design-for-manufacturing (DFM) and all the DRC rules suggested by onsemi to maximize the yield.

A random sampling of the devices from eight of the 26 wafers allowed for the estimation of a high yield of 99.5% (98.7%–99.8% with C.L. 90% [21]). It should be noted that the yield measurement was conducted using a chip socket, which could damage the chip if critical pins are not properly contacted, potentially worsening the measured yield.

The aging of the chip was tested in an accelerated environment, involving 700 h at 90 °C and 240 h at −55 °C, with no failures observed in the tested sample.

The exceptional yield and reliability of ALDO2, along with the very high uniformity demonstrated in Sections III-B and IV-C, have made it possible to skip individual chip testing prior to PCB mounting, as there is no need for individual trimming, neither across wafers.

IX. Summary and Future Prospects

This article presented the ALDO2 ASIC, a multifunction, radiation-hardened power management solution designed for SiPM-based particle physics detectors.

The chip has been manufactured in the required quantities for the BTL and HGC detectors of the CMS experiment at CERN (45 k chips) and, at the time of writing this article, is about to being assembled on the final PCBs of the front-end boards.

Due to ALDO2 unique features and characteristics (e.g., operation up to 70 V, radiation hardness above few Mrad of TID, and 10^{14} n_{eq}/cm^2 of neutron fluence), direct comparison with other state-of-the-art solutions is not feasible.

Considering the anticipated increase in the utilization of SiPMs in particle physics experiments, there exists the potential for further enhancements of the chip, incorporating additional functionalities. The design of ALDO3 should initiate with the selection of a different technology, since I3T80 from onsemi is becoming outdated and the fabrication facility used for the production of the chip and qualified for radiation hardness has ceased operations. Valuable improvements to the chip design could include the integration of digital circuits (e.g., DAC, ADC, I–V curve measurement logic), as well as the adoption of a capacitor-less compensation scheme for the HV regulators, which would circumvent the large PCB area currently occupied by HV tantalum capacitors.

Acknowledgment

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