PCIe 5.0 Connector Distributed Physical-Based Circuit Model With Loading Resonances for Fast SI Diagnosis and Pathfinding

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***Abstract*— We report on the development of a fast signal integrity (SI) diagnosis and pathfinding tool for a Peripheral Component Interconnect Express (PCIe) 5.0 connector based on the distributed physical-based transmission line (dPBTL) circuit model. Frequency-dependent loading resonances due to add-in card (AIC) and baseboard (BB) are identified via HFSS field simulation and analysis. The subcircuit models for ground-cavity (GC) and stub-effect resonances are established and matched well with the field simulated. The integrated dPBTL accurately predicts differential-mode performances and resonant crosstalk up to 64 GHz, speeds up simulation by 5000×, and reduces data storage by 4.84 × 10^6 compared with the traditional full-wave approach. Fast-guided and evaluated by 1-D dPBTL, design modifications reduce loading resonances and broadband dispersion, meeting PCIe 6.0 S-parameter requirements. Informed by dPBTL design, the 3-D pathfinding PCIe 6.0 connector demonstrates a 700% eye height (EH) enlargement and 150% eye width (EW) improvement at 64-GT/s non-return-to-zero (NRZ). Average 14% and 35% are improved in EH and EW for the three eyes at 64-GT/s (32-GBaud) PAM4. Furthermore, eye-openings at 128- and 144-GT/s PAM4 support further development toward PCIe 7.0 applications.**

***Index Terms*— 5G, connectors, crosstalk, equivalent circuits, peripheral component interconnect express (PCIe), resonance, signal integrity (SI), transmission lines.**

I. Introduction

PERIPHERAL Component Interconnect Express (PCIe)-based interconnects and architecture are featured by their ever-increasing high-speed data rates, low latency, scalability, wide adoption, and support of advanced technology such as NVMe storage and high-performance GPUs, enabling artificial intelligence (AI), machine learning (ML), and cloud computing on 5G and 6G. Since its inception in 2003, PCIe has evolved from 2.5 GT/s in version 1.0–32-GT/s non-return-to-zero (NRZ) in PCIe 5.0 by 2019 [1], [2], [3], [4]. PCIe has been advanced to 64- and 128-GT/s pulse amplitude modulation with four levels (PAM4) for the next generations (6.0 and 7.0) since 2021 [5], [6]. Traditional design methods for connectors, which primarily rely on full-wave electromagnetic (EM) simulations using the finite element method (FEM), have become increasingly time-consuming and computationally demanding. This is due to the significantly increased mesh density required to resolve the reduced wavelengths at higher frequencies accurately. Besides the traditional impedance control, the need to address loss and crosstalk in signal integrity (SI) diagnosis exacerbates the challenge in design cycle time during the process of scaling up bandwidth. Turnaround time is prolonged by n times with n iterations of designs of experiments (DOEs) to meet all specifications (specs) or n variations in pathfinding for the next generations with more critical requirements. The transition from NRZ to PAM4 adds further complexity due to reduced tolerance to noise and intersymbol interference (ISI).

While traditional mathematical-based modeling quickly generates matrix solutions, it often lacks the ability to provide detailed physical insights and localized diagnosis within the device under analysis (DUA) [7]. The equivalent physical-based model (PBM) presents a promising solution for fast SI diagnosis and facilitating quick pathfinding. The PBMs complementing commercial FEM simulators, such as HFSS, SIwave, and EMPro, efficiently characterize the performances of the DUA by abstracting complex EM phenomena into scalable physical-based circuit elements. This simplified approach facilitates straightforward design optimization and system integration with significantly reduced iteration time. Effective 1-D circuit transformations of 3-D connectors, including SMA, pin-in-socket, and pad-on-pad types, have been demonstrated in prior studies [8], [9], [10], [11], [12]. However, modeling high-speed multichannel connectors remains challenging due to their structural complexity, long electrical length, and the need for high-frequency, wide-bandwidth accuracy, which demands substantial computational resources for generating models comprising hundreds of lumped RLGC segments [10], [11].

Transmission-line-based PBMs abstract traditional distributed-RLGC-based PBMs by representing a uniform 3-D section as a physical-based transmission line (PBTL) with effective parameters including characteristic impedance and complex propagation constant over its effective length. When

Received 24 July 2024; revised 21 September 2024; accepted 8 October 2024. Date of publication 29 October 2024; date of current version 7 January 2025. This work was supported by Foxconn Interconnect Technology. *(Corresponding author: Milton Feng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2024.3479132.

Digital Object Identifier 10.1109/TMTT.2024.3479132

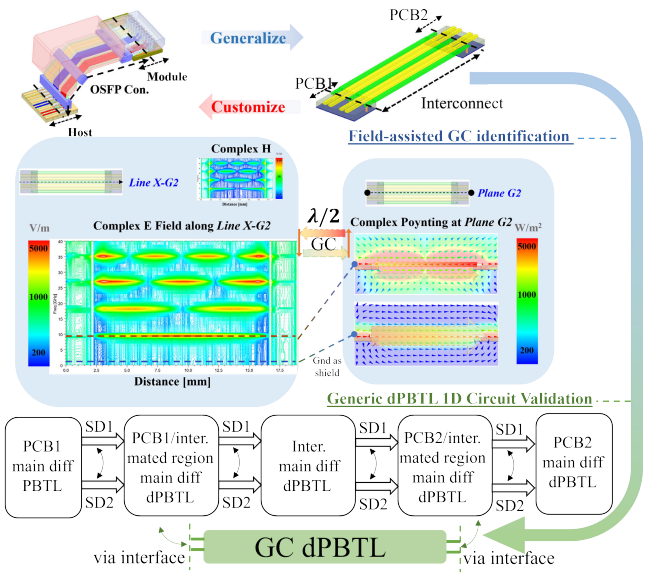

Fig. 1. Workflow diagram of dPBTL transformation and validation based on EM field-assisted GC identifications on a simplified pseudoconnector [13], [14].

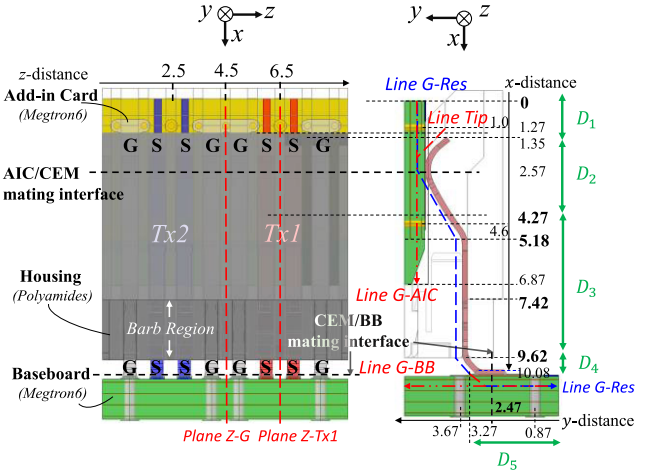

Fig. 2. Two-channel PCIe 5.0 CEM mated with AIC and BB as DUA, shown in front view and side view. Monitor lines and planes for field analysis are labeled. Locations of importance are annotated along the x-, y-, and z- directions. Units are all in mm. The domains (Di, $i = 1$ to 5) for section analysis and PBTL parameter extraction are labeled.

interconnected in cascaded or shunt configurations along the transmission path, PBTL segments form a distributed PBTL (dPBTL) subsystem for a nonuniform 3-D section. A 3-D connector DUA is modeled by a dPBTL system, integrating these subsystems. This advanced method provides a more straightforward diagnosis of impedance discontinuity, material nonuniformities, dispersion, and losses while enabling flexible sectional decomposition for localized SI diagnosis. Parameterization of each PBTL segment further supports local variations for fast pathfinding.

In [13], a preliminary dPBTL circuit system was introduced for the PCIe 5.0 Card Electromechanical (CEM) connector, effectively modeling unmated/mated conditions with distributed and dispersive features along the differential pairs up to 64 GHz. However, there are some oversimplifications. The extraction of effective loss tangent was overestimated due to the neglect of the conductor loss term in overall attenuations. The modeling of periodic high-Q crosstalk resonances in multiple sets of lumped RLC resonators lacked a physical-based explanation. These high-Q crosstalk resonances, along with sharp reductions in insertion loss (IL) and spikes in return loss (RL), have been correlated with multiple ground-related features, including the placement of ground return vias, ground return paths, and the length of the ground–signal–signal–ground (GSSG) channel [14], [15], [16]. Recently, we established a thorough and generic field diagnosis methodology using simplified 2xGSSG pseudoconnectors [17]. The generic diagnosis workflow with simple ground-cavity (GC) followed by dPBTL transformation is summarized in Fig. 1. The diagnosis established unique field "fingerprints" of ground-related resonances, distinguishing them from other types of resonances. Specifically, the fingerprints were visualized in fields plotted at monitor planes, fields along and across the interconnect by contourplots, net power, and total stored EM energy in 3-D sections. The fields include electric field (E), magnetic field (H), and complex Poynting vector (S). Thereby, the root cause of the major ground-related resonances was identified as the presence of GCs between two printed circuit boards (PCBs) with insufficient terminations. The longitudinal GC boundary is the ground via at each PCB most adjacent to the mating interface. The lateral GC boundary is loosely defined by the neighboring conductor, typically the signal line in connectors. The idea of GC and its coupling effect to the main differential signal path in the pseudoconnector is validated by a simplified equivalent dPBTL circuit in [18].

Building on this foundation, the field diagnosis methods are adapted to actual multichannel high-speed connectors, which are more structurally complicated, focusing specifically on the PCIe 5.0 connector in this work. The field performances varying along distance and frequencies are abstracted and quantified as multisegmented dPBTL circuits. The loading effects of add-in card (AIC) and baseboard (BB) onto signal paths and GC structures are investigated in field postprocessing and transformed into equivalent dPBTL subcircuits. The accuracy of the dPBTL model is verified by HFSS results in standalone GC, AIC-side, and BB-side subsections, and the full connector with all loaded components. The effectiveness of the dPBTL method in fast design and optimization is demonstrated in assisting pathfinding solutions for PCIe 6.0.

This article is organized as follows. Section II presents a field analysis of the PCIe 5.0 baseline connector, unveiling the underlying mechanisms of S-parameter resonances. Section III details the formulation of equivalent dPBTL models with the presence of loading resonances, illustrating circuit parameter extractions concerning location variation and frequency dependence. Section IV introduces pathfinding designs assisted by dPBTLs, showcasing improved S-parameter and eye-diagram performances for next-generation applications.

II. PCIe 5.0 Baseline 3-D Model and Field Analysis of GC and Stub-Effect Resonances

The two-pair (Tx1-Tx2) CEM connector mated with AIC and BB with extended 1.27-mm differential microstrip feedlines in both boards is shown in Fig. 2. The locations of

TABLE I
HOUSING MATERIAL PROPERTY

	1 GHz	5 GHz	10 GHz
ε_r	3.7	3.6	3.4
$tan\delta$	0.01	0.014	0.016

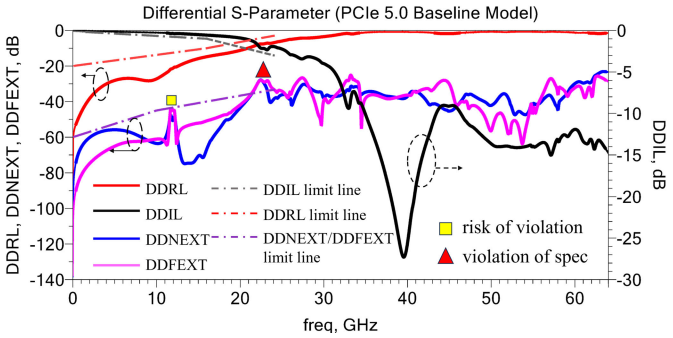

Fig. 3. DD S-parameter results of the PCIe 5.0 baseline model, yielded by HFSS FEM solver. Limit lines are defined in PCIe 5.0 CEM Spec [2].

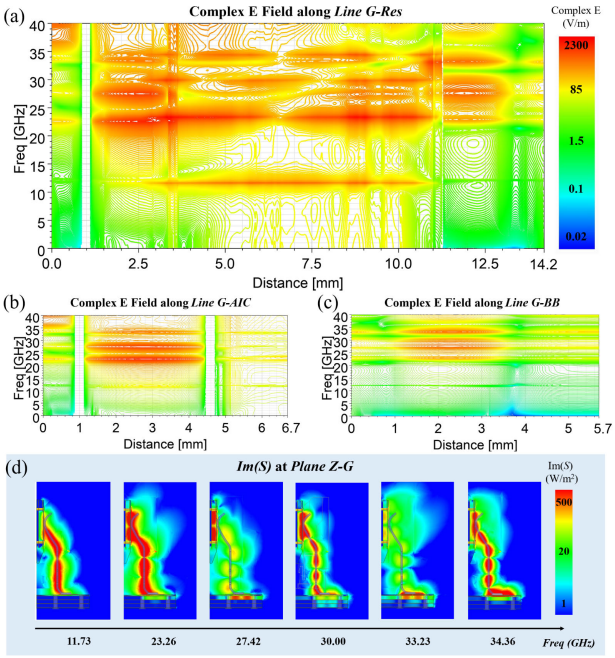

Fig. 4. Contourplots of complex E-field along (a) *Line G-Res*, (b) *Line G*-AIC, and (c) *Line G*-BB. (a)–(c) share the same color-key scale. (d) Magnitude field plots of imaginary Poynting vector Im(S) at *Plane* Z–G at resonant frequencies. Field plots are generated through the HFSS terminal solution. The 1-V incident voltage is applied with 1 V at Tx1 AIC (with 0°/180° phase), while all remaining differential ports are terminated with 85 Ω.

importance along the x-, y-, and z-directions are labeled for later discussion. AIC and BB use Megtron6 as the substrate dielectric material with relative permittivity ε_r of 3.5 and loss tangent tanδ of 0.002. A polyamide thermoplastic material is used as CEM housing material with frequency-dependent ε_r and tanδ defined in Table I by the piecewise linear model in Ansys HFSS [19]. Automatic Djordjevic–Sarkar models are applied to each dielectric object for wideband simulation with Kramers–Kronig conditions satisfied [20].

Differential-differential (DD) S-parameters for the PCIe 5.0 baseline model are obtained using the FEM solver in Ansys HFSS, through driven-terminal analysis with an 85-Ω differential port impedance. Due to the symmetrical 2xGSSG configuration, the Tx1 and Tx2 pairs exhibit identical performances. In all test cases, the Tx1 pair is the victim, and the Tx2 pair is the aggressor. In the data presented in Fig. 3, the AIC-side Tx1 port acts as the victim port, while the AIC- and BB-side ports of Tx2 serve as the near- and far-end aggressor ports, respectively. AIC-side is selected due to its higher risk of spec violation. Limit lines defined by PCIe 5.0 specification (spec) are placed in Fig. 3 [2]. Two types of resonances are observed: 1) wide and deep dip in DDIL at around 40 GHz and 2) sharp but small resonances in all four S-parameter curves including DDIL, DDRL of the aggressor pair, and DD far- and near-end crosstalk (DDFEXT and DDNEXT) between two pairs. While the DDIL remains within the spec limit of up to 24 GHz, its baseline drops due to the wide and deep resonance at 40 GHz. The presence of this resonance limits the scalability of the design for future higher data-rate standards. For DDNEXT and DDFEXT, sharp resonances near 11 GHz approach the spec limit, leaving a narrow design margin that leaves little tolerance for manufacturing variability or operational conditions. Moreover, a clear spec violation is observed around 22 GHz, further underscoring the need for root cause analysis to mitigate these resonances and minimize SI degradation.

As annotated in Fig. 2, a field monitor line *Line G-Res* for resonance analysis is placed under the shared ground lines (at $z = 4.5$ mm) of Tx1 and Tx2 GSSG pairs of CEM, AIC, and BB. It is aligned roughly with the wave propagation direction to diagnose locations and boundaries of resonant structures. The AIC- and BB-side monitor lines, *Line G*-AIC and *Line G*-BB, are placed at $z = 4.5$ mm. Contourplots of electric-field (E-field) complex magnitude along the lines are postprocessed from FEM solutions to provide compact information on the frequency-dependent performances of fields along a specified distance. For clear demonstration, we zoom in to frequency below 40 GHz to diagnose the lower order resonances.

Based on the E-field along *Line G-Res* shown in Fig. 4(a), standing waves are formed along CEM ground pins and loosely guided by neighboring Tx1 Tx2 conductors, indicating the presence of a cavity, i.e., the CEM GC. This weakly confined resonant GC supports wave oscillations when its effective length is $n\lambda/2$, n is an integer greater than 0, and λ is the wavelength. It is worth noting that the spacings of E-field antinodes and nodes are affected by the heterogeneous media with AIC and BB substrates, CEM housing, and air gaps. Multiple orders of CEM GC resonances are observed; however, the ith-order resonant frequency $f_{i,\mathrm{Gres}} \neq f_{i-1,\mathrm{rGes}} i/(i-1)$, $i \geq 2$, indicating nonnegligible dispersion. In other words, the CEM GC itself is nonuniform with location- and frequency-dependent effective dielectric losses and delays. AIC and BB GCs are also identified by field analysis along *Line G*-AIC and *Line G*-BB, as shown in Fig. 4(b) and (c) respectively. Both GCs are defined by their ground vias, which serve as nonideal electrically short

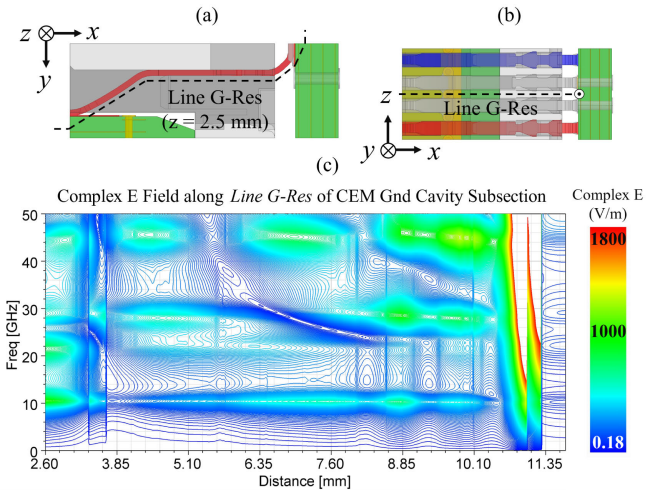

Fig. 5. CEM ground cavity section analysis with *Line G-Res*: (a) side view, (b) front view of the section, and (c) contourplot of complex E-field along *Line G-Res* of the CEM ground cavity section.

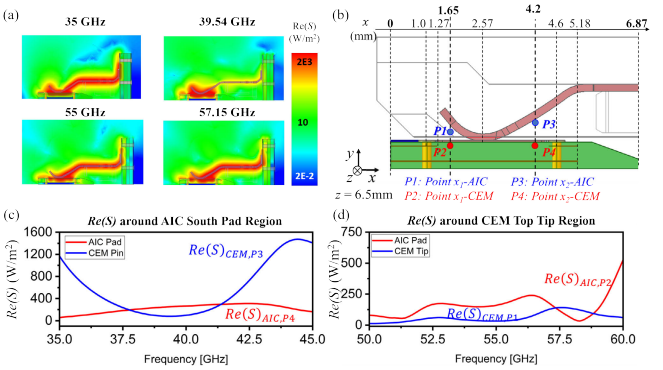

Fig. 6. Analysis of real Poynting vector $Re(S)$ magnitude at Tx1. (a) $Re(S)$ field plots on *Plane* Z-Tx1 at two stub-effect resonances (due to AIC south stub and due to CEM top tip) and the adjacent nonresonant frequencies. (b) Placement of field monitor points on *Plane* Z-Tx1. Rectangular field plots compare $Re(S)$ in AIC and CEM (c) for AIC pad and CEM pin at $x = 4.2$ mm at *Line Tx*-AIC and *Line Tx*-CEM, respectively, and (d) for AIC pad and CEM tip at $x = 1.65$ mm at *Line Tx*-AIC and *Line Tip*, respectively.

boundary conditions. AIC GC has stronger field confinement due to the north and south ground lateral bars. The complete GC structure in the connector is a combination of interconnected and overlapped three GCs (AIC, CEM, and BB GCs) and is named 3GC. The wave resonated at AIC and BB GCs perturbs field performance along the whole 3GC structure, contributing to the shifting and splitting of resonant frequencies. Visualization of the imaginary component of the Poynting vector, Im(S), directly identifies cavities of each resonant frequency by distinguishing resonances from real energy propagation. Thereby, Im(S) offers insights into both intracavity oscillations and extracavity interactions between AIC, CEM, and BB GCs [17], [21]. Fig. 4(d) shows magnitude plots of Im(S) on *Plane Z–G* at major resonant frequencies. The first resonance at 11.73 GHz is contributed by CEM GC. Around 23–25 GHz, the second-order CEM-GC resonance interacts with the first-order AIC-GC resonance. It is worth noting that both AIC GC and BB GC have "degeneracy-like" resonance behaviors seen in Fig. 4(b) and (c) respectively. This phenomenon is detailed in Fig. 4(d). The multiple "first-order" resonances in the AIC and BB GC indicate different effective GC lengths. This can be attributed to the weak confinement of GCs, nonunique GC paths, and couplings to adjacent GCs. The 3GC itself as the largest GC from AIC north via (at $x = 1.0$ mm) to BB outer via (at $y = 0.87$ mm) contributes higher frequency resonances. Consequently, the complete 3GC couples the energy propagating through the aggressor pair to the adjacent victim pair, leading to crosstalk resonances in DDFEXT and DDNEXT, besides the effect in DDIL and DDRL. In other words, at cavity resonance, the ground structure: 1) stores the energy instead of serving as a reference ground and shield and 2) leaks resonant energy due to its nonideal boundary conditions at its ends and along its length.

To further validate the GC mechanism and enable equivalent dPBTL circuit modeling, a CEM GC section is truncated from the full PCIe model. This allows direct excitation and probing of the inputs and outputs of the suspected cavity structure. As shown in Fig. 5(a), the section spans from the AIC/CEM interface ($x = 2.57$ mm) to the CEM/BB interface ($y = 2.47$ mm), analyzing the major CEM GC cavity and avoiding AIC and BB resonances. The front view in Fig. 5(b) includes the adjacent signal pins from Tx1 and Tx2 and the central shared ground pins. Fig. 5(c) shows the contourplot of the complex electric field along *Line G-Res* in the CEM ground section. The first three orders of $\lambda/2$ resonances in the E field are observed along the CEM section. The boundaries of this inner CEM GC at the AIC side are loosely defined by two parts: 1) AIC traces directly terminated with the south ground bar after the AIC/CEM mating interface and 2) indirect couplings to AIC south termination. The CEM GC formation will be verified through equivalent dPBTL circuit modeling in the later section with detailed interpretations.

Apart from GC resonances formed by loaded boards, the connector experiences resonances due to poor signal terminations, known as the signal stub effect. A detailed field analysis is conducted around 39.54 and 57.15 GHz on plane *Plane Z*-Tx1 at $z = 2.5$ mm. At $z = 6.5$ mm, monitor plane *Plane Z*-Tx1 is used to provide field visualization of signal-related resonances of the Tx1 pair in AIC and CEM. Fig. 6 shows the effect of loaded stubs in energy transferring along Tx1. Fig. 6(a) presents the field plots on the magnitude of real Poynting vector *Re(S)* at *Plane Z*-Tx1, comparing fields at different frequencies Around 39.54 GHz, the excited Tx1 pair experiences wide and deep resonance, indicating energy propagation into AIC south stubs rather than transferring to the receiving side, as visualized by comparing field performance at 35 and 39.54 GHz. With the comparison of the *Re(S)* field at 55 and 57.15 GHz, a similar signal-stub loading effect occurs at the CEM region above the AIC/CEM interface, shown as extra energy accumulated around the CEM tip. Quantitative field diagnosis is enabled by monitor points *Point* x_1-AIC and *Point* x_1-CEM at $x_1 = 1.35$ mm near the CEM-tip region, as well as *Point* x_2-AIC and *Point* x_2-CEM at $x_2 = 4.2$ mm around the AIC-south-pad region in *Plane Z*-Tx1, as illustrated in Fig. 6(b). Fig. 6(c) and (d) demonstrates a quantitative correlation between the DDIL dips and the field quantities obtained by field monitor points. At $x_2 = 4.2$ mm, Point

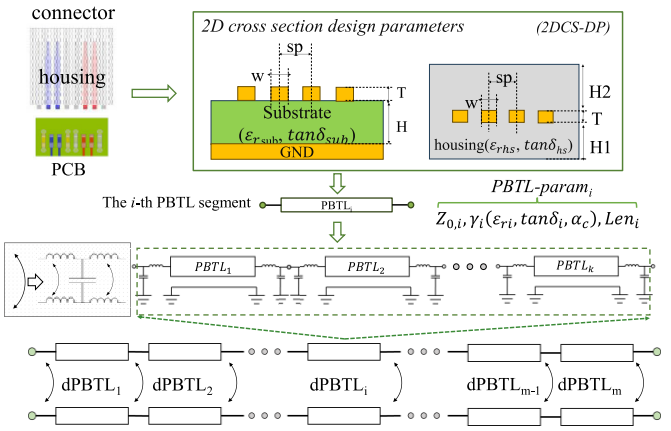

Fig. 7. General dPBTL transformation workflow diagram of 3-D standalone components.

x_2-AIC shows increased *Re(S)*, while Point x_2-CEM shows decreased *Re(S)* around 40 GHz. On the contrary, unterminated CEM tips above $x = 2.57$ mm cause undue energy flow to the CEM tip, resulting in increased *Re(S)* at the *Point* x_1-CEM. Consequently, this leads to reduced *Re(S)* in the Tx1 AIC signal path shown by *Point* x_1-AIC and a small DDIL dip around 57 GHz.

III. Physical-Based Equivalent Circuit Model

To further reduce the complexity of SI diagnosis and facilitate easy assessment, an equivalent dPBTL system for PCIe is established based on automatic 2-D extraction along the DUA. A given connector with nonuniformity and discontinuity can be simplified to a cascade of m-section equivalent transmission lines with sectional approximations [13], [18], [21]. As shown in Fig. 7, a 3-D standalone connector and PCBs, for example, the PCIe CEM connector, BB, and AIC, can be regarded as compositions of 2-D cross section design parameters (2DCS-DPs), which include material properties and dimensions. An ith 3-D section with approximately uniform 2DCS-DPs is transformed into the ith PBTL segment PBTL$_i$. The PBTL parameters (PBTL-param$_i$) of PBTL$_i$ include the effective length len$_i$, the complex propagation constant γ_i, and the characteristic impedance $Z_{0,i}$. The generic analytical form of a dPBTL main-path section (dPBTL$_M$, $1 \le M \le m$, $M \in \mathbb{Z}$) can be expressed in terms of cascaded ABCD matrices of k-segmented lossy PBTLs as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{dPBTL}_M} = \prod_{n=1}^{k} T_{\text{PBTL}_n} \tag{1}$$

where T_{PBTL_n} is the ABCD matrix (or T matrix) for the nth segment PBTL [22], [23]

$$T_{\text{PBTL}_n} = \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix}_{\text{PBTL}_n} \tag{2}$$

$$A_n = \cosh(\gamma_n \text{len}_n) \tag{3}$$

$$B_n = Z_{0,n} \sinh(\gamma_n \text{len}_n) \tag{4}$$

$$C_n = \sinh(\gamma_n \text{len}_n)/Z_{0,n} \tag{5}$$

$$D_n = \cosh(\gamma_n \text{len}_n). \tag{6}$$

Note that, here, T is a simplified notation for the ABCD matrix, not the chain scattering matrix. A complete dPBTL system is then formulated with m sections of a dPBTL subsystem.

Partial internal reflection takes place along dPBTL$_M$, with each partial reflection Γ_i related to the two adjacent PBTL$_i$ and PBTL$_{i+1}$ [22]. Therefore, the dPBTL circuit is able to assist detailed impedance tuning with time-domain reflectometry (TDR) besides the S-parameter performance for frequency-domain diagnosis, including losses and delays. The E-field and H-field disturbances at structural discontinuities can be represented by parasitic capacitive and inductive elements, respectively [21], [24], [25]. Thus, a more realistic ith PBTL cell, PBTL$_i$, can be represented as

$$T_{\text{PBTL}_i} = T_{pc,a} T_{pl,a} T_{\text{PBTL}_i} T_{pl,b} T_{pc,b} \tag{7}$$

where, at the junction nodes a or b, T_{pc} is the T matrix of the parasitic shunt capacitor

$$T_{pc} = \begin{bmatrix} 1 & 0 \\ jC2\pi f & 1 \end{bmatrix} \tag{8}$$

and T_{pl} is the T matrix of the parasitic series inductor

$$T_{pl} = \begin{bmatrix} 1 & jL2\pi f \\ 0 & 1 \end{bmatrix}. \tag{9}$$

Parasitic transitions are only added at major junctions to avoid overparameterization.

A. Extraction of Location-Varying and Frequency-Dependent Equivalent Circuit Parameters With Loading Effect

As shown in Section II, the field in CEM is influenced by the loaded AIC and BB, and vice versa. Such loading effect is reflected in the changes of PBTL-param around the loading regions. Six loading cases (with index as K_k, $k = 1$–6 for later discussion) are discussed for section analysis: (K_1) CEM and AIC loaded together, (K_2) CEM and AIC operate separately (i.e., unloaded), (K_3) AIC without CEM tip above AIC/CEM mating interface (defined for $1.35 \le x < 2.34$ mm in D_2), (K_4) CEM without AIC south signal stub (defined for $2.8 < x \le 4.27$ mm in D_2), (K_5) CEM and BB loading together, and (K_6) CEM and BB operate separately.

For each loading case, the PBTL-param(d, f) has two types of dependencies: 1) location dependence, where d is the position variable at the direction of analysis (e.g., $d = x, y, z$) and 2) frequency dependence, where f is the frequency within the operational range. Python-based automation is developed for 2-D slicing and parameter calculation in Ansys Q3D and 2-D extractor with a step size of 0.2 mm at differential mode [26], [27]. To visualize location dependence, Figs. 8 and 9 show PBTL-param (d,F_B) for $d = x$ (AIC and CEM pairs) and $d = y$ (CEM and BB pairs), respectively, at frequency midpoint $F_B = 32$ GHz for analysis up to 64 GHz. Initial extraction involves differential characteristic impedance Z_{dd}, effective relative real permittivity ε_r (the effective dielectric constant), and the total attenuation constant α [obtained from $Re\ (\gamma)$]. As shown in Fig. 8, loading AIC to CEM alters the PBTL-param of AIC and CEM pairs. The CEM pins and housing above the AIC pads perturb

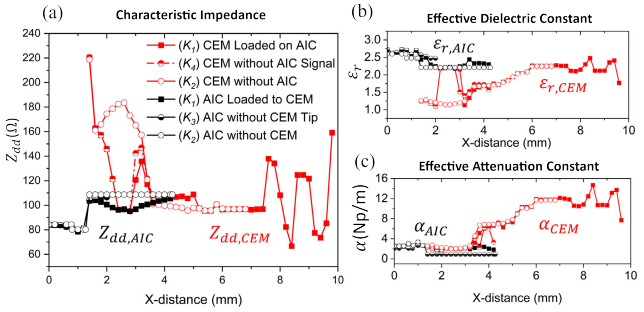

Fig. 8. PBTL parameter 2-D extraction for CEM and AIC differential pairs for (a) $Z_{dd}(x, F_B)$, (b) $\varepsilon_r(x, F_B)$, and (c) total $\alpha(x, F_B)$ at frequency F_B = 32 GHz in labeled loading cases K_k, k = 1 to 4. (b) and (c) share the same legend shown in (a). (b) and (c) share the same legend shown in (a).

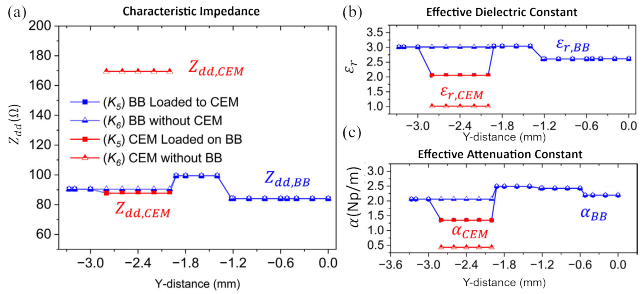

Fig. 9. PBTL parameter 2-D extraction for CEM and BB differential pairs (a) $Z_{dd}(y, F_B)$, (b) $\varepsilon_r(y, F_B)$, and (c) $\alpha(y, F_B)$ in labeled loading cases K_k, k = 5,6. (b) and (c) share the same legend shown in (a).

the field distribution around the AIC/CEM interface from x = 1.35 mm to x = 4.27 mm. Similarly, the AIC conductors (GSSG pins and ground bars) and substrates influence the wave propagation through the CEM structure from x = 0 mm to x = 6.87 mm. The loading effect on sectional impedance continuity, delay, and loss is quantified as the changes in Z_{dd}, ε_r, and total α of AIC and CEM. BB/CEM loading is more straightforward, as shown in Fig. 9. Loading CEM to BB changes $\varepsilon_{r,\mathrm{CEM}}$ from 1 in the air to 2.05 on the board and lowers $Z_{dd,\mathrm{CEM}}$ at the mating region but increases loss due to BB substrate.

The effective dispersion or the frequency dependence of ε_r and $\tan\delta$ is also addressed to accurately characterize the connector's wideband performances. The PBTL-param (D_i, f) averages the PBTL-param (d, f) collected in domain D_i, with frequency, f, from 0.01 to 64 GHz, and presents the overall effective frequency dependence in D_i. Linear approximation is performed on domains annotated in Fig. 2, allowing further implementation into PBTLs. The effective $\varepsilon_r(D_i, f)$ is fit as

$$\varepsilon_r = \varepsilon_{r0} + \varepsilon_r' f \tag{10}$$

where ε_{r0} is the intercepted dc point and ε_r' is the slope along frequency based on the average $\varepsilon_r(d, f)$. Fig. 10(a) shows $\varepsilon_{r,\mathrm{AIC}}(D_i, f)$ and $\varepsilon_{r,\mathrm{CEM}}(D_i, f)$, the effective dielectric constants of AIC and CEM PBTLs, in domain D_i, i = 1, 2, 3. D_4 does not require frequency-domain extraction as the CEM pins are exposed to air. The frequency dependence extracted in D_5 is also negligible as only Megtron6 and vacuum are present around BB, and the quasi-TEM approximation is satisfied with proper BB stack-up design and trace placement [28].

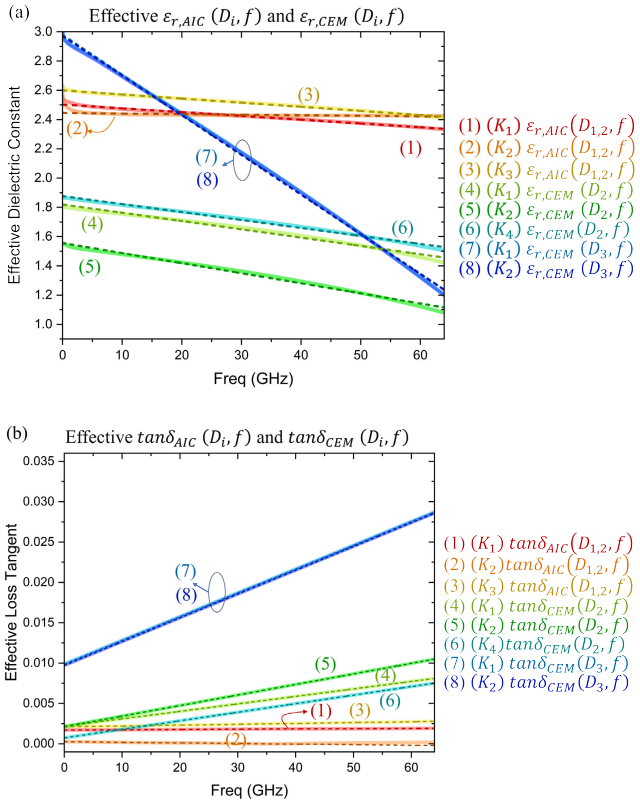

Fig. 10. Extraction and fitting of effective PBTL-param(D_i, f) in AIC and CEM: (a) $\varepsilon_{r,\mathrm{AIC}}(D_i, f)$ and $\varepsilon_{r,\mathrm{CEM}}(D_i, f)(k)$ and (b) $\tan\delta_{\mathrm{AIC}}(D_i, f)(k)$ and $\tan\delta_{\mathrm{CEM}}(D_i, f)(k)$ for domain D_i, i = 1,2,3, and loading case K_k, k = 1–5 shown in the legend. Solid lines are based on average values of PBTL-param over D_i, and dashed lines are calculated from linear fitting.

TABLE II
LINEAR APPROXIMATION OF EFFECTIVE RELATIVE PERMITTIVITY

Domain	dPBTL Path	k	ε_{r0}	$\varepsilon'_r \times 10^3$
1,2	AIC	1	2.50	-2.59
1,2	AIC	2	2.44	-0.38
2#	AIC	3	2.55	-2.59
2	CEM	1	1.82	-5.67
2	CEM	2	1.56	-6.89
2*	CEM	4	1.99	-8.44
3	CEM	1	2.98	-27.21
3	CEM	2	2.97	-27.12

k: subscript index of loading case K_k
2#: from 1.35 to 2.57 mm ; 2*: from 2.57 mm to 4.27 mm

The fitting coefficients ε_{r0} and ε_r' for domains $(i = 1, 2, 3)$ in AIC and CEM at different loading cases are summarized in Table II. The nontrivial frequency dependence in ε_r leads to frequency-dependent velocity and delays in the domains and, consequently, along the whole connector.

The total attenuation $\alpha(D_i, f)$ extracted through 2-D sectional analysis is associated with conductor loss $\alpha_c(D_i, f)$ and dielectric loss $\alpha_d(D_i, f)$ as

$$\alpha = \alpha_c + \alpha_d. \tag{11}$$

The conductor-related attenuation considering skin effect can be written as

$$\alpha_c = \alpha_c(F)\sqrt{f/F_B} \tag{12}$$

TABLE III
LINEAR APPROXIMATION OF EFFECTIVE LOSS TANGENT

Domain	dPBTL Path	k	$tan\delta_0 \times 10^3$	$tan\delta' \times 10^3$
1,2	AIC	1	1.71	0.00
1,2	AIC	2	0.25	0.01
2#	AIC	3	2.10	0.01
2	CEM	1	2.17	0.09
2	CEM	2	2.13	0.13
2*	CEM	4	1.51	0.15
3	CEM	1	9.88	0.29
3	CEM	2	9.72	0.29

k: subscript index of loading case K_k
2#: from 1.35 to 2.57 mm ; 2*: from 2.57 mm to 4.27 mm

where $\alpha_c(F)$ is the conductor-related attenuation calculated at a certain frequency F_B (GHz). The dielectric-related attenuation can be further expressed to relate the effective loss tangent $\tan\delta$, given by

$$\alpha_d = \pi f \tan\delta \sqrt{\varepsilon}_r / c_0 \tag{13}$$

where c_0 is the speed of light in a vacuum and ε_r possesses the frequency dependence in heterogeneous and dispersive media in each domain, i.e., $\varepsilon_r(D_i, f)$, which is linearly fit [29], [30]. Small higher order frequency-dependent loss in 3-D space including radiation loss (which, in general, $\propto f^2$) is not considered in the transmission-line transformation for the sectionally uniform domains but can be added as lossy $R(f)$ and $G(f)$ at sectional interfaces [31]. The PCIe connector uses $n\times$ GSSG configuration in CEM and differential microstrips as feed lines at mated boards. Therefore, the EM wave is relatively confined along the transmission structure. The dominant losses are still the conductor loss ($\propto \sqrt{f}$) and dielectric loss ($\propto f$, when $\varepsilon_r' = 0$ and $\tan\delta' = 0$), [22], [31], [32]. The total 2-D-sectional attenuation α is fit by (12) and (13) to extract the dielectric loss and the corresponding $\tan\delta$. The effective $\tan\delta(D_i, f)$ can be written as

$$\tan\delta = \sqrt{\left(1 + \frac{2\alpha_d^2}{\omega^2 \mu_0 \varepsilon_0 \varepsilon_r}\right)^2 - 1} \tag{14}$$

and also approximated as

$$\tan\delta = \tan\delta_0 + \tan\delta' f \tag{15}$$

in the fitting process, which is further implemented into PBTLs [28], [33]. Fig. 10(b) shows the extracted $\tan\delta$ from α_d for AIC and CEM in domains D_i, $i = 1, 2, 3$, along the x-direction from 0 to 9.62 mm under different loading cases. The fit parameters for $\tan\delta$ in AIC and CEM are summarized in Table III.

The frequency dependencies of the effective dielectric-related delays and losses of AIC and CEM pairs are characterized by corresponding functions of ε_r and $\tan\delta$ defined in equivalent PBTL segments.

B. Circuit Formulation With Loading Resonances

The simple cascading dPBTL framework can accommodate both standalone and loaded connectors without resonant structures, interpreting field distributions varied along interconnected parts. Nevertheless, in the DUA, loading causes resonances, as visualized in Section II. The parallelism of GSSG paths leads to $\lambda/4$ resonance in DDIL when the signal pins or pads are not properly terminated before or after the mating interface. For analytical analysis, a simplified dPBTL diagram is shown in Fig. 11. The signal stub is interpreted as an open-circuited shunt PBTL$_s$, with its ABCD matrix as

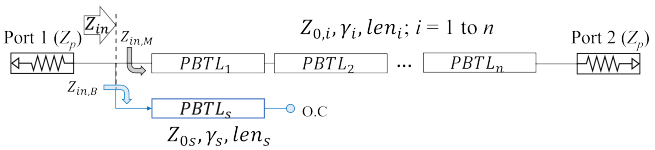

Fig. 11. Simplified dPBTL T-shaped circuit diagram with stub effect in signal transmission due to an open-circuited shunt path.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_s = \begin{bmatrix} 1 & 0 \\ 1/Z_{\text{in,B}} & 1 \end{bmatrix} \tag{16}$$

$$Z_{\text{in},B} = Z_{0s} \coth(\gamma_s \text{len}_s) \tag{17}$$

where $Z_{\text{in},B}$ is the input impedance of the shunt open-circuited PBTL$_s$ with length len$_s$. The total input impedance Z_{in} at Port 1 is the parallel connection of $Z_{\text{in},B}$ and the $Z_{\text{in},M}$ of dPBTL$_M$ with Port 2 impedance Z_p. The overall ABCD matrix of a connector main-path section, dPBTL$_M$, loaded on boards with unterminated stub is written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{total}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_s \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{dPBTL}_M} \tag{18}$$

which can be further transformed into an S-parameter matrix with port impedance Z_p [22], causing DDIL resonance at

$$f_{2n+1,S\text{res}} \approx \frac{(2n+1)c_0}{4\text{len}_s \sqrt{\varepsilon}_{r,s}} \tag{19}$$

where n is an integer from 0 and $f_{S\text{res}}$ is the stub resonant frequency. TDR is transformed from DDRL or directly obtained by sending a step input waveform. Therefore, besides the $\lambda/4$ resonance, the loaded shunt stub also causes changes on the TDR impedance curve even when the connector itself is matched to the designed characteristic impedance. To be more specific, the TDR impedance experiences down-and-up fluctuation. TDR response decreases due to paralleled paths until round trip t_s ($t_s = 0.5/f_{S\text{res}}$) at which $\lambda/4$ transformation is achieved, raising the TDR curve.

In the baseline PCIe 5.0 model, AIC south pads and CEM top pins cause $\lambda/4$ resonances at frequencies below 64 GHz. The AIC stub resonance in DDIL is deep and wide at around 40 GHz, while the CEM stub resonance is nearly negligible (at around 57 GHz). The subtle effect of the BB stub is also modeled in the dPBTL section.

Loading CEM with boards affects not only the main signal transmission but also the ground lines. As the field analysis revealed in Section II, ground lines in the CEM connector form resonant GC when loaded with AIC and BB. Ground cavities also exist in AIC and BB themselves, disturbing the wave oscillated and propagated in CEM ground interconnect through direct mating connections and indirect coupling. Similar to modeling loaded stubs in signal transmission, the CEM ground tip above *X2* is modeled as an open-circuited shunt PBTL$_{G-\text{CEMTip},D2}$, while AIC and BB ground pads

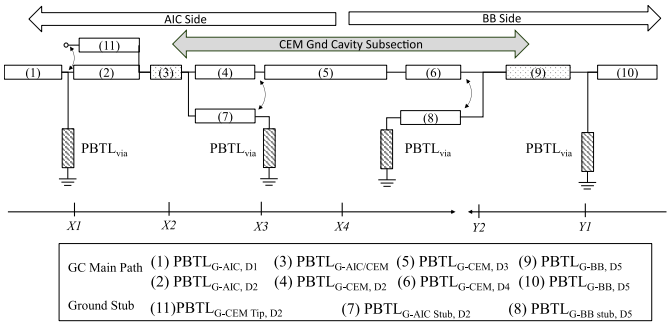

Fig. 12. Simplified π-shaped equivalent dPBTL circuit (dPBTL$_{3GC}$) of 3GC when CEM is loaded on AIC and CEM. The x-direction and y-direction coupling interfaces are labeled in the diagram. The CEM ground subsection is illustrated. The AIC side and the BB side are separated at X4.

below CEM ground pins are regarded as shunt short-circuited PBTLs. The mating interface also serves as a weak boundary for ground resonances in CEM with impedance discontinuity and resultant strong reflection. The resultant 3GC circuit is illustrated in Fig. 12. The equivalent ground paths represented by PBTL$_{G,D_i}$ for AIC, CEM, and BB in the ith domain (D_i) are cascaded along x- and y- directions. In the gigahertz regime, the ground vias are no longer electrically short to be considered as lumped RLGC and, thus, are instead effectively modeled as short-circuited transmission lines for wideband accuracy [34], [35].

The CEM GC per se is modeled as a π-shaped dPBTL equivalent circuit to abstract the EM resonance validated in Fig. 5. The dPBTL$_{G-\mathrm{CEM}}$ (as cascading PBTL$_{G-\mathrm{CEM},Di}$, i = 2,3,4), the equivalent dPBTL of CEM ground interconnect, is mounted on short-circuited dPBTL$_{G-\mathrm{AIC,GB}}$ and dPBTL$_{G-\mathrm{BB,GB}}$, which represent AIC and BB ground pads, respectively. The dPBTL$_{G-\mathrm{AIC,GB}}$ includes AIC pad PBTL$_{G-\mathrm{AICStub},D2}$ and ground via PBTL$_{\mathrm{via}}$ terminated to the south ground lateral bar. Similarly, dPBTL$_{G-\mathrm{BB,GB}}$ includes BB pad PBTL$_{G-\mathrm{BB\ Stub},D4}$, and BB ground via PBTL$_{\mathrm{via}}$ terminated to the BB ground plane. The analytical ABCD matrix of a ground cavity illustrated in Fig. 13 with loaded boards can be generally written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_C = \begin{bmatrix} 1 & 0 \\ 1/Z_{\mathrm{in,GB}} & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_G \times \begin{bmatrix} 1 & 0 \\ 1/Z_{\mathrm{in,GB}} & 1 \end{bmatrix} \tag{20}$$

$$Z_{\mathrm{in,GB}} = Z_{0,gs} \frac{Z_{\mathrm{in},v} + Z_{0,gs} \tanh(\gamma_{gs} \mathrm{len}_{gs})}{Z_{0,gs} + Z_{\mathrm{in},v} \tanh(\gamma_{gs} \mathrm{len}_{gs})} \tag{21}$$

$$Z_{\mathrm{in},v} = Z_{0s} \tanh(\gamma_v \mathrm{len}_v) \tag{22}$$

where ABCD$_G$ is the total ABCD matrix of dPBTL$_G$ with m segmented PBTLs for the ground lines with nonuniformity. The GC loaded with shunt short-circuited segments will also have $\lambda/4$ stub-effect resonance in its IL. Thus, in asymmetrical structures such as CEM GC loaded with shunt dPBTL$_{G-\mathrm{AIC,GB}}$ and dPBTL$_{G-\mathrm{BB,GB}}$, there are two $\lambda/4$ stub-effect resonances. The length of the BB-side shunt stub is small; thus, only the AIC-side short-circuited shunt stub effect will be observed within the analyzed frequency range. In GC without PCB

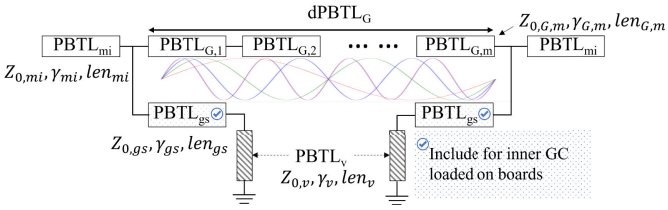

Fig. 13. Generic dPBTL circuit unit for GC formed when interconnect mounted on board with/without stub effect and for board-side GC.

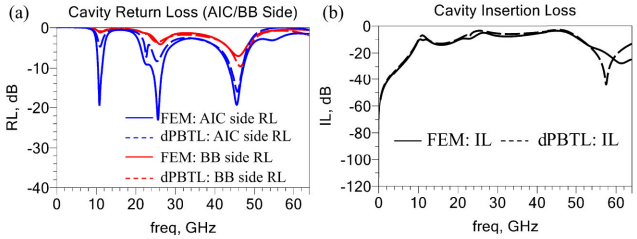

Fig. 14. CEM GC performances of PCIe Gen5 baseline model with the comparison of FEM and dPBTL results regarding (a) RL at AIC and BB side and (b) IL.

stubs, $Z_{\mathrm{in,GB}} = Z_{\mathrm{in},v}$, the $\lambda/4$ resonant frequency due to shunt via (i.e., short-circuited PBTL$_v$) will be beyond 64 GHz given its small len$_v$. The $\lambda/2$ GC resonant frequency $f_{n,Gres}$ of the ground cavity can be approximated as

$$f_{n,Gres} \approx \frac{nc_0}{2\mathrm{len}_G \sqrt{\varepsilon_{r,G}}}. \tag{23}$$

In [18] and [22], the mating interface or feed line of the GC, modeled as equivalent PBTL$_{mi}$, is included for direct verification and further connection to other sections; hence,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{GC}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{mi} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_C \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{mi}. \tag{24}$$

The equivalent dPBTL circuit of the standalone CEM GC is constructed to validate the GC idea. Fig. 14(a) shows RL analyzed at the AIC side and BB side of the CEM GC section by FEM and the equivalent dPBTL circuit. Fig. 14(b) compares the two methods concerning IL of CEM GC. Indirect capacitive couplings are added around *X3* (between the AIC south ground pad and the CEM ground interconnect in D_3) and around *Y2* (between the BB pad-to-via junction and CEM ground interconnect in D_5). The coexistence of direct short-circuited termination and indirect coupling contributes to the degeneracy-like resonances in cavity performance. In addition, the ground shunt stub in the AIC south region (D_2) contributes to a wide dip in IL of CEM GC above 50 GHz. The ground-stub resonant frequency is predicted with a 3-GHz error. The GC resonant frequencies are predicted with an error of 0.17 GHz in RL at two sides and 0.25 GHz in IL. The root mean square errors (RMSEs) of the S-parameters between dPBTL prediction and HFSS reference are used to quantify the overall accuracy. The RMSEs up to 50 GHz for DDRLs at the AIC side and the BB side are 2.9 and 0.6 dB, respectively, while the RMSE of DDIL prediction is 1.4 dB. The higher RMSE on the AIC side can be due to approximating the

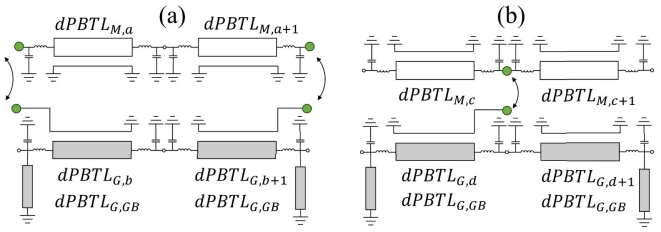

Fig. 15. Coupling between signal main path and GC with junction parasitics. (a) Extracavity coupling. (b) Intracavity coupling.

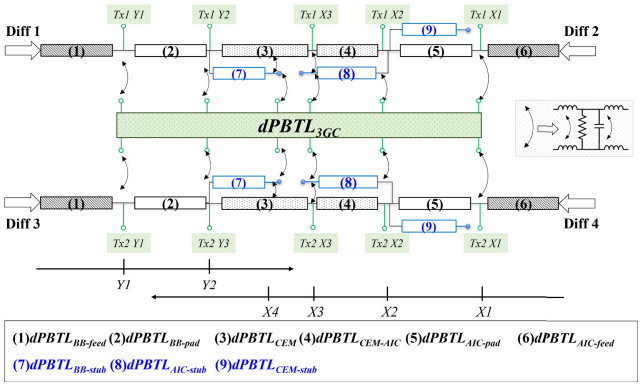

Fig. 16. Full dPBTL equivalent circuit of PCIe 5.0 connector: main-path CEM dPBTL loaded on AIC and BB dPBTLs with stub effects and integrated with ground resonance subcircuit ($dPBTL_{3GC}$) at annotated interfaces.

AIC-side nonuniform ground path with single PBTL per domain for AIC and CEM and underestimating AIC-to-CEM coupling and radiation.

The equivalent circuit modeling helps to explain the GC concept when it operates independently. In the full connector, as demonstrated in Fig. 4, the resonant fields occur along 3GC in AIC, CEM, and BB. Instead of direct excitation for previous investigation of GC mechanism, the GC or 3GC gains and loses energy through couplings with neighboring signal transmission paths, especially at interfaces with discontinuities labeled in Fig. 12 as $X1$ to $X3$ and $Y1$ to $Y2$ [17], [18]. The generic coupling between the signal main path and GC is illustrated in Fig. 15. The neighboring signal conductors serve as the reference in GC. Extracavity couplings happen at the outer boundaries of GC to signal main path, while intracavity coupling happens at the junction with strong discontinuity. The complete equivalent dPBTL circuit for PCIe CEM loaded with AIC and BB is shown in Fig. 16. X1 ($x = 1 \pm 0.2$ mm) is the transition position of microstrip feed lines to $n\times$ GSSG in AIC. *X2* (around $x = 2.57 \pm 0.235$ mm) is the AIC/CEM mating interface. *X3* is the end of the AIC south stub. *X3* is at $x = 4.27$ mm for the AIC signal stub, and *X3* is at $x = 4.6 \pm 0.2386$ mm for the AIC ground stub. *Y2* is at $y = 02.19$ mm after BB/CEM mating. *Y1* is at $y = 0.87 \pm 0.3218$ mm.

AIC- and BB-side subsections are evaluated for the PCIe DUA above and below *X4* ($x = 6.87$ mm). In AIC- and BB-side dPBTL, GC subcircuits are integrated between the signal pairs. Fig. 17(a) shows the DDIL of the AIC- and BB-side subsections modeled by dPBTL equivalent circuits compared to the FEM simulated DDIL. The AIC-to-CEM

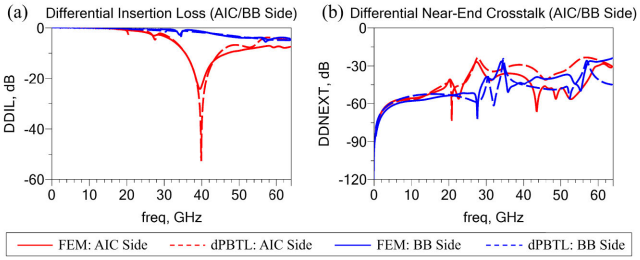

Fig. 17. Comparing results of HFSS FEM and dPBTL equivalent circuits for AIC- and BB-side subsections, regarding their DDIL and DDNEXT at AIC/BB side, respectively. (a) Differential insertion loss (AIC/BB side). (b) Differential near-end crosstalk (AIC/BB side).

loading effect of 3-D signal transmission is precisely transformed into a 1-D circuit by integrating CEM dPBTL with AIC-stub dPBTL. This circuit integration contributes to additional overall losses and moreover causes the 40-GHz resonance in DDIL of both the AIC-side section and full connector. The circuit integration for loading is also applied to the BB side. The DDIL baselines on both sides are accurately predicted by dPBTL, with an RMSE of 0.2 dB below 40 GHz for both sections. The dPBTL method overestimates the AIC-stub resonance depth, increasing the AIC-side RMSE to 1.2 dB up to 64 GHz, while the BB-side RMSE remains below 0.3 dB. Nevertheless, the AIC-stub resonant frequency is well predicted with an error of 0.3 GHz. Fig. 17(b) compares the DDNEXT results for AIC- and BB-side subsections, evaluated by dPBTL models and the 3-D FEM solver. For DDNEXT of both subsections, the dPBTL method predicts baselines with an average RMSE of 5 dB across all frequencies and accurately captures the main resonant frequencies below 40 GHz with an average error of 0.2 GHz.

Dividing the DUA into AIC- and BB-side subsections enables precise diagnosis of each crosstalk resonance with the equivalent dPBTL circuits. The inner CEM GC is disabled due to separation, hence no resonance at around 11 GHz. The AIC GC structure consists of two GCs from $X1$–$X3$: 1) a major GC between the AIC north via at $X1$ and south via at $X3$ and 2) a weaker GC between the north via at *X1* and CEM, coupling down to the AIC south via at $X3$, contributing to resonances between 20 and 30 GHz. The BB GC structure is similar, but with shorter effective lengths, causing resonances between 30 and 40 GHz. These GC resonances are "loaded" to the connector, perceived as spikes in crosstalk and dips in DDIL.

After the section validation and diagnosis, AIC- and BB-side dPBTLs are connected to form the complete PCIe 5.0 equivalent dPBTL circuit. Integration of loading effects with resonances is established with the signal stubs $dPBTL_{AIC\text{-}stub}$, $dPBTL_{CEM\text{-}stub}$, $dPBTL_{BB\text{-}stub}$, and the 3GC $dPBTL_{3GC}$.

C. Results of PCIe 5.0 dPBTL Circuit Model

Fig. 18 compares the performance of PCIe 5.0 analyzed by FEM and by the 1-D equivalent dPBTL circuit. The complete PCIe dPBTL circuit consists of 44 PBTL segments and 20 parasitic blocks. Fig. 18(a) shows Tx1 DDIL and

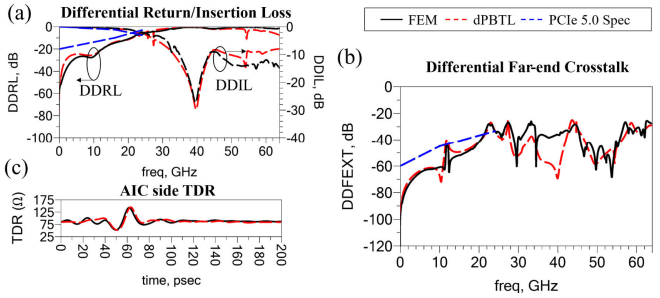

Fig. 18. Differential S-Parameter performances with limit lines defined in PCIe 5.0 CEM specification (spec) [2]. (a) Tx1 DDIL and AIC-side DDRL. (b) DDFEXT (BB-side Tx1 to AIC-side Tx2). (c) Differential AIC-side TDR transformed from AIC-side DDRL.

AIC-side DDRL, with the differential TDR from DDRL plotted in Fig. 18(c). The dPBTL circuit accurately characterizes the Tx1 pair with 0.16-GHz error in error in stub resonance prediction and average RMSE of 0.8 and 3 dB for DDIL and DDRL, respectively. Thus, the circuit model effectively captures impedance discontinuities, frequency-dependent losses, sectional-variant delays, and the effects of the loaded stubs. The AIC-stub loading effect includes DDIL resonance around 40 GHz and TDR impedance variations at 50 ps (drop) and 145 ps (peak). Fig. 18(b) demonstrates that the dPBTL circuit accurately predicts the baseline and major resonance spikes of DDFEXT, with an average RMSE of 6 dB across all frequencies and an average error of 0.042 GHz in major resonant frequencies below 40 GHz, closely aligning with the FEM-generated results. The CEM GC formed between AIC and BB contributes to the resonance at 11.73 GHz. In addition, AIC- and BB-side GC-induced resonances are transferred from the subsections to the full model. Each major resonance is, thus, pinpointed to its corresponding GC, validated by the dPBTL counterpart. Therefore, a PCIe-specific dPBTL circuit system is established with flexible sectional decomposition and localized diagnosis, unveiling and quantifying the narrowband and broadband field features as circuit counterparts within the black box of the network matrix solutions.

Aside from improving the effectiveness of diagnosis through circuits, transforming a 3-D connector to a 1-D dPBTL also enhances time efficiency and reduces data storage during SI diagnosis and subsequent pathfinding processes. Table IV lists the time costs of full-wave and dPBTL simulations, using a 64-core high-performance computer. For full-wave analysis of the reduced double-channel PCIe connector, $T_{FW,I}$, is 14 611 s (4.06 h) with an interpolating frequency sweep from 0.01 to 64 GHz at a 0.01-GHz step size. However, mere matrix results with field solutions only provide a characterization of the DUA in terms of inputs and outputs, in other words, as a black box. In-depth analysis requires a discrete solution with saved fields. The total simulation time of the DUA, $T_{FW,D}$, is 58 464 s (16.24 h). For dPBTL, the circuit simulation time, T_{CS}, is 2.74 s, significantly accelerating simulation by at least 5000×, compared to $T_{FW,I}$.

Moreover, the generation of field plots requires substantial postprocessing time besides $T_{FW,D}$. In contrast, a validated

TABLE IV
TIME COSTS OF FULL-WAVE FEM ANALYSIS AND 1-D DPBTL SIMULATION WITH PREPARATION

$T_{FW,I}$(s)	14611	Full-wave Interpolating without Field Solutions
$T_{FW,D}$(s)	58464	Full-wave Discrete with Saved Field
T_{CS} (s)	2.74	1D dPBTL Circuit Simulation
$T_{2D,bs}$ (s)	8040	Total dPBTL Extraction Time for Baseline

TABLE V
DATA STORAGE OF ANALYSIS APPROACHES

Interpolating without Field Solutions#	225 GB
Discrete with Saved Field#	2.15 TB
dPBTL*	444 KB

#: 3D full-wave FEM
*: 1D circuit

product-specific dPBTL offers sufficient interpretation at its preparation or preprocessing stage, at the time cost of detailed 2-D extraction with $t_{2D} = 2$ min per PBTL-param(d, f) parameter set. For better proof of concept, 67 sets are sampled along the connector with a 0.2-mm-dense step size. The time cost of PBTL preparation can be reduced by coarse sampling in more uniform regions without compromising modeling accuracy. The time-efficient advantage of dPBTL can be further promoted in the later stages of pathfinding and design optimization. Each variation of connectors requires a complete full-wave simulation. After the n iterations, the pathfinding time costs $T_{FW,PF}$ will be $nT_{FW,I}$ for matrix solutions and $nT_{FW,D}$ for thorough SI diagnosis with field solutions. In contrast, the pathfinding time costs $T_{\text{dPBTL},PF}$ after n iterations using the equivalent dPBTL will be $nT_{CS} + T_{2D,bs} + T_{2D,vr}$, where $T_{2D,vr} = \sum_{i=1}^{n} k_i t_{2D}$, with k_i as the number of 2-D extractions for the unique regional variation in the ith pathfinding design. Thus, the whole DUA is extracted only once as the regional variations are considered locally for dPBTL, while the full wave approach requires rerunning full model analysis.

The utilization of the dPBTL model as an intermediate express tool can also significantly reduce data storage requirements. As summarized in Table V, dPBTL schematics with results of the complete PCIe 5.0 connector require only 444 kB of disk space. This demonstrates a reduction in storage occupation by a factor of 5.07×10^5 compared to a full-wave interpolating-sweep simulation project with matrix solutions and by a factor of 4.84×10^6 compared to the full-wave discrete-sweep simulation project with field and matrix solutions.

IV. PCIE PATHFINDING ASSISTED BY EQUIVALENT CIRCUIT

Pathfinding solutions to improve the channel performances can be facilitated by the dPBTL-assisted diagnosis illustrated in Section III. The stub resonance due to the loaded AIC south stub limits the bandwidth of the PCIe channel under the current design. The ground resonances due to the 3GC structure interconnecting between AIC and BB through CEM

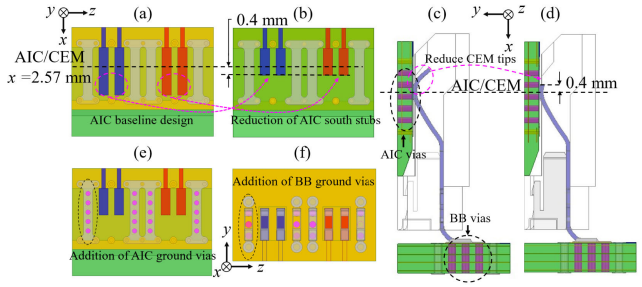

Fig. 19. AIC of PCIe 5.0 baseline model (a), side view of PCIe 5.0 baseline model (c), compared with pathfinding solutions: (b) reduction of AIC south stub, (d) reduction of CEM tips, (e) AIC with blind ground vias, and (f) BB with blind ground vias.

also violate the crosstalk limit lines defined by PCIe 5.0 CEM spec and require improvement. As PCIe marches to higher data rates, the connectors face increased susceptibility to interferences and noises, making these enhancements even more critical to be achieved in early pathfinding.

A. Suppression of Resonances

The root causes of resonances are identified and modeled with their circuit counterparts. This enables more efficient pathfinding solutions, eliminating the need for brute-force parametric sweeping across all design parameters. Initially, two primary aspects are addressed: eliminating stub resonances and suppressing ground resonances. The modifications are illustrated in Fig. 19. The top view of AIC and the side view of the PCIe 5.0 baseline model are shown in Fig. 19(a) and (c) for comparison. In Fig. 19(b), the major PCB stub (i.e., AIC south signal stub) is truncated, leaving a 0.4-mm margin for mechanical mating while preserving ground terminations to the south lateral bar. In Fig. 19(d), the CEM tip stub is fully removed to eliminate any open stub effect in both signal transmission and GC, with a 0.4-mm mating margin as well. The margin may be adjusted during product development to ensure mechanical reliability. To suppress ground resonances, equally spaced blind ground vias are added in the AIC and BB regions, as shown in Fig. 19(e) and (f), respectively. This pathfinding solution is named PF-220. The indices represent the number of steps in each type of modification. For further development, PF-*mnl* indicates m steps in suppressing ground resonances, n steps in eliminating shunt stub effects, and l steps in general broadband improvements.

Field analysis is performed along monitor line *Line G-Res*, *Line G*-AIC, and *Line G*-BB for PCIe PF-220. The contourplots of the E-field complex magnitude are shown in Fig. 20. The improvements in AIC and BB ground terminations effectively eliminate the resonances caused by loaded AIC and BB. Although the CEM GC is still present between the mating interfaces and the nearest ground vias, its field strength is reduced due to the placement of additional vias, which impedes wave transmission into the GC. The reduction of CEM-GC resonances is further demonstrated in the subsection analysis with direct excitation, as seen in Fig. 21. For comparison, in Fig. 5, when the baseline CEM GC is loaded with AIC and BB, fields in AIC and BB ground stubs

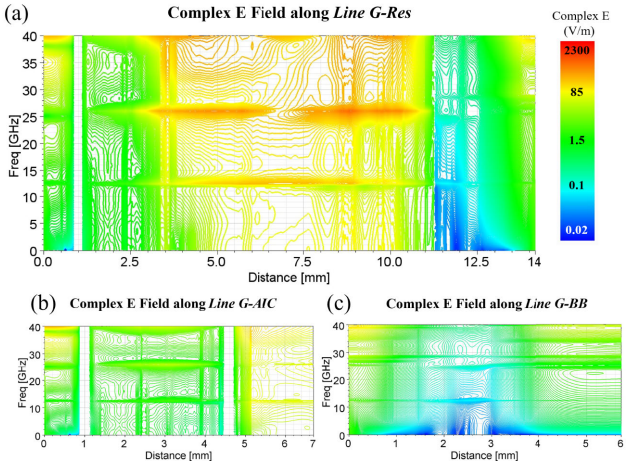

Fig. 20. Contourplots of complex E-field along (a) *Line G-Res*, (b) *Line G*-AIC, and (c) *Line G*-BB in the PCIe pathfinding PF-220 model. (a)–(c) share the same color-key scale.

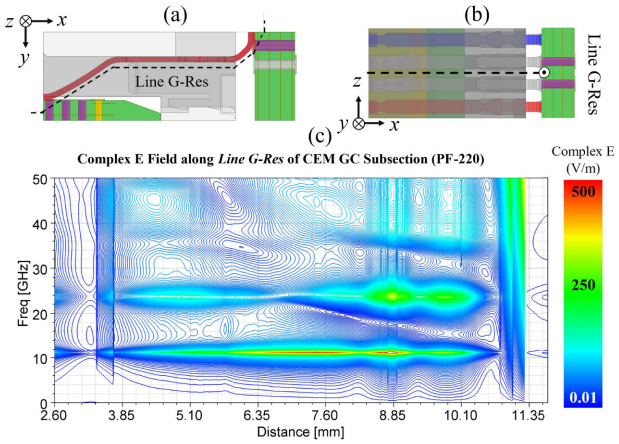

Fig. 21. CEM ground cavity section analysis for the PCIe PF-220: (a) side view, (b) front view of the subsection, and (c) contourplot of complex E field along *Line G-Res* of the CEM ground cavity section.

couple to CEM GC, promoting stronger wave oscillations and allowing energy leakage due to weak confinement.

The equivalent dPBTL circuit of PF-220 CEM GC, $\text{dPBTL}_{\text{CEM-GC}}$, can be quickly modified from Fig. 12 by simply removing the AIC and BB ground-stub dPBTLs and tuning CEM GC PBTL-param$_i$ to remove stub effects, as referred to in PBTL extractions in Section II-A. The S-parameter results of the standalone CEM GC are well predicted by the dPBTL method, as seen in Fig. 22. Without the interactions between AIC and BB, the CEM GC exhibits no degeneracy-like resonance and, moreover, shows a significant reduction in resonances, as well as overall RL and IL. The first-order (i.e., $\lambda/2$) resonance is reduced by 0.83 dB in BB-side RL, 19.35 dB in AIC-side RL, and 16.86 dB in IL. The second-order resonance is reduced by 3.85 dB in BB-side RL, 22.17 dB in AIC-side RL, and 19.95 dB in IL. The third-order resonance is reduced by 6.89 dB in BB-side RL, 18.52 dB in AIC-side RL, and 17.90 dB in IL. The AIC- and BB-side RLs of the CEM GC at 32 GHz are reduced by 1.28 and 2.76 dB, respectively, while the IL at 32 GHz is reduced by 24.31 dB. The suppression of resonance in CEM GC itself is well captured by $\text{dPBTL}_{\text{CEM-GC}}$. The full dPBTL

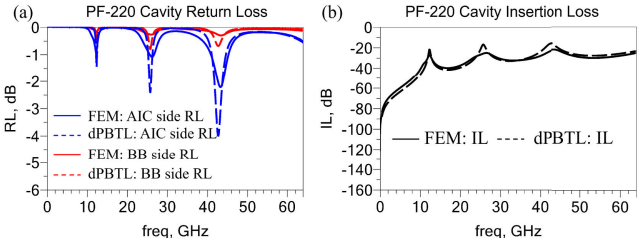

Fig. 22. CEM GC performances of PCIe PF-220 model with the comparison of FEM and dPBTL results regarding (a) RL at AIC and BB side and (b) IL.

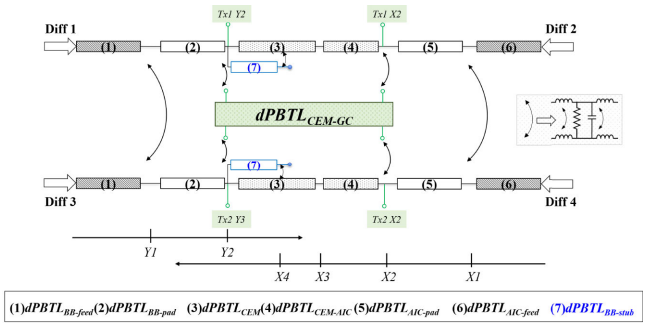

Fig. 23. Full dPBTL equivalent circuit of PCIe pathfinding connector: main-path CEM dPBTL loaded on AIC and BB dPBTLs and integrated with ground resonance subcircuit ($\text{dPBTL}_{\text{CEM-GC}}$) at annotated interfaces.

PCIe PF-220 circuit evolves from Fig. 16 and incorporates the modifications in the signal path and GC. As shown in Fig. 23, the $\text{dPBTL}_{\text{CEM}-GC}$ is integrated into the full circuit at interfaces *Y2* and *X2*.

B. Reduction of Dispersion

The removal of CEM and AIC stubs, AIC and BB GCs, and suppression of CEM-GC resonance aim at reducing undesirable performances at specific frequencies. Pathfinding also needs to stress the importance of broadband improvement. Aside from frequency-dependent loss, dispersion causes degradation of channel performance. The baseline PCIe 5.0 connector exhibits frequency-dependent delay, hence dispersion. In this baseline design, the housing material is the primary contributor to dispersion. Signals transmitted through AIC and CEM above 9.62 mm experience speed increasing with frequency due to effective ε_r decreasing with frequency (i.e., negative ε_r'). The frequency dependence due to the non-homogeneous nature of microstrip lines and coplanar structure in AIC and BB with the field more concentrated in the substrate is subtle compared to the effect of the dispersive housing material. The removal of the AIC south stub in PCIe PF-220 increases the overall frequency dependence due to the reduction of AIC perturbation onto the whole channel. The effective dielectric constant of the full connector, $\varepsilon_{r,T}$, is extracted from the propagation constant γ_T

$$\gamma_T = \tanh^{-a}\left(1/(Z_{d,T}Y_{dd,11})\right)/\text{len}_T \tag{25}$$

where len_T is the effective channel length and the overall differential characteristic impedance $Z_{d,T}$ is $\sqrt{Z_{dd,11}/Y_{dd,11}}$ converted from a differential S-parameter matrix [36]. As shown in Fig. 24, the PCIe 5.0 baseline model has a smaller slope in

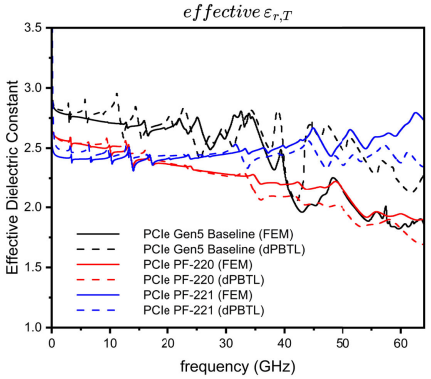

Fig. 24. Effective total $\varepsilon_{r,T}$ extracted from FEM and dPBTL results for PCIe Gen5 baseline design, pathfinding solution PF-220, and PF-221.

$\varepsilon_{r,T}$ up to 40 GHz compared to PF-220 as AIC stub offers an additional path and perturbs the wave transmission.

The next pathfinding involves replacing the original polyamide thermoplastics with a less frequency-dependent housing material. Liquid-crystalline polymer (LCP) is commonly used as housing and packaging material known for its good mechanical properties and excellent heat resistance [37]. Moreover, in [38], the dielectric constant (ε_r) of LCP is determined as 3.16 ± 0.05 up to 104.60 GHz with a loss tangent $\tan\delta$ of 0.004 at 60 GHz and 0.0049 at 97 GHz. In PCIe PF-221, LCP ($\varepsilon_r = 3.16$ and $\tan\delta = 0.004$) is chosen due to negligible frequency dependence and minimal impact on characteristic impedances along the PCIe channel. Compared to the housing materials relying on automatic prediction by the Djordjevic–Sarkar model beyond the available measured frequency in Section II, LCP has verified dielectric properties up to 97 GHz, ensuring more accurate high-frequency simulation results. Without further parameter extraction, the equivalent dPBTL circuit of PF-221 can be approximated by slightly tweaking down $\varepsilon_{r,\text{AIC}}$ and $\varepsilon_{r,\text{CEM}}$ and lowering $\varepsilon'_{r,\text{AIC}}$ and $\varepsilon'_{r,\text{CEM}}$ in corresponding PBTLs in both signal main path and CEM GC to around zero. As shown in Fig. 24, the overall dispersion is largely reduced for PF-221, predicted by the fast-adapted dPBTL and validated through FEM simulation.

The time efficiency of the pathfinding process is greatly improved with the dPBTL approach, as compared in Table VI. The total pathfinding time up to PF-221 for the full-wave approach is 248467 s, due to $4T_{FW,D} + T_{FW,I}$, as all the resonance reduction steps require validation in field analysis. The total pathfinding time cost can be reduced using dPBTL to $5T_{CS} + T_{2D,bs} + T_{2D,vr}$. The variations during PF-220 are extracted in Section III. An additional 16 unique data points are sampled for the structural changes. Thus, the total dPBTL pathfinding time cost is 9973.7 s with $T_{2D,vr} = 16t_{2D}$. The result-generation time is still reduced by 5000× comparing $5T_{CS}$ versus $5T_{FW,I}$, and total pathfinding time cost including validation and analysis is reduced by 25×.

C. Results of Pathfinding Solutions

The effectiveness of pathfinding and the ability of dPBTL models to quickly predict the design modifications are demonstrated by comparing differential S-parameters and differential

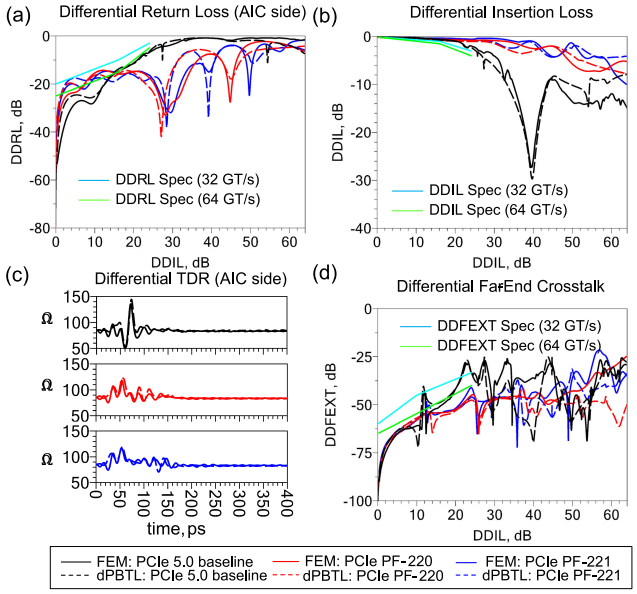

Fig. 25. FEM and equivalent dPBTL circuit results of PCIe pathfinding solutions PF-220 and PF-221 compared with PCIe 5.0 baseline design, with limit lines defined in PCIe 5.0 CEM Spec [2] and in PCIe 6.0 Spec [6], regarding (a) DDRL, (b) DDIL, (c) differential TDR, and (d) DDFEXT.

TABLE VI
TIME COSTS OF FULL-WAVE FEM AND 1-D DPBTL APPROACHES

$T_{FW,PF-221}$(s)	248467	Full-wave Approach up to PF-221
$T_{dPBTL,PF-221}$(s)	9973.7	dPBTL Approach up to PF-221

TABLE VII
AVERAGE RMSE OF DPBTL VERSUS FEM

RMSE (dB)	DDRL	DDIL	DDFEXT
Baseline	3.0	0.80	6.0
PF-220	5.0	0.48	2.9
PF-221	4.3	0.46	3.8

TDR of PCIe PF-220 and PF-221 with the PCIe 5.0 baseline model. The summary of the average RMSE of the differential parameters is shown in Table VII, quantifying the modeling accuracy. For stub-effect reduction, the 40-GHz DDIL resonance is removed through PCIe PF-220, as shown in Fig. 25(b). Reducing the AIC stub in PF-220 significantly decreases the impedance discontinuity around the AIC/CEM interface, lowering the overall DDRL baseline in Fig. 25(a), and reducing the TDR deviation from 85 Ω in Fig. 25(c). DDRL is worse below 15 GHz as the removal of stubs leads to increased $Z_{dd,\mathrm{CEM}}$ and $Z_{dd,\mathrm{AIC}}$, as seen in Fig. 8(a).

PCIe 5.0 baseline connector and its subsequent pathfinding designs all-pass the DDRL requirement for 32 GT/s (i.e., PCIe 5.0). Further efforts will be required to reduce RL below 24 GHz and lower integrated return loss (iRL) of both PF-220 and PF-221 as excursion allowance (iRL ≤ -28 dB). The definition of iRL in dB ($20\log_{10}$) is given as follows:

$$\mathrm{iRL} = \mathrm{dB}\left(\sqrt{\left\{1/N\sum_{i=1}^{N} W(f_i)RL_{\mathrm{avg}}^2(f_i)\right\}}\right) \tag{26}$$

TABLE VIII
IRL (64 GT/s) OF TWO APPROACHES

iRL (dB)	Baseline	PF-220	PF-221
FEM	-34.65	-29.62	-29.18
dPBTL	-31.52	-28.36	-27.35

where N is the number of frequency-based samples. $RL_{\mathrm{avg}}(f_i) = (|\mathrm{DDRL}_{11}(f_i)| + |\mathrm{DDRL}_{22}(f_i)|)/2$, where DDRL_{11} and DDRL_{22} are PCIe DDRLs at the BB and AIC sides. $W(f_i)$ is the weighting function, written as

$$W(f_i) = \mathrm{sinc}^2(f_i/f_b)\frac{1}{1+\left(\frac{f_i}{f_t}\right)^4}\frac{1}{1+\left(\frac{f_i}{f_r}\right)^8} \tag{27}$$

where f_b is the symbol rate for PCIe 6.0 (i.e., 32 GBaud), $f_t = 9.46$ GHz, and $f_r = 24$ GHz at 25-ps rise time. Evaluation of iRL for PCIe 5.0 baseline connector, PF-220, and PF-221 is shown in Table VIII. PF-221 shows the best iRL, improving from -34.65 dB in the baseline connector to -29.18 dB. This trend is also captured by the dPBTL circuit, though underestimated due to coarse PBTL segmentation and limited parasitic elements at segment junctions.

Reduction of reflection around the AIC/CEM mating region and removal of AIC and BB GCs effectively lowers the broadband crosstalk baseline in Fig. 25(d). The GC removal at AIC and BB eliminates AIC-GC and BB-GC resonances and reduces the remaining CEM-GC resonance magnitudes of DDFEXT, as seen in Fig. 25(d). The first two GC resonant frequencies are predicted with an error of 0.2 GHz for PF-220 and 0.35 GHz for PF-221. DDFEXT of PCIe PF-220 and PF-221 not only passes PCIe 5.0 spec but also satisfies PCIe 6.0 spec.

Aside from frequency-based evaluation, eye diagram assessment is also necessitated, offering practical analysis of the digital signal received after transmitting through the connector. Channel simulation with bit-by-bit $2^{13}-1$ pseudorandom binary sequence (PRBS13) at 1 V peak-to-peak is performed for the PCIe 5.0 baseline and pathfinding connectors, with data rate from 16 to 144 Gb/s. No encoder is used for a clear demonstration regarding the effect of pathfinding solutions with increased data rates and different modulations. Thus, the data rate (Gb/s) is the same as the data transfer rate (GT/s) without overhead in this discussion.

NRZ eye diagrams are shown comparing the three designs at 32, 64, and 128 Gb/s, as seen in Fig. 26. Eye closure is experienced by all connectors at 128-Gb/s NRZ. The data-rate-based eye height (EH), eye width (EW), jitter rms, and signal-to-noise ratio (SNR) are summarized in Fig. 27. The improvement of EH and EW, reduction of jitter rms, and enhancement of SNR are achieved by the reduction of resonances and dispersion from 48 to 96 Gb/s. The eye-quality enhancement by PF-221 is more effective in PAM4, which has a higher susceptibility to ISI. PAM4 eye diagrams are visualized in Fig. 28. After the removal of stubs, the dispersion effect throughout PF-220 is worse than the baseline connector; thus, its PAM4 eye-openings are smaller than the baseline

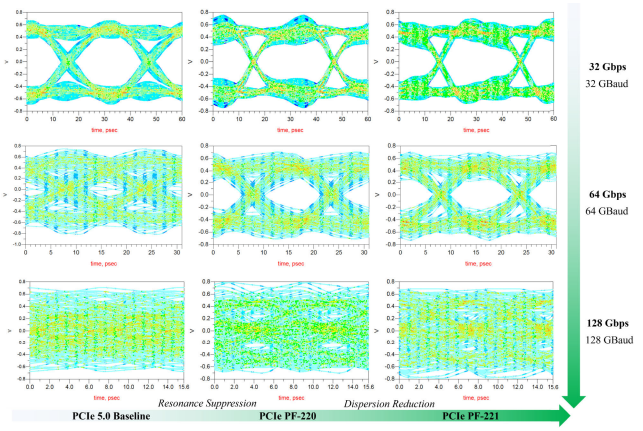

Fig. 26. NRZ eye-diagram demonstration of eye-opening improvement from PCIe 5.0 baseline design, through pathfinding solution PF-220 and PF-221, with PRBS13, from 32 to 128 Gb/s.

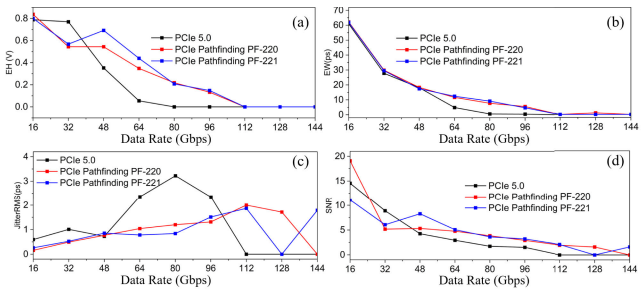

Fig. 27. Eye measurement on NRZ eye diagrams of PCIe 5.0 baseline design, pathfinding solution PF-220, and PF-221, regarding (a) EH, (b) EW, (c) jitter rms, and (d) SNR.

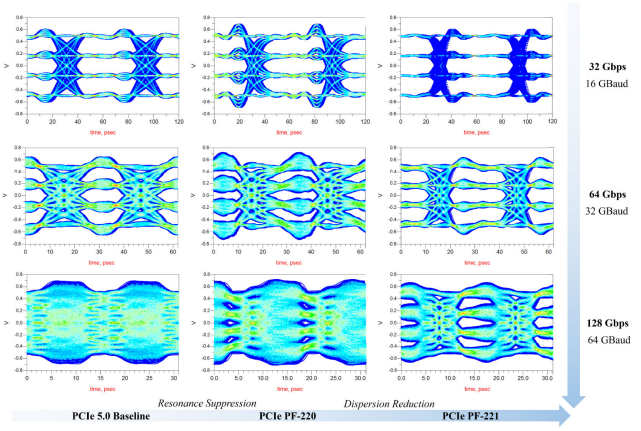

Fig. 28. PAM4 eye-diagram demonstration of eye-opening improvement from PCIe 5.0 baseline design, through pathfinding solution PF-220 and PF-221, with PRBS13, from 32 Gb/s (16 GBaud) to 128 Gb/s (64 GBaud).

before 128 Gb/s. Nevertheless, the stub reduction moves $\lambda/4$ resonance beyond at least $0.75\,f_b = 48$ GHz [39], improving the connector bandwidth and enabling PAM4 eye-opening for PF-220 even at 128 Gb/s (64 GBaud). Furthermore, the utilization of a more frequency-independent housing material in the PCIe PF-221 CEM connector greatly remedies the degradation due to stub removal and even opens the PAM-4 eyes up to 144 Gb/s (72 GBaud). The data-rate-based EH and EW of the upper, middle, and lower eyes of PAM4 eye diagrams in three designs are summarized in Fig. 29.

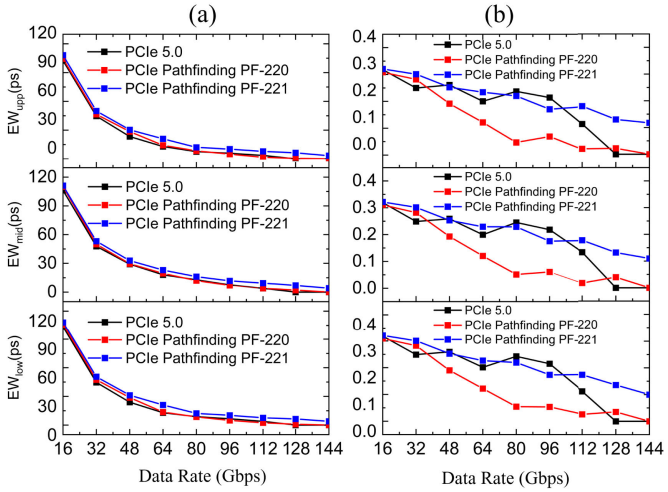

Fig. 29. Eye measurement on PAM4 eye diagrams of PCIe 5.0 baseline design, pathfinding solution PF-220 and PF-221, regarding upper, middle, and lower eye-openings in terms of (a) EH and (b) EW.

The PCIe PF-221 design demonstrates over 150% and around 700% improvement in NRZ EW and EH, respectively, at 64 Gb/s. For PAM4 at 64 Gb/s (32 GBaud), the average enlargement of all three eyes in terms of EW and EH is over 35% and 14% for PF-221 compared to the PCIe 5.0 baseline connector.

V. Conclusion

A PCIe-specific dPBTL model is developed in this work to facilitate fast SI diagnosis and pathfinding solutions for future generations, offering direct and comprehensive insight beyond matrix solutions. A generic dPBTL methodology is proposed for multichannel high-speed connectors with loaded components and resonant structures. Automatic PBTL-parameter extraction is leveraged to achieve fast establishment of the dPBTL circuit model, quantifying the regional-varying, frequency-dependent field features into equivalent circuit parameters. The fast extraction also enables fast model adaptation to interpret connectors under various loading cases and predict design variations. Through EM-based field analyses, the underlying root causes of SI degradation and spec violation in S-parameter performances of the PCIe 5.0 connector are clearly defined and distinguished. Unique frequency-dependent field fingerprints of stub-effect and GC resonances are identified and then concisely transformed into equivalent subcircuits. Specifically, the stub subsections are the shunt open-circuited stubs in AIC, CEM, and BB, leading to $\lambda/4$-resonance in DDIL. The high-Q $\lambda/2$-resonance in all differential S-parameters due to shared GC between aggressor and victim differential pairs is complicated by loading CEM with AIC and BB with shunt short-circuited ground stubs. An equivalent dPBTL circuit models the identified AIC-CEM-BB 3GC structure. The circuit-level interpretation provides insights into the root cause of degeneracy-like resonances due to multiple coexisted GC paths parallel with shunt short-circuited ground stubs. The energy oscillating and accumulating in the GC structure transfers to the losses

and crosstalk along and between the differential signal pairs through field couplings. These field interactions are translated into circuit-level integration between differential-mode dPBTL main paths and the 3GC dPBTL at major interfaces. Separate dPBTL modeling of AIC- and BB-side subsections unveils loading resonances with GC-to-signal interactions.

The integrated dPBTL model of PCIe 5.0 baseline connector is formulated with dPBTL subcircuits assembled at discontinuities and coupling interfaces. The complete circuit model accurately predicts DDRL, DDIL, and DDFEXT up to 64 GHz and differential TDR. By mapping essential field interactions into physical-based circuit models, the dPBTL method offers detailed sectional diagnosis for each SI degradation, pinpointing the root causes of performance issues. Bypassing the complexity of 3-D FEM, the dPBTL approach provides a 5000× acceleration in result generation and a reduction in data storage by a factor of 4.84×10^6.

Guided by the integrated dPBTL modeling of PCIe 5.0 connector, pathfinding solutions on the next-generation connectors efficiently eliminate the stub-effect resonances, suppress the GC resonances, and reduce the dispersion effects. The PCIe-specific dPBTL model effectively predicts differential-mode S-parameter performances of pathfinding modifications up to 64 GHz, reducing the in-depth validation diagnosis time by 25× compared to full-wave simulation. The dPBTL-guided pathfinding connector demonstrates promising improvement for PCIe 6.0 with a 700% EH enlargement, 150% EW improvement at 64-GT/s NRZ, and an average 14% and 35% improvement in EH and EW for three eyes at 64-GT/s (32-GBaud) PAM4. It also shows clear eye-openings at 128- and 144-GT/s PAM4, making it feasible for further DOEs on PCIe 7.0 applications.

The successful application of the integrated dPBTL model in the PCIe connector demonstrates its feasibility for broader use in high-speed multichannel connectors, such as M.2, Octal Small Form-factor Pluggable (OSFP), Quad Small Form-factor Pluggable (QSFP), MicroQuad, High-Speed (MQS) connectors, and emerging 448 G ethernet interfaces. Future work should involve validating FEM simulations with S-parameter and eye-diagram measurements while extending dPBTL capability for precise multiport de-embedding with crosstalk. Automating the dPBTL workflow and integrating ML into the dPBTL-assisted pathfinding process can further enhance design optimization for next-generation high-bandwidth applications.

ACKNOWLEDGMENT

The authors would like to acknowledge the sponsorship of C-NICE on Express Tool for the 5G Link research project by Foxconn Interconnect Technology (FIT), a leading interconnect company led by Sidney Lu UIUC's distinguished alumni. They would like to thank the technical guidance from Jesse Li, Dr. Jason Chou, Dr. Xin Yu, and Dr. Joseph Wang from FIT, for providing valuable suggestions for SI diagnosis.

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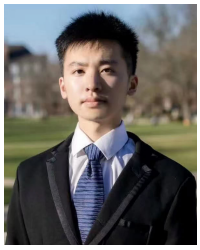

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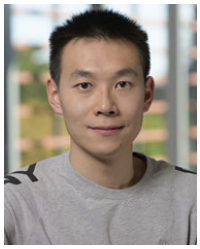

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