Differential Voltage-to-Time Conversion for Digital Readout of Capacitive Sensors

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***Abstract*— This article presents a novel circuit to interface a capacitive sensor directly with a digital processor (DP). The circuit is straightforward, requiring only two resistors, a comparator, and the DP. The method to estimate sensor capacitance, C_x, is also simple and consists of a single sensor charging and discharging process, thus reducing measurement time and power consumption. In the second part of the process, the voltage from each sensor terminal is used to generate a differential input to the comparator. The instant at which there is a change of sign in the differential signal generates the sole time measurement required to estimate C_x. Using a differential signal decreases uncertainty in the C_x estimate by eliminating common-mode noise, which may be important due to the presence of the DP. Under certain considerations, the circuit also eliminates errors due to stray capacitors and, in any case, attenuates them. The circuit can, therefore, estimate C_x values in a wide range with low error. As proof of concept, the circuit has been implemented using a general-purpose board with a field-programmable gate array (FPGA) as the DP. For this circuit and C_x in the range 9.45 pF–95.95 nF, the maximum error is 0.32% with a maximum relative uncertainty of 0.004% if the quantization effects are not considered.**

***Index Terms*— Capacitive sensor, direct interface circuits (DICs), sensor interface electronics, time to digital conversion.**

I. Introduction

CAPACITIVE sensors act as electrical transducers, exhibiting a variety of physical or chemical properties. These sensors can measure pressure [1], [2], strain [3], relative humidity [4], [5], [6], [7], [8], steel surface corrosion [9], [10], and analyze organic substances [11] or monitor microbial growth [12]. The sensor converts the magnitudes of these properties into a capacitance value, C_x, estimated by a designated electronic circuit.

The final measurement from these capacitive sensors' readout circuits increasingly needs to be in digital format, using the minimum possible hardware, time, and energy consumption. Designing circuits that meet all these requirements is challenging, but it enables the integration of capacitive sensors in portable and economical systems suitable for various emerging applications.

Moreover, proposals increasingly incorporate a digital processor (DP), such as a microcontroller, a field-programmable gate array (FPGA), or an ASIC into the sensor readout interface. The DP typically forms part of a higher level system, where the information supplied by the sensor is just one of many inputs received by the system. Therefore, the presence of the DP in the sensor readout circuit does not increase the hardware in the overall system. This is the design principle of the so-called direct interface circuits (DICs). DICs are very simple, using only a few passive components (besides the DP) and, in some cases, a comparator or operational amplifier without analog-to-digital converters.

DICs are used in reading resistive sensors [13], [14], inductive sensors [15], or even sensors that can be modeled using a mixture of components [16]. DICs are also proposed for reading capacitive sensors [17], [18], [19], [20], [21], [22]. The operation of these circuits is based on performing a series of charging and discharging cycles of the capacitor that forms the sensor.

Due to their simplicity, these circuits have several limitations. First, the capacitance ranges they can measure are usually narrow. The range in [17] and [18] is between 10 and 100 pF, spanning just a decade. The same is true for [19], although the circuit can be used for different ranges of values by changing some of the components for each span. The range used in [20] is even narrower, 100–240 pF. Although [21] has a slightly larger range of 4.7–220 nF, only [22] uses a range that exceeds 60 dB, 100 pF–561 nF.

Meanwhile, the estimation errors are typically around 1% for C_x values over 100 pF. Still, they can be significantly larger for lower values, which may be excessive in many applications, where the capacitance range is between 10 and 100 pF.

The proposal in [23] differs by using an RC relaxation oscillator built with three inverters, two resistors, and the DP. The oscillator generates a square signal, whose frequency, measured by the DP, depends on the value of C_x. The range of tested values varies between 1 and 300 pF. Nevertheless, the author only presents results for uncertainty in the estimates, omitting the errors. These errors seem important since the use of up to 19 calibration capacitors is proposed.

One cause of errors in estimating C_x is using time measurements derived from nondifferential voltages. These single-pole voltages are affected by electrical noise introduced in the circuit, primarily due to the clock signal and to switching activity in the DP and propagated through the power lines. It is widely recognized that differential voltage signals offer the benefit of canceling common-mode noise in the circuit [24], [25]. However, as of now, no such signals have been used in the various DICs proposed in the literature.

A second cause of errors in estimating C_x, especially for low values, is stray capacitors that inevitably appear in any

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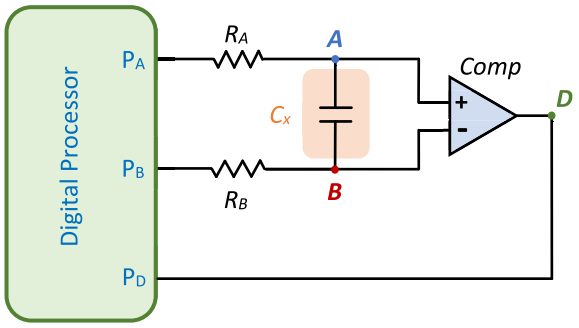

Fig. 1. New DIC to obtain C_x from a differential voltage signal.

circuit. To the best of our knowledge, no DICs address this issue to eliminate or even mitigate their effects.

Finally, except in [22], where just a single sensor charging and discharging process is used to estimate C_x, the other proposals require several such processes, increasing acquisition time, the number of measurements, and power consumption.

This article presents a novel DIC designed to measure a wide span of capacitance values without altering any circuit elements. The hardware is simple and requires a single charging and discharging process to provide the sole time measurement needed to obtain C_x. The estimation is made from a single differential voltage signal, improving the precision and accuracy of these estimates. However, only a single unipolar voltage source is necessary to power the circuit. Furthermore, in common situations, the new method can suppress errors due to stray capacitors in the circuit.

II. New Circuit for Reading Capacitive Sensors

A. Description of the Method and Circuit Analysis

Fig. 1 shows the new circuit proposal to estimate C_x in a capacitive sensor. The circuit consists of the DP, two resistors of known value, R_A and R_B, and a comparator, Comp in Fig. 1. The P_A and P_B pins of the DP should be output pins, while the P_D pin is an input pin.

The relationship between the input and output voltages of the comparator in Fig. 1 is as follows:

$$V_D = \begin{cases} V_{\text{low}}, & \text{if } V_A < V_B \\ V_{\text{high}}, & \text{otherwise} \end{cases} \quad (1)$$

where V_{high} and V_{low} must be compatible with the DP's logical levels. Thus, the DP will consider V_{high} and V_{low} as a "1" and a "0," respectively.

On the other hand, the input voltages of the comparator must be compatible with the "1" and "0" output levels of the DP pins; from now on, we will assume, without loss of generality, that these are V_{DD} (voltage supply) and 0, respectively. Consequently, to simplify the circuit design of Fig. 1 using a single power supply for the DP and comparator, the comparator must allow rail-to-rail inputs. Finally, a large input resistance has also been assumed at the comparator's input terminals, so no current enters them. The reader should consider that some commercial DPs already incorporate a comparator with these characteristics, further reducing the circuit's external components.

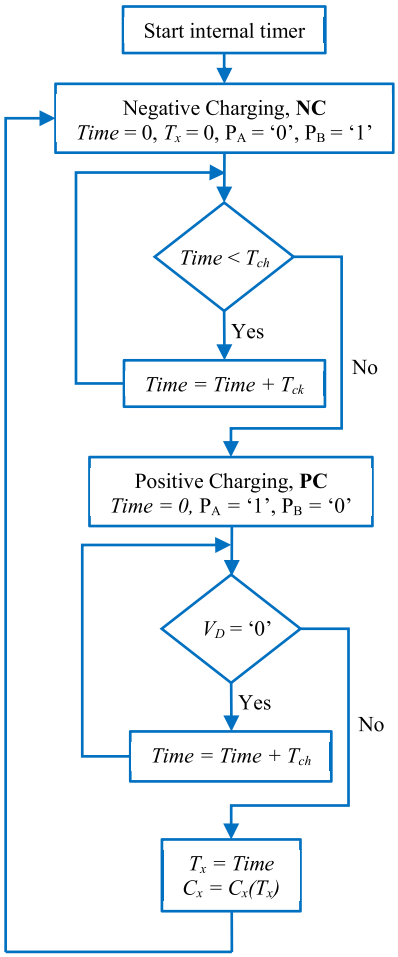

Fig. 2. C_x estimation process.

The C_x estimation process is shown in Fig. 2 and requires only two steps: negative charging (NC) and positive charging (PC). The procedure is controlled by a counter that acts as a timer generating the time variable that stores the information on the time elapsed in each step. Time advances in units of T_{ck}, with T_{ck} being the DP's internal clock signal period.

During NC, P_A = "0" and P_B = "1," such that, after sufficient time, T_{ch}, the voltages at nodes A and B in Fig. 1 are $V_A = 0$ and $V_B = V_{DD}$. Consequently, the voltage difference between these nodes is $V_{AB} = -V_{DD}$. Thus, from a certain instant, the output of the comparator is a "0" input to the DP. Once time T_{ch} has elapsed since the start of NC, the DP changes the states of the output pins to P_A = "1" and P_B = "0," initiating the PC step.

Due to these new values on the DP output pins, V_{AB} increases its value until the instant at which the comparator detects $V_{AB} > 0$. In this situation, the comparator changes the output to "1." This change in V_D will occur with a small delay due to the comparator propagation time, T_p. The duration of the time interval from PC starting until the P_D pin detects a "1" (trigger instant) is the sole time measurement, T_x, needed to estimate C_x. The DP stores the T_x value in the form of a number of cycles of its internal clock. The acquisition process is complete once T_x is obtained, and a new estimation can be started immediately.

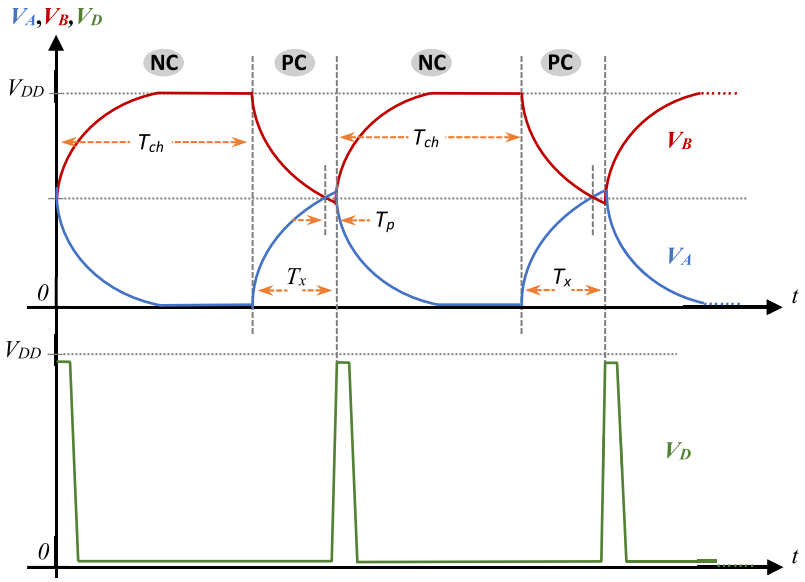

Fig. 3. Expected waveforms for the proposed method in the NC-PC steps shown in Fig. 2. Notice how, at the end of an estimation process (PC step), the next estimation (NC step) can begin.

Fig. 3 shows the time evolution of the voltages V_A, V_B, and V_D during the two steps of several estimation processes (the label of each curve appears on the right side of the figure). The time for which V_D is "1" depends on how fast the DP can detect the "1" in P_D, as well as on the value of T_p and when a new estimation process is started. If the intention is to start a new estimate immediately after obtaining T_x, this time is minimal and can be as small as one cycle of the DP's internal clock.

Fig. 3 also shows that, even if we wish to perform a new estimation process immediately after $V_{AB} > 0$ is reached, the PC duration is extended mainly due to T_p, and V_{AB} continues to increase during this time. Fig. 3 points out this time amplified for the purposes of clarity, although in practice, $T_p \ll T_x$ (there are comparators with T_p values of the order of a few tens of nanoseconds).

The analysis to find the relationship between C_x and T_x is simple but requires some preliminary clarifications. First, pins P_A and P_B have output resistances given by two values, R_p and R_n (usually different), when they provide outputs "1" and "0," respectively. The designer most likely does not know these values. Values R_A and R_B must be selected by the designer to minimize the influence of R_p and R_n on the C_x estimate, verifying

$$R_A + R_B \gg R_p + R_n. \tag{2}$$

This is not a very restrictive condition since high values of R_A and R_B are necessary for good resolution in T_x, especially if C_x is small. Second, $T_p \ll T_x$ will be considered in the following analysis, although this restriction will be removed later.

With the above considerations, the equation that describes the C_x charging process during PC is the well-known equation for a capacitor in an RC circuit

$$\begin{aligned} V_{AB}(t) &= V_f + (V_i - V_f)e^{\frac{-t}{(R_A+R_B+R_p+R_n)\cdot C_x}} \\ &\approx V_f + (V_i - V_f)e^{\frac{-t}{(R_A+R_B)\cdot C_x}} \end{aligned} \tag{3}$$

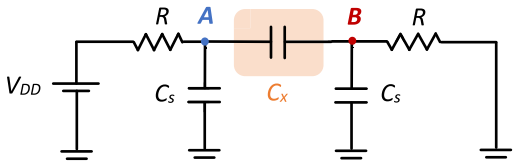

Fig. 4. Circuit to analyze the effect of stray capacitors in the PC step.

where V_f is the value that V_{AB} would reach if the charging process was maintained indefinitely over time, $V_f = V_{DD}$, while V_i is the value of V_{AB} at the beginning of PC, $V_i = V_{AB}(t = 0) = -V_{DD}$. As T_x is obtained practically at the same instant as $V_{AB} = 0$, using (3), we find

$$0 = V_{DD} - 2V_{DD}e^{\frac{-T_x}{(R_A+R_B)\cdot C_x}} \tag{4}$$

and solving for C_x

$$C_x = \frac{T_x}{\ln(2)(R_A + R_B)}. \tag{5}$$

Since all the denominator terms in (5) are known, a constant, a, can be stored in the DP to simplify arithmetic calculations on the processor

$$a = \frac{1}{\ln(2)(R_A + R_B)}. \tag{6}$$

By doing this, the DP estimates C_x using

$$C_x = a \cdot T_x. \tag{7}$$

The steps described in Fig. 2, together with (7), constitute the C_x estimation method. Besides the simplicity of the hardware and the estimation (7), the method uses a single charging and discharging cycle to acquire the sole time measurement required, thus diminishing power consumption and enhancing estimation speed. In addition, time measurements from a differential voltage will yield better estimates than those from circuits using single-pole signals. This is particularly important in DICs since, as mentioned, noises caused by switching in the DP appear on its input and output pins.

B. Effects of Stray Capacitors and Comparator Propagation Time

Together with T_p, the presence of stray capacitors at nodes A and B of the circuit in Fig. 1 delays the trigger instant, increasing the T_x value. These stray capacitors, C_s, become more important as the distance between the DP and the sensor increases and include those at the two comparator inputs, the outputs of the DP, and those arising from the circuit's routing.

However, the errors introduced in T_x by these capacitors can be eliminated under certain conditions. The first condition is that C_s be equal at nodes A and B in Fig. 1. This condition is not overly restrictive, and a well-implemented design can achieve values for the two capacitors at least very close. The second condition requires the designer to choose $R_A = R_B = R$. With these limitations, the new value of T_x is then calculated (which depends on both C_x and C_s).

For this purpose, in the PC step, the circuit of Fig. 1 can be simplified, becoming the circuit in Fig. 4. Observing this circuit, the following equations for nodes A and B can be established:

$$\frac{V_{DD} - V_A}{R} = C_x \frac{d(V_A - V_B)}{dt} + C_s \frac{dV_A}{dt} \tag{8}$$

$$\frac{V_B}{R} = C_x \frac{d(V_A - V_B)}{dt} - C_s \frac{dV_B}{dt}. \tag{9}$$

As the values of V_A and V_B at the beginning of the PC step are $V_A(0) = 0$ and $V_B(0) = V_{DD}$, it is trivial to verify that the solutions of this system of differential equations are as follows:

$$V_A(t) = V_{DD}\left(1 - e^{\frac{-t}{2R\cdot(C_x+C_s/2)}}\right) \tag{10}$$

$$V_B(t) = V_{DD} \cdot e^{\frac{-t}{2R\cdot(C_x+C_s/2)}} \tag{11}$$

and finally

$$V_{AB}(T_x) = V_A(T_x) - V_B(T_x) = V_{DD}\left(1 - 2 \cdot e^{\frac{-T_x}{2R\cdot(C_x+C_s/2)}}\right) = 0. \tag{12}$$

From this result, the value of T_x is

$$T_x = 2\ln(2)R\left(C_x + \frac{C_s}{2}\right). \tag{13}$$

The above expression can easily include the delay due to the comparator's propagation time, T_p

$$T_x = 2\ln(2)R\left(C_x + \frac{C_s}{2}\right) + T_p. \tag{14}$$

The increase in T_x produced by the stray capacitors and the comparator's propagation time can be seen when comparing this result with the value of T_x obtained by solving (5). However, (14) allows a simple calibration method to simultaneously eliminate the effects of C_s and T_p to be designed.

C. Calibration Method

The calibration process consists of estimating a calibration capacitor of known value, C_c. By replacing the sensor with this capacitor in the circuit in Fig. 1 and using the proposed estimation method, a calibration time, T_c, is obtained from (14) replacing C_x with C_c

$$T_c = 2\ln(2)R\left(C_c + \frac{C_s}{2}\right) + T_p \tag{15}$$

and rearranging, we obtain

$$\ln(2)RC_s + T_p = T_c - 2\ln(2)RC_c. \tag{16}$$

Entering this result in (14), we find

$$T_x = 2\ln(2)RC_x + T_c - 2\ln(2)RC_c \tag{17}$$

and finally, the value of C_x

$$C_x = \frac{T_x - T_c}{2\ln(2)R} + C_c. \tag{18}$$

When storing the following constant (known to the designer after calibration) in the DP:

$$b = \frac{T_c}{2\ln(2)R} - C_c \tag{19}$$

the DP provides the estimate of C_x in the form

$$C_x = a \cdot T_x - b. \tag{20}$$

This equation eliminates the effects of C_s and T_p in estimating C_x. However, the limitations under which it has been found must be considered. Thus, the designer must therefore take special care to ensure that the stray capacitors of nodes A and B are as similar as possible. On the other hand, since R_p and R_n are different, the equivalent resistances connected to nodes A and B are slightly different, even if (2) is verified, which will affect the accuracy the system of (8) and (9) can provide.

The asymmetries in the values of the stray capacitors and resistors connected to nodes A and B lead to the appearance of several time constants in the circuit in Fig. 4, meaning errors will appear when estimating C_x using (20). Notwithstanding, if these asymmetries are not very large, (20) will at least partially eliminate the errors introduced by the stray capacitors.

D. Uncertainty

Considering uncertainty as the standard deviation of a series of experimental measurements of a certain magnitude, the uncertainty in the T_x measurement comes from that found when detecting the trigger instant. This uncertainty is caused by the following:

1) uncertainty in detecting the instant of the change of sign of V_{AB}. This uncertainty is due to the comparator;
2) uncertainty caused by the DP when detecting the instant at which V_D becomes "1."

If the comparator changes its output very quickly (as is usually the case), uncertainty in detecting the trigger instant caused by the DP is due solely to the quantization in clock cycles, $u_q(T_x)$. As is well known, this uncertainty is given as a function of the DP clock signal used for T_x quantization [26]

$$u_q(T_x) = \frac{T_{ck}}{\sqrt{12}}. \tag{21}$$

For its part, uncertainty in the comparator detecting the trigger instant, $u_t(T_x)$, is inversely proportional to the slope of $V_{AB}(t)$ when $t = T_x$ [27]

$$u_t(T_x) = \frac{\alpha}{\frac{dV_{AB}}{dt}\Big|_{t=T_x}} \tag{22}$$

where α is a value proportional to the effective value of the noise present in V_{AB}. Considering that V_{AB} is given by (3), with $V_f = V_{DD}$ and $V_i = -V_{DD}$, then

$$u_t(T_x) = \frac{\alpha(R_A + R_B)C_x}{V_{DD}}. \tag{23}$$

The total uncertainty in the measurement of T_x is therefore

$$u(T_x) = \sqrt{u_q^2(T_x) + u_t^2(T_x)} = \sqrt{\frac{T_{ck}^2}{12} + \left(\frac{\alpha(R_A + R_B)C_x}{V_{DD}}\right)^2}. \tag{24}$$

The quantization effects can be neglected if $T_{ck} \ll T_x$ [a condition closely related to $T_{ck} \ll (R_A + R_B) \cdot C_x$], such that $u(T_x) \approx u_t(T_x)$. In this case, the quality in estimating T_x, $u(T_x)/T_x$ can be found straightforwardly using (23) and solving for the value of T_x in (5)

$$\frac{u(T_x)}{T_x} \approx \frac{\alpha(R_A + R_B)C_x}{V_{DD}} \cdot \frac{1}{\ln(2)(R_A + R_B)C_x} = \frac{\alpha}{\ln(2)V_{DD}}. \tag{25}$$

The same result can be found for relative uncertainty in C_x, $u_R(C_x)$, since, using (5) again and the propagation law of uncertainties

$$u_R(C_x) = \frac{u(C_x)}{C_x} = \frac{1}{C_x}\left|\frac{\partial C_x}{\partial T_x}\right| u(T_x) \approx \frac{u(T_x)}{T_x} = \frac{\alpha}{\ln(2)V_{DD}}. \tag{26}$$

Based on this result, the only way to reduce $u_R(C_x)$ after selecting V_{DD} is to meticulously design the circuit to minimize the difference between electrical noise at nodes A and B of the circuit in Fig. 1.

III. Experimental Results and Discussion

As proof of concept, the circuit in Fig. 1 has been implemented using an FPGA as the DP. The FPGA used, Xilinx Artix 7 XC7A35T, is included in a commercial board, namely, the CMOD A7 from Diligent (Pullman, Washington). The internal clock frequency of the FPGA is set to 100 MHz; however, both the rising and falling edges of the clock have been used to detect trigger times, meaning $T_{ck} = 5$ ns. The power supply for the P_A, P_B, and P_D pins is $V_{DD} = 3.3$ V. The values of the output resistors of the P_A and P_B pins are approximately 15 Ω for R_n and 25 Ω for R_p.

The comparator is one of two included in a TLV3202 from Texas Instruments. For this family of comparators, the power range varies between 2.7 and 5.5 V. Thus, the same value of 3.3 V as on the FPGA pins has been used in the design. In this comparator model, the input common-mode range extends 200 mV beyond either rail, while the voltage output swing varies from 175 mV to $V_{DD} - 125$ mV. The input impedances for each terminal are 10^{13} Ω and 2 pF. Thus, the comparator verifies all the requirements established at the beginning of Section II. It should be noted that the value of C_s will always be somewhat greater than the 2 pF of the input capacitance of the comparator pins since the capacitance due to the routing of nodes A and B in Fig. 1 must be added. Finally, propagation time is only $T_p = 40$ ns.

To demonstrate the performance of the new circuit, a very wide range of C_x values, from 9.45 pF to 95.952 nF, was selected by using 26 discrete capacitors. This range includes a wide variety of capacitive sensors, several of which are mentioned in Section I. Both resistors and capacitors were measured using an RS Pro LCR-6300 meter. The basic accuracy of this meter is 0.05% for resistors measured with a dc voltage and the same value for capacitors measured with an ac voltage of 1 KHz. The final value assigned is the average generated by the meter after 16 measurements.

The value of the resistors has been selected according to the range of C_x, such that.

1) For the minimum values of C_x, the quantization errors are small compared to T_x.
2) For the maximum values of C_x, T_x is not excessively large.

Therefore, a nominal value of 200 kΩ has been chosen for R_A and R_B, also ensuring (2) is met. Accurately measuring the resistors has provided the values $R_A = 200.228$ kΩ and $R_B = 200.259$ kΩ. With these values, it has been necessary to implement a 23-bit counter in the FPGA to acquire any time measurement, since it has been experimentally verified that the maximum value of T_x (measured in 5 ns cycles) is $5.3 \cdot 10^6$. In contrast, the minimum value is slightly higher than 500. T_{ch} has been selected to stabilize the charging voltage of C_x sufficiently. This is achieved with $T_{ch} = 5 \cdot (R_A + R_B) \cdot C_{x,max}$, with $C_{x,max}$ being the maximum value of C_x (in our case, 95.952 nF). Thus, $T_{ch} \approx 192$ ms, this time is obtained using an additional 2-bit counter that controls the 23-bit counter. Obviously, in other applications where the range of C_x is different, the values of R_A and R_B will also be different. For example, if the minimum value of C_x was 100 nF, then the values of R_A and R_B could be divided by ten, so that the same minimum count value for T_x would be maintained.

Since the errors introduced by C_s appear in the independent term b of (20), a one-point calibration with C_c could be sufficient to compensate for these errors. However, as mentioned, the compensation is not perfect, and it is preferable to use low C_c values to reduce the larger percentage of errors that will occur for low C_x values. Thus, $C_c = 10.02$ pF has been selected.

A series of 200 estimates have been carried out to find the results presented below for each value of C_x. This provides values for various figures of merit that characterize the errors in estimating C_x. The first figure of merit is the maximum relative error for estimating C_x, $e_R(C_x)$, which is defined as

$$e_R(C_x) = \text{Max}\left(\frac{|C_x(i) - C_{x,a}|}{C_{x,a}}\right) \times 100\% \quad i = \{1, 2, \ldots, 200\} \tag{27}$$

where $C_x(i)$ is each of the estimates of C_x, and $C_{x,a}$ is the actual value of C_x obtained with the RS Pro LCR-6300 meter. $e_R(C_x)$ includes both systematic errors, $e_S(C_x)$, and those due

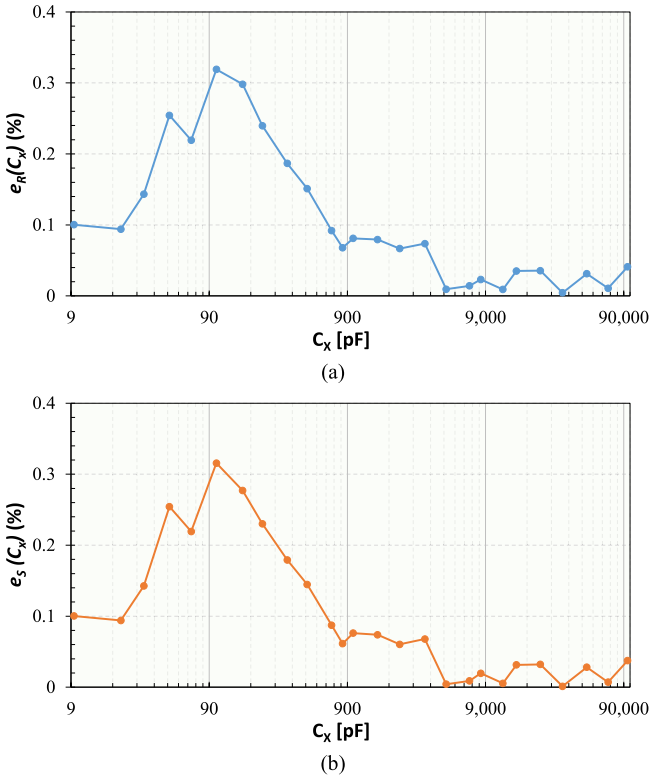

Fig. 5. Relative errors in estimating C_x. (a) $e_R(C_x)$ and (b) $e_S(C_x)$. Note that for $C_x < 90$ pF, e_R and e_S are practically superimposed.

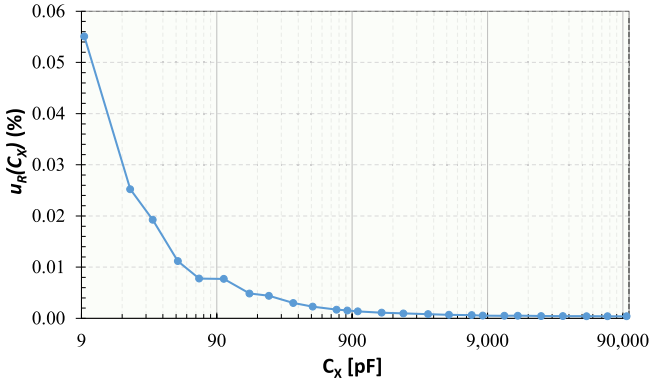

Fig. 6. Relative uncertainty in estimating C_x.

to measurement uncertainty, $u_R(C_x)$. If we define $e_S(C_x)$ as

$$e_S(C_x) = \frac{|\overline{C_x} - C_{x,a}|}{C_{x,a}} \times 100\% \tag{28}$$

where $\overline{C}_x$ is the average of all $C_x(i)$; then, $e_R(C_x)$ can be expressed as

$$e_R(C_x) = \sqrt{e_S^2(C_x) + u_R^2(C_x)}. \tag{29}$$

The value of $e_R(C_x)$ is determined experimentally from (27), and the same occurs with $u_R(C_x)$, which, according to (26), coincides with $u(T_x)/T_x$.

Fig. 5(a) shows the values of $e_R(C_x)$ obtained from (27) (in this figure, and in Figs. 6 and 7, the horizontal axis corresponding to C_x is on a log10 scale for clarity). Fig. 5(a) shows four distinct regions. The region with the smallest values of C_x (up to about 30 pF) has low errors, about 0.1%, and with $e_R(C_x)$ and $e_S(C_x)$ virtually equal. This

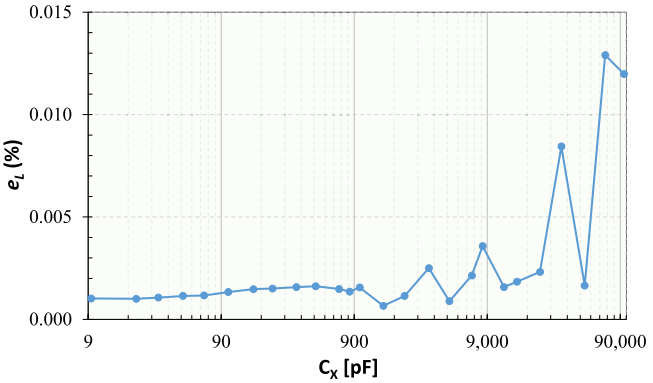

Fig. 7. Linearity errors, e_L, in %.

TABLE I
OTHER INTERESTING PARAMETERS OF THE PROPOSED METHOD

PARAMETER	Value
Number of Estimates/Sample	200
Maximum Repeatability	0.062%
Maximum e_L(%)	0.013%
Minimum Signal-to-Noise Ratio SNR (dB)	102.69
Effective Number of Bits (ENOB)	16.8
Number of Output Bits	23
Resolution	31.2 fF
Normalized Measurement Time	0.677 µs/pF

is because (20) provides a good estimate of C_x, not only eliminating errors due to the stray capacitors but also because the capacitors have values close to the calibration one.

The increase in C_x values is accompanied by greater errors due to the limitations, as discussed, of the calibration method (for example, in our case, R_A and R_B are very similar but not identical, and slight differences may also exist between the values of the stray capacitors at nodes A and B of the implemented circuit).

Although the increase in $e_R(C_x)$ continues up to C_x values around 100 pF, $e_R(C_x)$ is always small, with a maximum of 0.32%. $e_R(C_x)$ begins to decrease after that. This behavior demonstrates that, up to 100 pF, error depends mostly on the independent term b. As (19) indicates, b is small (since T_c and C_c are), and the errors it may cause are therefore also small, although its relative importance increases if small values of C_x are also being estimated. As of 100 pF, the $e_R(C_x)$ decrease is practically monotonic up to 830 pF. From there, the errors are random with a maximum of 0.08%, indicating the good accuracy and precision of parameter a.

Fig. 5(b), which shows the values of $e_S(C_x)$, points out that $e_R(C_x)$ and $e_S(C_x)$ are close throughout the entire range, which, according to (29), is justified by the extremely low values of $u_R(C_x)$.

For $u_R(C_x)$, the results are shown in Fig. 6. First, it should be noted that their values are much lower than those for $e_R(C_x)$

TABLE II
COMPARISON

Work	DC Source	Charging-Discharging Processes	Capacitor Range	Relative Errors	Additional Elements	DP type / Used Pins / DP Requirements	Arithmetic Operations
[18]	5 V	3	149 pF – 206 pF (2.8 dB)	5.61%	2 Resistors + 1 Capacitor	µC / 3 / Timer	1 Division + 2 Subtractions
[19]	5 V	3	100 pF – 1 nF (20 dB)	1.1%	3 Capacitors	µC / 5 / Timer	5 Multiplications + 2 Divisions + 4 Subtractions
[20]	3.3 V	1	100 pF – 240 pF (7.6 dB)	1.3%	3 Resistors	µC / 4 / Timer DAC Voltage comparator Voltage reference source	1 Multiplication + 1 Subtraction
[21]	3.3 V	2	47 nF – 220 nF (13.4 dB)	2%	1 Resistor	µC / 2 / Timer	Square root + 5 Multiplications + 1 Division + 1 Addition
[22]	3.3 V	1	100 pF – 561 nF (75 dB)	1.0%	2 Resistors	FPGA / 3 / Timer	1 Multiplication + 2 Subtractions
This Work	3.3V	1	9.45 pF – 95.952 nF (80.1 dB)	0.32%	2 Resistors + 1 Comparator	FPGA / 3 / Timer	1 Multiplication + 1 Subtraction

(in most cases, more than an order of magnitude lower). Fig. 6 also shows that $u_R(C_x)$ reaches its maximum values for low C_x values (a decreasing function in this region).

The explanation of this behavior is simple since, as shown in (21), the quantization uncertainty is constant. Therefore, as we decrease C_x (the denominator in the calculation of the relative uncertainty), the relative quantization uncertainty increases and because of this $u_R(C_x)$. From 150 pF, $u_R(C_x)$ is practically constant due to the lower relative weight of the quantization uncertainty, as shown by (26).

It is important to remember that relative uncertainty due to quantization will decrease as the R_A and R_B values increase, although this also increases measurement times. However, the experimental results show that $u_R(C_x) \ll e_R(C_x)$ throughout the C_x range, so increasing R_A and R_B does not offer any advantage. It should be noted that the maximum value of $u_R(C_x)$ for $C_x > 150$ pF is 0.004%. This result is only possible due to the differential detection performed by the comparator and has more value, given that the FPGA is part of a commercially available general-purpose board without having a particularly careful design for noise suppression.

Fig. 7 shows the results for the linearity errors expressed in %, $e_L(\%)$. The $e_L(\%)$ values shown in Fig. 7 are small, with a maximum of 0.013%. The fact that the C_x range is so broad (over 80 dB) explains why the $e_L(\%)$ maxima coincide with that of C_x. It should be noted that the apparently large variations of e_L with C_x are solely due to the narrow range (0%–0.015%) of the Y-axis in Fig. 7.

For its part, Fig. 8 shows the relative frequency of estimates for the maximum value of $C_x = 95.952$ nF. As it is the largest capacitance in the range, according to (23), it is also the one that exhibits the greatest uncertainty in measuring times, $u(T_x)$, and, therefore, in estimating capacitances, $u(C_x)$. However, Fig. 8 shows that the difference between the maximum and minimum estimates is only 0.007% of the C_x value. Fig. 8 also shows that, except for the value

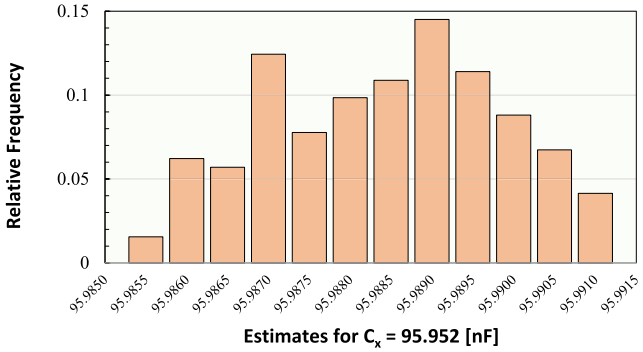

Fig. 8. Relative frequency of estimates for $C_x = 95.952$ nF.

95.9870 nF, the distribution clearly looks like a normal distribution (although slightly skewed to the right).

Table I shows other interesting parameters of the new method, as defined in [28]. In Table I, repeatability is the variation in multiple measurements taken by a circuit on the same C_x and under the same conditions

$$\text{Repeatability} = \frac{\Delta C_x}{C_u - C_l} \times 100\% \tag{30}$$

where ΔC_x is the maximum difference between multiple measurements of C_x. C_u and C_l are the upper limit and lower limit of the measurement range (95.952 nF and 9.45 pF, respectively). For its part, the signal-to-noise ratio (SNR) is defined as

$$\text{SNR} = 10 \log \frac{\sum_i C_x^2(i)}{\sum_i \left(C_x(i) - \overline{C_x}\right)^2}. \tag{31}$$

The table shows how the reduction in uncertainty due to the differential measurement causes high values for SNR and the effective number of bits (ENOBs). The last row in the table includes the normalized measurement time, defined as the quotient between the maximum time necessary to make

an estimate (the sum of the duration of the PC and NC steps) and the maximum value of C_x.

Table II compares the characteristics of the new circuit and other DICs in the literature. The combination of the results of columns two and three of the table shows that the power consumption is similar to the minimum marked by [22], although somewhat higher due to the presence of the comparator. On the contrary, the range of measured values of C_x, the relative errors, and the number of arithmetic operations necessary to obtain an estimate shows a better or equal performance than the best proposal in the literature.

IV. Conclusion

A new circuit has been presented for the digital reading of a capacitive sensor. The circuit is based on the design methodology known as DICs. The circuit, therefore, uses a DP, which controls the sole sensor charging and discharging process required to estimate its capacitance, C_x. Furthermore, the circuit comprises only two resistors and a comparator, while the entire architecture only needs a unipolar power supply. Using a single charging–discharging process reduces both acquisition time and power consumption. The estimation method is based on detecting the passage crossing of 0 of the voltage difference in the two sensor nodes, performing a differential voltage-to-time conversion. The DP is also in charge of obtaining the sole time measurement necessary to estimate C_x.

Employing a differential voltage signal means common-mode noise typically present in DICs (due to the clock signal and switching in the DP) can be reduced, thereby improving uncertainty in the estimations. Moreover, the circuit can, using a calibration capacitor and under certain conditions, eliminate the errors that stray capacitors introduce in estimating C_x. All the above allows a wide range of C_x to be estimated. The circuit has been implemented using an FPGA as the DP, presenting a maximum relative error in estimating C_x of 0.32% for values between 9.45 pF and 95.952 nF, a range of more than 80 dB. Meanwhile, uncertainty in estimating C_x is only 0.004% for $C_x > 150$ pF.

In future work, we will investigate the application of the technique described here to resistive and inductive sensors.

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