An Isolation Amplifier-Based Front-End Circuit for Grounded Capacitive Sensors

Daniel Gelmini, Marcelo A. Haberman, Vittorio Ferrari, *Senior Member, IEEE*, Enrique M. Spinelli, and Ferran Reverter

***Abstract*— A novel front-end circuit for capacitive sensors with one terminal grounded is proposed and evaluated in this article. For the first time, it is suggested to employ an isolation amplifier (IsoAmp) in the front-end circuit of a capacitive sensor. Thanks to this IsoAmp, a floating voltage source is generated that appropriately excites the capacitive sensor. In addition, the concept of active shielding is applied so as to be able to measure remote sensors that are interconnected through a shielded cable. The theoretical, simulation, and experimental results reported herein demonstrate that the sensitivity of the circuit does not depend on the parasitic capacitance of the cable. However, such a parasitic does alter the offset of the input–output (I/O) characteristic mainly due to the nonidealities of the IsoAmp. In terms of linearity, the proposed front-end circuit offers remarkable values, with a maximum nonlinearity error (NLE) of around 0.1% full-scale span (FSS) in the 1–10-pF range and 0.01% FSS in the 10–100-pF range.**

***Index Terms*— Active shielding, capacitive sensor, front-end circuit, grounded capacitive sensor (GCS), sensor interface electronics.**

I. Introduction

THANKS to the proliferation of information and communication technology and the deployment of technologies such as wireless sensor networks and the Internet of Things (IoT), almost everything in the society of the 21st century (such as home appliances, cars, buildings, and cities) is getting smart. However, to become smart, it is essential in the first place to monitor through sensors what occurs in and/or around the smart thing. Different sensing technologies (e.g., resistive, capacitive, and inductive) with different topologies (e.g., single element, differential, and bridge type) are available for monitoring purposes. In comparison with other technologies, capacitive sensors, which are the focus of this article, offer a low-power, low-cost, and robust sensing solution [1], [2].

Manuscript received 27 March 2024; revised 25 April 2024; accepted 3 May 2024. Date of publication 12 June 2024; date of current version 21 June 2024. This work was supported by the Spanish Ministry of Science and Innovation under Project PID2022-139505OB-I00. The Associate Editor coordinating the review process was Dr. Roman Sotner. *(Corresponding author: Ferran Reverter.)*

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Digital Object Identifier 10.1109/TIM.2024.3413177

Capacitive sensors convert information of interest from a given energy domain to the electrical domain by changing its electrical capacitance. These are widely employed to monitor magnitudes from the mechanical domain (such as pressure, acceleration, and displacement), but also from the chemical domain (e.g., humidity) [3]. In a single-element faced-plate topology, the capacitive sensor is formed by two electrodes (or plates) and an intermediate dielectric material. The variables involved in the determination of the capacitance are the distance (d) between electrodes, the overlap area (A) between electrodes, and the electric permittivity (ε) of the dielectric. The electrical capacitance of the sensor changes because the measurand alters d, A, and/or ε, although the effects on d are the most common.

In terms of the potential applied to the electrodes, two subtypes of capacitive sensor can be identified [4]: a) floating capacitive sensors (FCS), in which the two electrodes are not connected by default to any potential and, hence, they are available to the measurement circuit and b) grounded capacitive sensors (GCS), also known as one-terminal capacitive sensors [5], in which one of the two electrodes is always connected to ground. Although FCS is more attractive than GCS in terms of circuit design, the use of GCS is mandatory in some scenarios since the ground connection of one of the sensor electrodes is imposed by the application itself. A typical example is the level measurement of a conductive liquid inside a metallic tank that is grounded for safety reasons [6]. In such a case, an isolated metal rod is one of the sensor electrodes, whereas the other is the grounded shell of the tank. Other examples where GCS is required are the distance/proximity measurement to a grounded metallic object [7] and the linear/angular displacement measurement of a grounded shaft [8].

In terms of localization of the sensor with respect to the measurement circuit, two cases can be distinguished: nonremote and remote sensors. In the former case, the sensor and the circuit are in the same placement, which can be either an electronic board or even an integrated circuit. In the latter case, there is a significant distance (up to several meters) between the sensor and the circuit. Accordingly, it is required an interconnecting cable that has to be shielded to avoid the effects of external interference. In terms of circuit design, nonremote sensors are preferable to remote sensors. However, in some industrial applications, the use of remote sensors is compulsory. This situation occurs when the sensing region offers a harsh environment with extreme operating conditions.

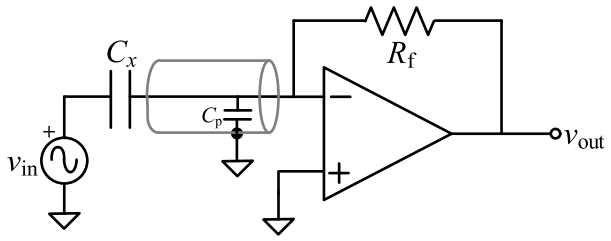

Fig. 1. AC bridge with a current-detection technique applied to the measurement of remote FCS using passive shielding.

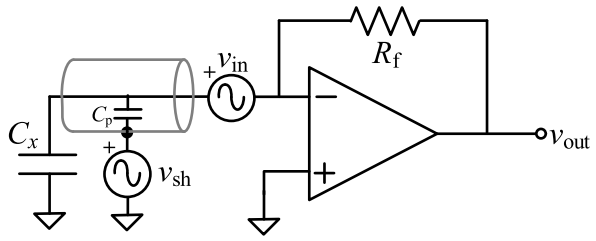

Fig. 2. AC bridge with a current-detection technique applied to the measurement of remote GCS using active shielding.

A typical scenario is when the sensor is located in an environment with very low or very high temperatures (to be precise, below −50 °C and/or above +150 °C) that are not withstood by standard silicon chips required in the readout circuit [9]. Another scenario is when the sensor has to be located in an environment with high radiation levels [10].

For remote FCS, the interconnection to the circuit can be carried out by a cable whose shield is connected to the ground; this is known as passive shielding. In such a case, the parasitic capacitance of the cable (which can be up to three orders of magnitude higher than the sensor capacitance) does not affect the output provided that an ac bridge with a current-detection technique is applied [11], [12]. An example of the implementation of this technique is shown in Fig. 1 using a transimpedance amplifier (TIA) [13], where v_{in} is the sinusoidal input voltage source, C_x is the capacitive sensor, C_p is the parasitic capacitance of the interconnecting cable, and R_f is the feedback resistor of the amplifier. Note that, assuming an ideal operational amplifier (OpAmp), the voltage across C_p is null thanks to the virtual ground and, hence, C_p does not affect the output.

For remote GCS, passive shielding is not recommended since C_p becomes parallel with C_x and can generate a high offset error in the measurement, although it was employed in [7]. To cope with such a limitation, it is advisable to apply the concept of active shielding, where the shield of the interconnecting cable is driven—by a source with a low output impedance—at the same potential as that of the inner conductor of the cable [14]. The circuit in Fig. 1 can be adapted to GCS using the active-shielding technique as represented in Fig. 2 [15], where the voltage (v_{sh}) applied to the shield is ideally equal to v_{in}. Comparing the circuits in Figs. 1 and 2, one realizes that v_{in} and C_x have interchanged their positions. Note that one terminal of v_{in} is grounded and C_x is floating in Fig. 1, whereas v_{in} is floating and C_x is grounded in Fig. 2. The main challenge of the circuit in Fig. 2 is the implementation of the floating voltage source. This was implemented in [15] by a particularly shielded transformer (with 1:1 voltage ratio) so that the voltage applied to the primary side also was in charge of driving the cable shield, whereas the resulting voltage at the secondary side acted as a floating voltage source. The experimental results using such a transformer-based topology were very remarkable, for example, an offset capacitance less than 2 fF and a nonlinearity error (NLE) less than 0.01% full-scale span (FSS) for a 12-m interconnecting cable. However, the circuit in [15] had limitations in terms of volume, cost, and suitability to be integrated into a chip.

In the recent literature, we can find other proposals for the reading of GCS that do not rely on the floating voltage source shown in Fig. 2. For example, a circuit based on a smart driving of the reference node of the OpAmp supply voltage together with active shielding was suggested in [16]. Its experimental results in terms of linearity and offset were comparable to those in [15]. The main limitations of the circuit in [16] are that it requires, on the one hand, a demodulator with a differential input and, on the other hand, good isolation between the reference node of the OpAmp supply voltage and the ground of the circuit. Simpler circuits based on a low-cost microcontroller unit (MCU) for the measurement of GCS have also been recently proposed. In these circuits, the capacitive sensor is usually part of a passive *RC* network and the MCU measures its charging/discharging time [4], [17] or the phase shift affecting a sine wave signal [18]. The output of these circuits was quite sensitive to the parasitic components, thus resulting in an absolute error of 0.8, 1.2, and 0.6 pF in [4], [17], and [18], respectively, when a sensor capacitance of 100 pF was measured. In addition, the previous three MCU-based circuits were not recommended for remote GCS since no specific strategy to compensate the cable effects was applied.

The semiconductor market offers interesting integrated solutions acting as a capacitance-to-digital converter (CDC) for GCS. For example, Analog Devices offers AD7147 (which was employed in [19]) and AD7747. However, most of these commercial CDCs have significant limitations for long interconnecting cables, although the concept of active shielding is applied. For instance, in AD7147, the sensor can be placed only at 10 cm from the CDC. On the other hand, the accuracy of the AD7747 clearly deteriorates when the parasitic capacitance of the interconnecting cable (between CIN and SHLD using the terminology of that chip) becomes higher than 200 pF, which corresponds to around 2 m.

In this article, a novel front-end circuit for remote GCS is suggested and then analyzed theoretically, by simulations, and experimentally. The proposed circuit relies on the configuration shown in Fig. 2, but, unlike [15], the floating voltage source is implemented using an isolation amplifier (IsoAmp) instead of a transformer. Accordingly, the suggested design becomes less expensive, more compact, and more integrable, although it has some technical limitations that are evaluated herein. To the best of the knowledge of the authors, this is the first time that an IsoAmp is proposed to be employed in the

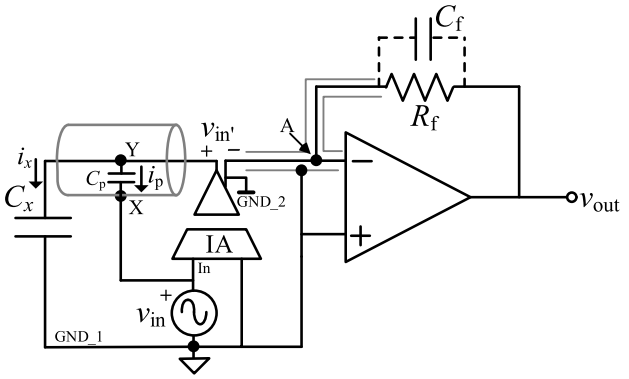

Fig. 3. Proposed IsoAmp-based front-end circuit for the measurement of remote GCS.

front-end circuit of a capacitive sensor. Therefore, the circuit suggested herein can stimulate the design of other new circuits for sensors based on IsoAmps.

This article is organized as follows. The operating principle of the proposed IsoAmp-based circuit is explained in Section II. The simulation results are reported in Section III. The materials and method, and the corresponding experimental results are provided in Sections IV and V, respectively. Finally, the main conclusions are drawn in Section VI.

II. Operating Principle

Using the circuit topology shown in Fig. 2 as a reference, this article proposes the novel front-end circuit represented in Fig. 3 for the measurement of remote GCS. The core of the circuit in Fig. 3 is a floating voltage source implemented by an IsoAmp. The excitation voltage (v_{in}) is applied to the input of the primary side of the IsoAmp and also to the shield of the interconnecting cable, thus resulting in an active shielding. On the other hand, the output of the secondary side of the IsoAmp provides a floating voltage (identified as $v_{in'}$ in Fig. 3) with respect to the reference of the secondary side (identified as GND_2 in Fig. 3). This GND_2 is then connected to the inverting input of the OpAmp that has a voltage equal to zero thanks to the virtual short circuit. The main ground of the circuit is identified in Fig. 3 as GND_1. As the circuits in Figs. 1 and 2 rely on a TIA to convert the sensor current to a voltage, the following analysis corresponding to Fig. 3 is also based on a TIA. However, the idea is also applicable if a charge amplifier is used instead of TIA.

IsoAmps of different technologies (such as magnetic, optic, and capacitive) are available nowadays on the semiconductor market. The operating principle explained here in Section II is valid regardless of the IsoAmp technology selected. However, Sections III–V focus on the use of an IsoAmp with a capacitive technology barrier since this is the alternative that offers the lowest cost and dimensions.

A. Ideal IsoAmp

Let us analyze first the circuit in Fig. 3 considering an ideal IsoAmp. Therefore, since the IsoAmp voltage gain is exactly equal to 1 and there is no phase shift between the input and the output, we have $v_{in} = v_{in'}$. In addition, let us assume the following sinusoidal excitation applied to the input:

$$v_{in}(t) = \sqrt{2}V_{in} \cdot \sin \omega t \tag{1}$$

where V_{in} is the root-mean-square (rms) value of v_{in} and $\omega = 2\pi f$, f being the frequency of the input signal. In such conditions and also considering an ideal OpAmp, the analysis of the circuit in Fig. 3 provides the following expression for the TIA output voltage:

$$v_{out}(t) = \sqrt{2}V_{in}R_f C_x \omega \cdot \cos \omega t. \tag{2}$$

From (2), C_p does not affect the measurement since the same voltage is exactly applied to both its terminals. Furthermore, the output voltage is in quadrature with respect to the input signal. The rms value of this quadrature component is equal to

$$V_{out\_q,i} = V_{in}R_f C_x \omega \tag{3}$$

which increases proportionally to C_x without any offset component.

B. Nonideal IsoAmp

At real conditions, $v_{in'}$ cannot be considered exactly equal to v_{in} due to the dc and ac limitations of the IsoAmp. For a sinusoidal excitation as in (1), the actual output voltage of the IsoAmp can be expressed as

$$v_{in'}(t) = \sqrt{2}V_{in}k \cdot \sin(\omega t + \vartheta) + V_{off} \tag{4}$$

where k is the gain factor (ideally, equal to 1), ϑ is the phase shift (ideally, equal to 0), and V_{off} is the output offset voltage (ideally, equal to 0). Note, in addition, that k and ϑ are expected to be frequency-dependent. Accurate information about k and ϑ is usually not given in the IsoAmp datasheet and, for this reason, these will be specifically determined in Sections III and V.

The analysis of the circuit in Fig. 3 assuming (4) results in the following expression of the TIA output voltage:

$$\begin{aligned} v_{out}(t) = &-\sqrt{2}V_{in}R_f\omega k\left(C_x + C_p\right)\sin\vartheta \cdot \sin\omega t \\ &+\sqrt{2}V_{in}R_f\omega\left[C_x k\cos\vartheta + C_p(k\cos\vartheta - 1)\right]\cdot\cos\omega t. \end{aligned} \tag{5}$$

From (5), the output voltage depends on k, ϑ, and C_p, but it does not on V_{off}. Furthermore, unlike (2), the output voltage has an in-phase and a quadrature component with respect to the input signal. The quadrature component is the signal of interest here since it highly depends on C_x, but slightly on C_p. As explained in more detail in the following sections, this quadrature component will be extracted from v_{out} using a lock-in amplifier (LIA) synchronized at the operating frequency (f) [20].

According to (5), the quadrature component has an rms value that can be expressed as

$$V_{out\_q,r} = V_{in}R_f C_x \omega \underbrace{k\cos\vartheta}_{\substack{\text{Gain}\\ \text{error}}} + \underbrace{V_{in}R_f C_p \omega(k\cos\vartheta - 1)}_{\text{Offset error}}. \tag{6}$$

Comparing (6) with (3), one realizes that the output undergoes a gain error that only depends on k and ϑ, and an offset error that depends on k, ϑ, and C_p. The higher C_p, the higher the offset error. In addition, since both k and $\cos\vartheta$ are expected to be positive but lower than one, the resulting offset error in (6) becomes negative. Such a negative offset can also be deduced from the circuit itself. Note that the voltage at node X is expected to be slightly higher than that at node Y and, hence, the polarity of the current (i_p) through C_p will be the opposite of that (i_x) through C_x.

C. Feedback Impedance

In order to compensate for instability and noise issues found in a basic topology of an OpAmp-based differentiator, a feedback capacitor (C_f) was placed in parallel with R_f [21], as represented in the dashed line in Fig. 3. In such conditions, a pole at $\omega_c = (R_f \cdot C_f)^{-1}$ is introduced in the frequency response, thus limiting the bandwidth of the circuit. Assuming that the frequency of that pole is at least ten times higher than the operating frequency of the circuit, the TIA output voltage is mainly affected in terms of phase. Such effects on the phase generate a quadrature component that is slightly different than that obtained in (6). The rms value of this new quadrature component can be expressed, in an approximate form, as

$$V_{\text{out\_q, r2}} \approx V_{\text{out\_q, r}} + V_{\text{in}} R_f C_p \omega k \sin\vartheta \frac{\frac{\omega}{\omega_c}}{\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2}} \tag{7}$$

where $V_{\text{out\_q,r}}$ is defined by (6). According to (7) and with respect to (6), the presence of C_f introduces an additional offset error that depends on k, ϑ, C_p, and ω/ω_c. Since ϑ is expected to be negative, the resulting $\sin\vartheta$ is also negative, thus generating again a negative offset error.

D. Other Design Considerations

In the circuit shown in Fig. 3, node A is susceptible to interference, either external or internal. For example, the input signal (v_{in}) can capacitively couple to node A, thus generating an (offset) error in the output voltage. For this reason, node A has to be shielded to GND_1, as represented in Fig. 3.

As a consequence of the shielding indicated before, the parasitic capacitance between node A and GND_1 becomes higher. For an ideal OpAmp, this is not a problem thanks to the virtual ground present at node A. However, for a real OpAmp, the voltage at node A is not exactly equal to zero and, hence, such a parasitic capacitance could affect the output voltage. To avoid such effects, it is advisable to select an OpAmp with a high open-loop gain at the operating frequency of the circuit.

Considering that the output voltage of the OpAmp will be connected to an LIA, the dc limitations of the OpAmp (such as the input offset voltage and the input bias current) are not critical here. Note that the mixer of the LIA will move such a dc offset to an ac component with a frequency f, which will be removed by the ensuing low-pass filter (LPF) of the LIA.

III. Simulations

The front-end circuit proposed in Fig. 3 was simulated using the PSpice-for-TI software (Texas Instruments, TI). The selected IsoAmp was the ISO121 (TI), which has a capacitive technology barrier. The TIA was implemented first with an ideal OpAmp and then with a commercial OpAmp. The commercial model was OPA828 (TI), which offers an open-loop gain of 95 dB at the selected operating frequency (i.e., 1 kHz, as discussed in Section III-A). Both IsoAmp and OpAmp were powered at ±6 V. However, the supply voltage of the secondary side of the IsoAmp was independent of that applied to the IsoAmp primary side and the OpAmp. The sinusoidal excitation signal had $V_{\text{in}} = 1$ V, which is a typical excitation amplitude that did not generate overload problems at the input stage of the LIA in the experiments.

As for C_x, two ranges were considered: 1) 1–10-pF range and 2) 10–100-pF range; note that capacitive sensors offering units [22], [23] or tens [24] of picofarads are the most common in the literature. On the other hand, the effects of the interconnecting coaxial cable were simulated by including a capacitor of different values: 0, 100, and 200 pF. These correspond to a cable length of 0, 1, and 2 m, assuming a typical parasitic capacitance of 100 pF/m.

A. Characterization of the IsoAmp

The selected IsoAmp was first simulated alone so as to have more information about the parameters k and ϑ defined in (4). Fig. 4 shows the simulated frequency response of these parameters, with a clear LPF behavior. Note that the higher the frequency, the lower the gain and the higher (in absolute value) the phase shift. Accordingly, for the implementation of the circuit in Fig. 3 using the ISO121, it seems inappropriate to select a high operating frequency since, then, as inferred from (6), both the gain and offset errors would increase significantly. For this reason, it was decided to excite the circuit in Fig. 3 at $f = 1$ kHz, which involves $k = 0.9993$ and $\vartheta = -1.83°$; similar excitation frequencies were employed in [7], [8], [16]. Note, from Fig. 4, that k becomes clearly different than 1 and ϑ different than zero for $f > 1$ kHz. In order to operate at higher frequencies, an IsoAmp with a higher bandwidth should be selected, which will be probably a more expensive chip.

B. 1–10-pF Range

The circuit in Fig. 3 was simulated at $f = 1$ kHz for C_x values in the 1–10-pF range. The TIA was implemented with $R_f = 10$ MΩ and $C_f = 1$ pF. In order to extract the quadrature component from the TIA output voltage, the block diagram shown in Fig. 5 (including a 90° shifter, an ideal mixer, and a second-order LPF with a cutoff frequency of 3 Hz) was employed [20].

The resulting input–output (I/O) characteristic is represented in Fig. 6 for different values of C_p and assuming an ideal OpAmp. According to Fig. 6, the rms value of the quadrature component increases linearly with C_x, as expected. In addition, the presence of C_p introduces a negative offset error but does not affect the slope of the I/O, which agrees with (6) and (7).

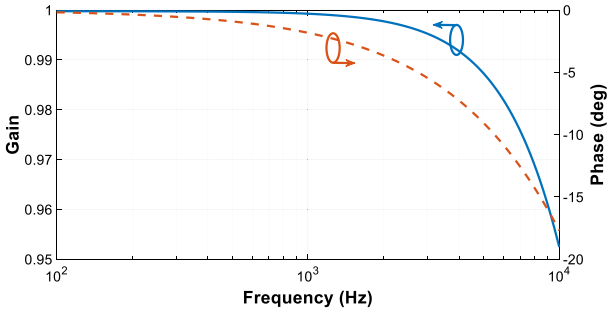

Fig. 4. Simulated frequency response of the gain and phase shift for the commercial IsoAmp under test.

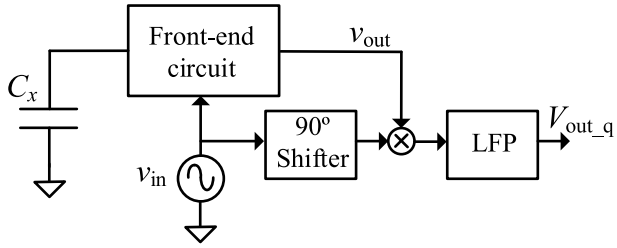

Fig. 5. Block diagram of the circuit simulated to extract the quadrature component (V_{out_q}) of the output signal (v_{out}).

C. 10–100-pF Range

Using the same methodology explained in Section III-B, the circuit in Fig. 3 was simulated in the 10–100-pF range. In this case, the TIA had $R_f = 1$ MΩ and $C_f = 2.2$ pF. In comparison with Section III-B, R_f was selected ten times lower since the applied C_x was ten times higher, and therefore, we could achieve a very similar output voltage range in both scenarios.

Fig. 7 shows the resulting I/O characteristic, again for different values of C_p and assuming an ideal OpAmp. As in Fig. 6, the rms value of the quadrature component in Fig. 7 linearly increases with C_x. The presence of C_p also introduces a negative offset error, but this is much lower than that obtained in Fig. 6. Note, in the zoom provided in Fig. 7, that the difference between the three cases represented is around 1 mV, which is an order of magnitude lower than that obtained in Fig. 6. This is because of the lower value of R_f employed herein and is in agreement with (6) and (7).

D. Discussion

Let us express the rms value of the quadrature component as $V_{out\_q} = m \cdot C_x + b$, where m is the slope and b is the y-intercept. Then, m and b can be calculated from: 1) the ideal model in (3); 2) the actual model in (6); 3) the improved actual model in (7); 4) simulations using an ideal OpAmp (i.e., Figs. 6 and 7); and 5) simulations using a real OpAmp (OPA828), which were conducted but not represented graphically here.

The results for the values of m and b are summarized in Tables I and II for the 1–10-pF and 10–100-pF ranges, respectively. The following conclusions can be drawn from these tables.

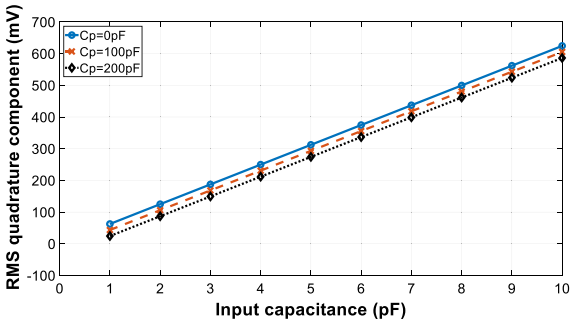

Fig. 6. Simulated I/O characteristic of the circuit shown in Fig. 3 in the 1–10-pF range for different values of C_p and assuming an ideal OpAmp.

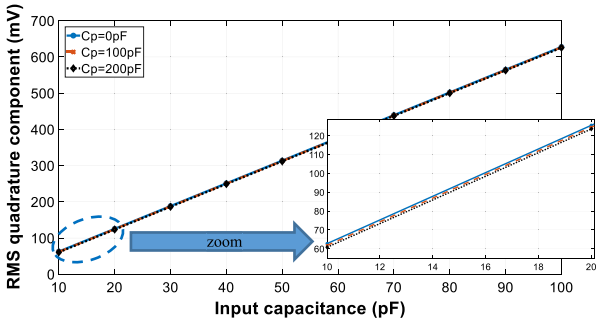

Fig. 7. Simulated I/O characteristic of the circuit shown in Fig. 3 in the 10–100-pF range for different values of C_p and assuming an ideal OpAmp.

1) The model in (3) does not predict any offset error (i.e., $b = 0$).
2) The model in (6) provides a lower value of m with respect to (3) and offers a (negative) b value that depends on C_p.
3) The model in (7) provides a more negative value of b with respect to (6); such effects are higher in the 1–10-pF range (Table I) since the resulting ω_c is lower in that range, and hence, the second offset contribution inferred from (7) becomes higher.
4) The simulation results using the ideal OpAmp are very similar to those obtained from (7).
5) The simulation results using the real OpAmp are almost identical to those obtained with the ideal OpAmp. Accordingly, we can conclude that the commercial OpAmp was well selected for the application of interest.

From Table I, $\Delta C_p = 100$ pF generates $|\Delta b| \approx 19$ mV that corresponds, assuming 62.44 mV/pF, to 0.30 pF. On the other hand, from Table II, $\Delta C_p = 100$ pF causes $|\Delta b| \approx 1$ mV that corresponds, considering 6.276 mV/pF, to 0.16 pF. Consequently, the active shielding suggested in Fig. 3 does not completely eliminate the effects of C_p, but it appears as a residual offset grounded capacitance with an attenuation factor of 333 (= 100/0.30) and 625 (= 100/0.16) in the 1–10- and 10–100-pF ranges, respectively.

IV. Materials and Method

A prototype of the circuit in Fig. 3 was designed in a printed circuit board (PCB) using off-the-shelf components. These components, which are the same or very similar to

TABLE I
THEORETICAL AND SIMULATION RESULTS IN THE 1–10-pF RANGE, FOR DIFFERENT VALUES OF THE CABLE PARASITIC CAPACITANCE

C_p (pF)	Eq. (3)		Eq. (6) [a]		Eq. (7) [a]		Sim. Ideal OpAmp		Sim. Real OpAmp	
	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)
0	62.83	0	62.75	0	62.75	0	62.43	$-6\cdot10^{-5}$	62.44	-0.001
100	62.83	0	62.75	-7.84	62.75	-20.39	62.43	-19.04	62.44	-19.05
200	62.83	0	62.75	-15.67	62.75	-40.78	62.43	-38.07	62.45	-38.10

[a] Calculated using the values of k and ϑ obtained from simulations (Fig. 4).

TABLE II
THEORETICAL AND SIMULATION RESULTS IN THE 10–100-pF RANGE, FOR DIFFERENT VALUES OF THE CABLE PARASITIC CAPACITANCE

C_p (pF)	Eq. (3)		Eq. (6) [a]		Eq. (7) [a]		Sim. Ideal OpAmp		Sim. Real OpAmp	
	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)
0	6.283	0	6.275	0	6.275	0	6.276	$7\cdot10^{-6}$	6.276	-0.001
100	6.283	0	6.275	-0.784	6.275	-1.060	6.276	-0.976	6.276	-0.972
200	6.283	0	6.275	-1.567	6.275	-2.120	6.276	-1.951	6.277	-1.959

[a] Calculated using the values of k and ϑ obtained from simulations (Fig. 4).

TABLE III
COMPONENTS EMPLOYED TO BUILD THE CIRCUIT SHOWN IN FIG. 3

Component	Model or value
IsoAmp	ISO122 (TI) [a]
OpAmp	OPA828 (TI)
R_f	10 MΩ [b] / 1 MΩ [c]
C_f	1 pF [b] / 2.2 pF [c]
v_{in}	f = 1 kHz, V_{in} = 1 V

[a] Note that this IsoAmp is not exactly the same model simulated in Section III, although it is from the same family. In the experiments, ISO122 was selected since it is five times cheaper, but it was not simulated because its PSpice model was not available.
[b] For the 1-10 pF range.
[c] For the 10-100 pF range.

those employed before in the simulations, are summarized in Table III. The capacitive sensor (C_x) was emulated by NP0 ceramic capacitors in two different ranges: 1–10 and 10–100 pF. As for the interconnecting coaxial cable, this was emulated by capacitors of different values: 0, 100, and 200 pF. The main difference with respect to the circuit simulated in Section III is that a first-order LPF (with a cutoff frequency of 50 kHz) was placed at the output of the TIA. Thanks to this LPF, the noise level at the output was decreased before the LIA measurement, thus avoiding a potential overload of the input range when the signal amplitude was close to the limit.

Fig. 8 shows a picture of the measurement setup employed to test the front-end circuit. The OpAmp and the IsoAmp primary side were supplied at ±6 V by means of a bench-top dc power supply (Keithley 2231A–30–3). The IsoAmp secondary side was also supplied at ±6 V but through batteries (Yuasa NP2.8-6S) so as to ensure appropriate isolation between the two grounds (i.e., GND_1 and GND_2 in Fig. 3) of the circuit. A bench-top LIA (Stanford Research Systems SR860) was employed to: 1) provide the excitation signal of 1 kHz to the circuit and 2) extract the quadrature component of the output signal. The lock-in reference source of the LIA was set as internal so that the previous 1-kHz signal was also the synchronization signal for the demodulation. In order to have a stable and reliable measurement, the LIA was set with a time constant of 10 s in the 1–10-pF range and 1 s in the 10–100-pF range. Although it is not present in Fig. 8, the PCB and the batteries were placed inside a metallic box during the measurements so as to avoid any potential effects of external interference. This box was connected to GND_1 that, in turn, was at the Earth's potential. For the initial testing of the circuit, a four-channel digital oscilloscope (Keysight DSOX1204A) was employed to monitor the waveform of the voltage at the main nodes.

The NLE of the experimental I/O characteristic was evaluated as follows. First, the actual value of the input capacitance was measured by an impedance analyzer (Keysight E4990A) at 1 kHz, whereas the rms value of the quadrature component of the output voltage was measured using the LIA. Afterward, a straight line was fit to the experimental data by applying the least-squares method. The difference between the actual output and the output calculated using the previous straight line was then expressed as a percentage of the FSS.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. Characterization of the IsoAmp

The first experiment carried out was the characterization of the IsoAmp alone. The gain and phase shift of the IsoAmp were evaluated in the frequency range between 100 Hz and 10 kHz using the bench-top LIA. This provided the input

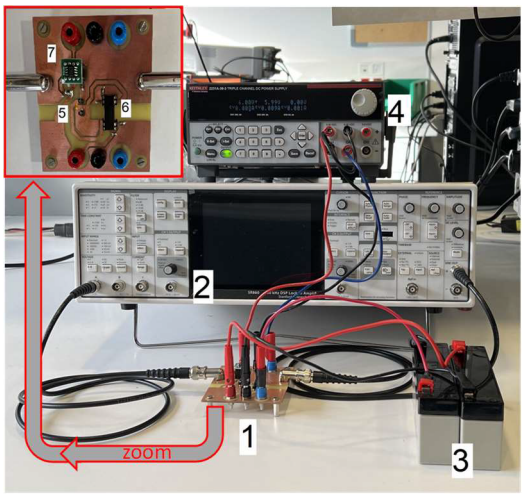

Fig. 8. Picture of the experimental setup. (1) PCB with the front-end circuit. (2) LIA for the generation of the input signal and the reading of the output signal. (3) Batteries to supply the IsoAmp secondary side. (4) Bench-top power supply for both IsoAmp primary side and OpAmp. (5) Placement of C_x on the PCB. (6) IsoAmp on the PCB. (7) OpAmp on the PCB.

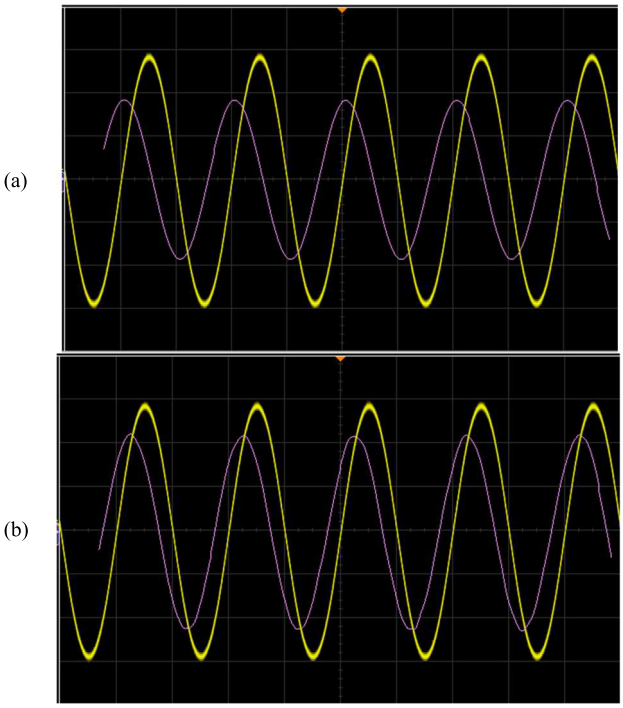

Fig. 9. Snapshots showing the waveform of the input (channel 1 in yellow) and output (channel 2 in purple) voltages of the prototype for (a) $C_x = 10$ pF and $C_p = 0$ pF, and (b) $C_x = 10$ pF and $C_p = 200$ pF. The vertical scale of both channels is 500 mV/div, whereas the horizontal scale is 500 μs/div. The bandwidth of channel 2 was digitally limited to 5 kHz to better observe the signal at the main frequency component.

signal to the IsoAmp primary side and also measured the amplitude and phase of the IsoAmp secondary side using the input signal as a lock-in reference.

The experimental frequency response showed again an LPF behavior, similar to that represented in Fig. 4. At the selected operating frequency (i.e., 1 kHz), the resulting values were $k = 0.9984$ and $\vartheta = -2.01°$. In comparison with the simulation results in Fig. 4 ($k = 0.9993$ and $\vartheta = -1.83°$), the experimental values at 1 kHz were slightly more different than the

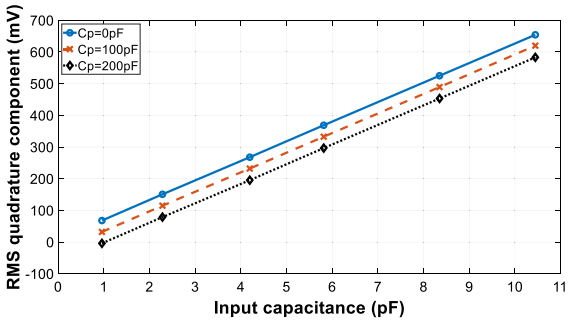

Fig. 10. Experimental I/O characteristic of the circuit shown in Fig. 3 in the 1–10-pF range for different values of C_p.

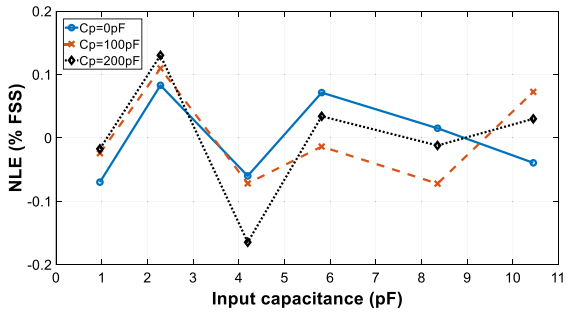

Fig. 11. Experimental NLE of the circuit in Fig. 3 in the 1–10-pF range.

ideal ones (i.e., $k = 1$ and $\vartheta = 0°$). Therefore, the experimental output is expected to suffer from higher offset and gain errors. At higher frequencies (e.g., 10 kHz), the experimental gain was less frequency-dependent, but the experimental phase shift was more frequency-dependent.

B. Experimental Waveforms

After evaluating the frequency response of the IsoAmp, the experimental waveforms at the main nodes of the circuit in Fig. 3 were acquired to validate its correct operating principle. As an example, for $C_x = 10$ pF, Fig. 9(a) and (b) shows the waveforms captured of v_{in} and v_{out} for $C_p = 0$ pF and $C_p = 200$ pF, respectively. In Fig. 9(a), the output voltage is almost in quadrature with respect to the input signal. This is because the in-phase component of the output has a very low amplitude when $C_p = 0$ pF, as inferred from (5). However, in Fig. 9(b), the output has a higher amplitude and is not in quadrature with respect to the input. This is due to the stronger contribution of the in-phase component when C_p has a high value, as predicted before by (5).

C. 1–10-pF Range

Fig. 10 shows the experimental I/O characteristic in the 1–10-pF range using the components indicated in Table III, for different values of C_p. The experimental rms value of the quadrature component in Fig. 10 proportionally increases with C_x, as in the simulation results represented before in Fig. 6. Furthermore, the presence of C_p introduces a negative offset, but it does not affect the slope in Fig. 10, which is similar to what occurs in Fig. 6.

For a better quantitative comparison between theoretical and experimental results, Table IV shows the values of m and b that result from: 1) the model in (7) assuming the experimental

TABLE IV
THEORETICAL AND EXPERIMENTAL RESULTS IN THE 1–10-pF RANGE

C_p (pF)	Eq. (7) [a]		Experimental	
	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)
0	62.69	0	61.80	8.94
100	62.69	-27.62	61.93	-27.44
200	62.69	-55.25	61.87	-63.42

[a] Calculated using the values of k and ϑ obtained from the experimental test of the IsoAmp.

TABLE V
THEORETICAL AND EXPERIMENTAL RESULTS IN THE 10–100-pF RANGE

C_p (pF)	Eq. (7) [a]		Experimental	
	m (mV/pF)	b (mV)	m (mV/pF)	b (mV)
0	6.269	0	6.279	1.204
100	6.269	-1.686	6.279	-0.823
200	6.269	-3.374	6.278	-2.785

[a] Calculated using the values of k and ϑ obtained from the experimental test of the IsoAmp.

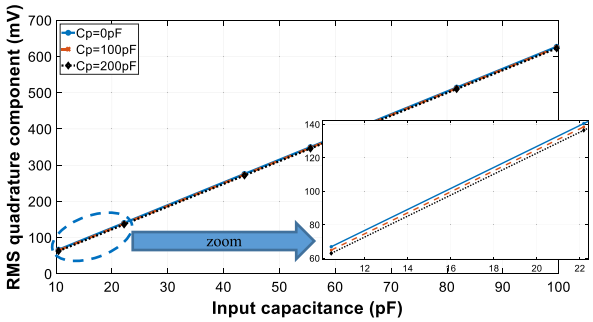

Fig. 12. Experimental I/O characteristic of the circuit shown in Fig. 3 in the 10–100-pF range for different values of C_p.

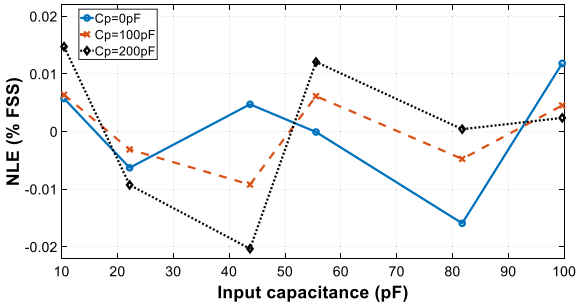

Fig. 13. Experimental NLE of the circuit in Fig. 3 in the 10–100-pF range.

values of k and ϑ and 2) the fitting of a straight line to the experimental data in Fig. 10. According to Table IV, the experimental value of m is around 1% lower than the theoretical one, which can be due to the tolerance of R_f. On the other hand, the experimental value of b for C_p = 0 pF is 8.94 mV instead of 0 mV, which can be attributable to a parasitic grounded capacitance of the PCB; this can be computed by dividing b by m, thus resulting in 0.14 pF. In addition, for ΔC_p = 100 pF, the experimental $|\Delta b|$ is around 36 mV, which is quite similar to the value predicted by (7) (i.e., $|\Delta b| \approx$ 27–28 mV). Such an experimental $|\Delta b|$ corresponds to 0.58 pF, thus resulting in an attenuation factor of 172 (= 100/0.58). This factor is lower than that obtained in the simulations in part because the actual values of k and ϑ are not as ideal as those found in the simulations.

The experimental NLE, resulting from the application of the methodology explained in Section IV, is represented in Fig. 11 for different values of C_p. The maximum NLE (in absolute value) is 0.08, 0.11, and 0.16% FSS for C_p of 0, 100, and 200 pF, respectively.

D. 10–100-pF Range

The methodology explained before in Section V-C was equally applied in the 10–100-pF range, thus resulting in the I/O characteristic shown in Fig. 12, the values of m and b summarized in Table V, and the NLE shown in Fig. 13.

The experimental I/O in Fig. 12 is almost identical to the simulated one represented in Fig. 7. According to the zoom provided in the same Fig. 12, the presence of C_p introduces a negative offset error, but this is much lower than that obtained in Fig. 10.

The theoretical and experimental values of m and b reported in Table V are in remarkable agreement. On the one hand, the experimental value of m is around 0.2% higher than the theoretical one. On the other hand, for C_p = 0 pF, b becomes equal to 1.204 mV instead of 0 mV, which again can be ascribed to a PCB parasitic grounded capacitance ($\approx$ 0.19 pF). Furthermore, ΔC_p = 100 pF causes an experimental $|\Delta b|$ of around 2 mV, which is very similar to the value predicted by (7) (i.e., $|\Delta b| \approx$ 1.7 mV). This experimental $|\Delta b|$ corresponds to 0.32 pF, and hence, the attenuation factor is equal to 314 (= 100/0.32).

As for the linearity represented in Fig. 13, the results are very remarkable for the 10–100-pF range. Note that the maximum NLE (in absolute value) is 0.016, 0.009, and 0.020% FSS for C_p of 0, 100, and 200 pF, respectively. These values are significantly better (a factor between 5 and 12) than those obtained in Fig. 11 for the 1–10-pF range. This is probably thanks to the better accuracy of the impedance analyzer when measuring the actual value of capacitors in the 10–100-pF range.

E. Discussion and Comparison

The theoretical, simulation, and experimental results reported before have demonstrated that the sensitivity of the proposed front-end circuit does not depend on C_p. However, unlike [15], C_p does alter the offset of the I/O characteristic and, hence, a single-point calibration may be required. This limitation is because the applied active shielding does not completely eliminate the effects of C_p. Actually, C_p appears as a (negative) offset grounded capacitance with an attenuation factor that depends, among others, on k and ϑ. The closer the response of the IsoAmp to the ideal one (i.e., k = 1 and ϑ = 0°), the higher the attenuation factor. Consequently, the previous results could be improved using an IsoAmp with a higher accuracy (based on either the same or different

TABLE VI
COMPARISON STUDY BETWEEN CIRCUITS PROPOSED FOR GCS

Chip or reference	Circuit topology	Shielding	Measurement range (pF)	Max. NLE	Cable length	Circuit complexity	Sensitivity to parasitic capacitances
AD7147	ΣΔ modulator-based CDC	Active	[0, 20]	NR	Short	Medium	High
AD7747	ΣΔ modulator-based CDC	Active	[0, 16]	0.01% FSS	Medium	Medium	Medium [b]
[4]	DIC[a] measuring time intervals	NA	[100, 561·10^3]	0.03% at 100 pF	Very short	Low	High
[7]	AC bridge with sinusoidal excitation	Passive	[10, 110]	0.025%	Medium	Medium	High [c]
[14]	Charge-transfer based relaxation oscillator	Active	[10, 330]	0.03%	Long	Medium	Low [d]
[15]	Transformer-based circuit	Active	a) [0,10] b) [10,100]	a) 0.01% FSS at 0 m b) 0.006% FSS at 0 m	Long	High	Very low
[16]	Smart driving of the reference node	Active	[0, 10]	0.025% FSS at 1 m	Long	Medium [e]	Very low
[17]	MCU measuring time intervals	NA	[100, 225]	NR [g]	Very short	Low	High
[18]	Phase shifter-based circuit	NA	[100, 300]	NR [h]	Very short	Medium	High
[25]	Capacitance-to-frequency-to-DC voltage	NA	[100, 470·10^3]	Inherent non-linear response [i]	Very short	Medium	High
This work	IsoAmp-based circuit	Active	a) [1,10] b) [10,100]	a) 0.08% FSS at 0 m b) 0.016% FSS at 0 m	Medium	Medium	Low [f]

Abbreviations: NR: Not reported; NA: Not applicable.
[a] Direct interface circuit. [b] Strong performance degradation for a cable length longer than 2 m. [c] A manual adjustment of a capacitor is required to compensate for the offset caused by the cable. [d] Provided that a continuous 3-signal auto-calibration is carried out. [e] A differential-input LIA is required. [f] The cable capacitance slightly affects the I/O offset. [g] Error of 1.2 pF at 100 pF. [h] Error of 0.6 pF at 100 pF. [i] Error > 10% for $C_x < 6.8$ nF.

technology), but probably at the expense of a higher cost. Thus, as usually occurs in design, there is a tradeoff between cost and performance.

For comparison purposes, Table VI summarizes the main features of circuits suggested so far in the literature for GCS, including the circuit proposed herein. In terms of linearity, the proposed front-end circuit offers remarkable values, and these are quite independent of C_p. In comparison with the recent circuit proposed in [15], which relies on the same principle but implemented by a transformer, the circuit in Fig. 3 offers higher values of NLE, although these are comparable in the 10–100-pF range. However, the circuit in Fig. 3 is clearly less expensive, more compact, and more integrable than the transformer-based topology in [15]. The performance of the circuit suggested in [16] was slightly better than that proposed herein, but this required an LIA with a differential input for the reading of the output signal. In both cases (here and [16]), an isolated supply voltage is needed. In comparison with the low-cost solutions suggested in [4], [17], [18], and [25], the main advantage of the circuit proposed here is the ability to compensate for the effects of the parasitic capacitance of the interconnecting cable in case the GCS is remote. Note, in addition, that the circuits in [4], [17], [18], and [25] were not characterized for capacitances lower than 100 pF, which is the range where the effects of the parasitic components are higher. The commercial integrated solutions (such as AD7147 and AD7747) directly offer a digital output with information about the sensor capacitance, but again with limitations regarding the length of the interconnecting cable. In the opinion of the authors of this article, the concept of floating voltage source could be employed at the front-end circuit of the next generation of these integrated solutions to better compensate for the effects of long interconnecting cables.

VI. CONCLUSION

In this article, a novel front-end circuit for GCS has been proposed and then evaluated theoretically, by simulations, and experimentally. The core of the suggested front-end circuit is a floating voltage source implemented by an IsoAmp. According to the evaluation reported herein, the limitations

of the front-end circuit basically depend on the nonidealities of the IsoAmp. The closer its gain to one and phase shift to zero, the better the performance of the front-end circuit. Results using a commercial capacitive technology IsoAmp have shown the effects of its nonidealities on the I/O characteristic of the circuit when measuring capacitances of units and tens of picofarad. In comparison with the transformer-based counterpart, the circuit proposed herein has more limitations (especially, in terms of offset), but it offers a less expensive, more compact, and more integrable design solution. Industrial applications, such as the level measurement of a conductive liquid in a grounded metallic container, can benefit from the proposal of this new front-end circuit for capacitive sensors.

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