# Dual-Layer Proton Irradiation for Passive Component Enhancement and Noise Coupling Suppression on CMOS Process

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***Abstract*— This work presents the development of a dual-layer proton irradiation profile to decrease the fluence required to create a thermally stable localized high-resistivity silicon (HR-Si) substrate for on-chip passive component enhancement and to create a guard band to suppress noise coupling. Additional irradiation was done on the Si–$SiO_2$ interface to prevent conductive layer formation and reduce the main irradiation's fluence requirement. The thermally stable dual-layer profile was optimized experimentally by applying several interface and main irradiation fluence combinations to the on-chip inductor and comparing the quality factor before and after annealing. The optimum total fluence found for the dual-layer profile was $4 \times 10^{14}$ $cm^{-2}$ with a measured mask-edge margin distance of 22 $\mu$m, corresponding to 60% fluence reduction and 56% margin reduction compared to conventional proton irradiation with $10^{15}$-$cm^{-2}$ fluence. Adding a 20-$\mu$m-thick guard band formed by dual-layer proton irradiation between two circuits introduced 5-dB noise coupling suppression at 1 GHz, with a further 2.5-dB increase every time the thickness was doubled.**

***Index Terms*— CMOS, high-resistivity substrate, inductor, noise suppression, proton irradiation, silicon.**

## I. Introduction

HIGHER data rate requirements for the future 6G wireless communication standards and spectrum congestion below 10 GHz have pushed transceiver (TRX) research toward mm-wave [1] and sub-terahertz [2], [3] frequencies. At these frequencies, the size of passive components is reduced to the level where on-chip implementation of traditionally large passives, such as antennas or chip-to-waveguide transitions, is possible, enabling full on-chip system integration and eliminating losses due to chip-to-PCB interconnects [4], [5]. The implementation using CMOS processes has been demonstrated to be possible up to the frequency of 280 GHz [3], promising low cost, high integration capability with digital circuits, high yield, and large volume production capacity. However, the low-resistivity silicon substrate (around 10 Ω-cm) limits the performance of the on-chip passives implemented on the standard CMOS process. Bottom metal shielding [6], [7], [8] can be used to isolate the substrate from the passive component. However, the additional parasitic capacitance reduces the maximum operating frequency on some passives, and it cannot be implemented in components that require substrate interaction, such as an endfire antenna or a dielectric resonant antenna [9]. Switching to alternative substrates, such as high-resistivity silicon (HR-Si) [10], hollow silicon [11], and silicon-on-insulator (SOI) [12], requires new process development, device modeling, and preparation of new mass-production infrastructures, incurring additional costs than using the readily available CMOS processes.

Ion irradiation (see Fig. 1) creates a localized high-resistivity region by generating defects and charge traps [13], [14], [15], [16] to reduce carrier mobility on the substrate without modifying the existing chip manufacturing process. A nickel mask covers the active device area to prevent changes in characteristics and to eliminate the need for remodeling. The freedom to adjust the shape and location of the high-resistivity region also enables alternative applications, such as creating a high-resistivity guard band to suppress substrate noise coupling between two circuit areas. Compared with other ions, the proton has the lowest mass and can penetrate through the silicon substrate with a low-energy requirement, reducing the cost of the ion source and enabling the formation of high-resistivity regions with the same depth as the substrate thickness. The proton fluence

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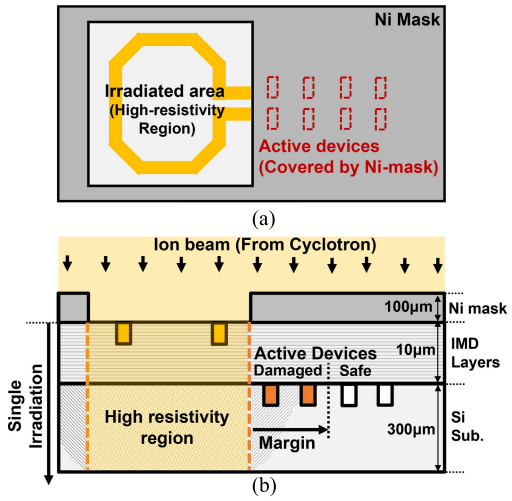


Fig. 1. (a) Top view and (b) cross-sectional view of the conventional ion irradiation setup.

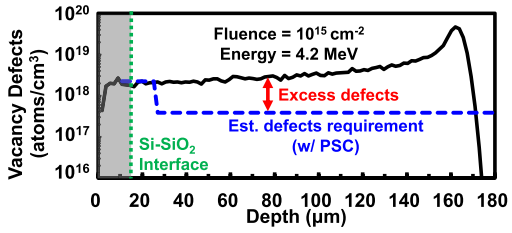


Fig. 2. TRIM simulation of vacancy defects of a single 4.2-MeV proton irradiation with $10^{15}$-cm$^{-2}$ fluence compared with estimated defect requirement after considering PSC effects.

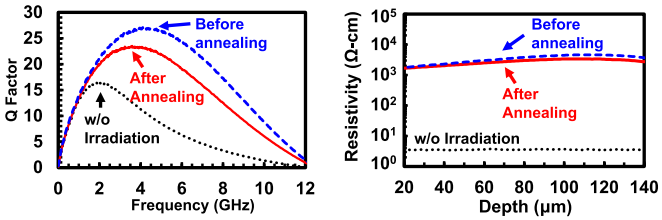


Fig. 3. Measurement results of (a) *Q*-factor of a 1.8-nH on-chip inductor manufactured in a standard 65-nm CMOS process and (b) resistivity of a CZ-P (100) 4-Ω-cm Si wafer. Both structures were irradiated with $4 \times 10^{14}$ – cm$^{-2}$ proton fluence and measured before and after 1-min 260 °C annealing.

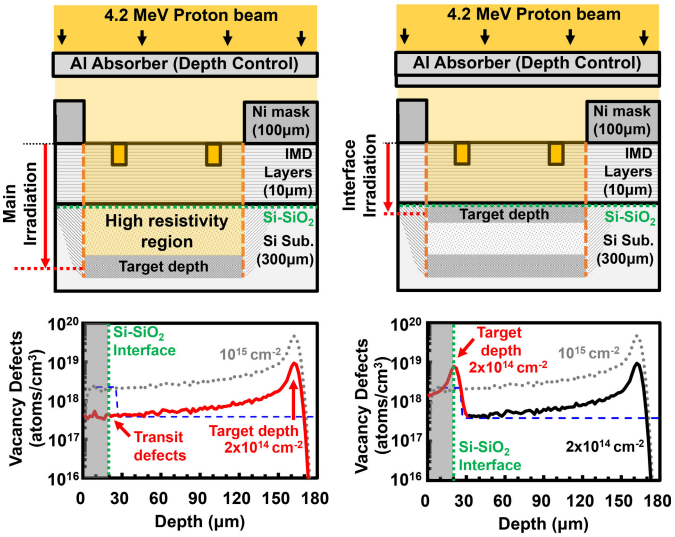


Fig. 4. Proposed dual-layer proton irradiation consists of (a) main irradiation and (b) interface irradiation. Expected defects generated by both steps were simulated with TRIM.

level needs to be tuned to prevent resistivity degradation due to high-temperature postprocessing, such as reflow soldering, which can reach up to 260 °C [17]. The previous proton irradiation studies [14], [15], [16] demonstrated that the fluence above $10^{15}$ cm$^{-2}$ was required to raise substrate resistivity from 10 Ω-cm to above 1 kΩ-cm and maintain it after 200 °C annealing. This high-fluence requirement leads to longer machine time and increased process costs. A margin distance of 50 $\mu$m to the mask edge was also required for proton irradiation to prevent radiation damage on active devices due to the scattered protons, which generates defects and charge traps at the oxides around the transistor, leading to performance degradation [18], [19]. Moreover, a large mask-edge margin creates an unusable area around irradiated components.

This work aims to reduce the fluence requirement and mask-edge margin distance of proton irradiation by investigating the parasitic surface conduction (PSC) effect, which was not considered in previous studies. Based on the investigation results, the dual-layer proton irradiation profile was proposed, and the fluence value was optimized to achieve thermal stability. The mask-edge distance of the optimized dual-layer profile was measured and compared with conventional irradiation. The effectiveness of a high-resistivity guard band formed using dual-layer proton irradiation for substrate noise coupling suppression was also characterized.

## II. PSC Effect on Proton Irradiated Substrate

PSC effect refers to the formation of a low-resistivity layer at the Si–$SiO_2$ interface due to the presence of fixed charges in the oxide, which attract free carriers to the interface. As a result, the effective substrate resistivity seen by passive components decreases by a factor of 10 to $10^4$ from its original value [20], [21], [22]. The PSC effect was overlooked in previous proton irradiation studies, because the PSC layer formation was naturally prevented by increasing the proton fluence until the transiting protons generated enough traps and defects to passivate the Si–$SiO_2$ interface. However, this leads to excess defects generated in the deeper part of the silicon substrate, where the PSC effect does not happen, and the defect requirement for thermal stability is not as high as the interface, as illustrated by the transport of ion in matter (TRIM) simulation in Fig. 2. The additional resistivity generated by this excess defect has minimal effect on passive component performance improvement, as substrate loss becomes negligible above 1-kΩ-cm resistivity. The single irradiation used by previous studies [14], [15] could not solve this issue due to the inability to independently adjust the defect generation at the interface and in the deeper region.

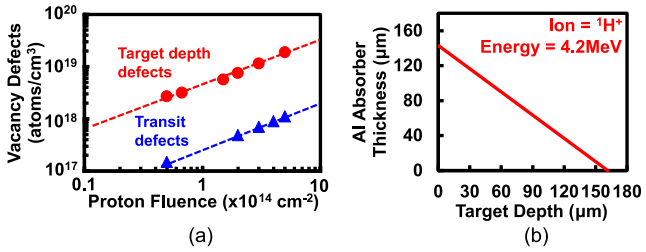


Fig. 5. TRIM simulation results of (a) defects generated at target depth and transit depth across different fluences and (b) relationship between Al absorber thickness and target depth.

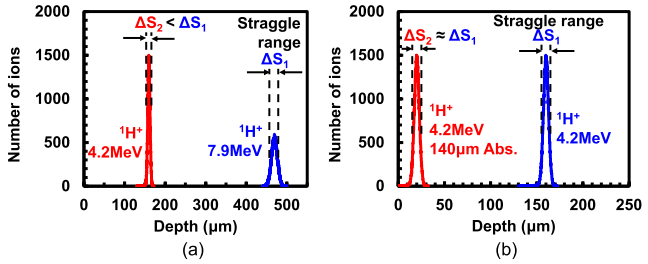


Fig. 6. TRIM simulation results of proton distribution after depth control through (a) changing proton energy and (b) changing Al absorber thickness.

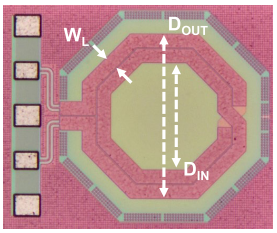


Fig. 7. Die micrograph of the on-chip two-turn 1.8-nH inductor manufactured in a standard 65-nm CMOS process used for irradiation profile optimization ($D_{IN} = 240$ $\mu$m, $D_{OUT} = 366$ $\mu$m, and $W_L = 30$ $\mu$m).

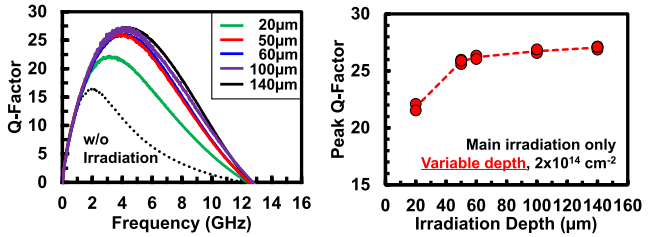


Fig. 8. Measurement results of inductor $Q$-factor across different main irradiation depths.

To demonstrate this phenomenon, a comparison was performed between the $Q$-factor measurement of a 1.8-nH on-chip inductor manufactured in a standard CMOS 65-nm process and the spread resistance profiling (SRP) measurement of a bare Czochralski p-type (100) Si wafer with 4-Ω-cm initial resistivity. Both structures were irradiated with $4 \times 10^{14}$-cm$^{-2}$ proton fluence and measured before and after 1-min 260 °C annealing. The $Q$-factor degradation after annealing observed in Fig. 3(a) indicates that the effective substrate resistivity seen by the inductor was not thermally stable. However, the direct resistivity measurement at the deeper region in Fig. 3(b) did not change after annealing. These results show that the proton fluence of $4 \times 10^{14}$ cm$^{-2}$ generated enough defects to maintain thermally stable resistivity at the deeper regions but did not generate enough defects to prevent PSC layer formation at the Si–$SiO_2$ interface, resulting in degraded inductor performance. Hence, the fluence must be increased to prevent PSC layer formation, resulting in the $10^{15}$-cm$^{-2}$ proton fluence requirement obtained in previous studies [14], [15] to achieve thermal stability.

## III. Dual-Layer Proton Irradiation

### A. Process Overview

To efficiently achieve the different defect requirements at the interface and deeper region, a dual-layer proton irradiation profile was proposed with process details shown in Fig. 4. The additional irradiation targeted at the interface utilizes the increased defect generation at the target depth compared with the transit depth [see Fig. 5(a)], which decreases the fluence requirement by up to a factor of 10 to generate the same amount of defects. The interface irradiation also removes the requirement on the main irradiation to generate interface defects, allowing reduction of the main irradiation fluence to the level required for the deeper region and eliminating excess defects generation. Target depth control was achieved by adjusting the Al absorber thickness according to the target depth, as shown in Fig. 5(b). This method was chosen over directly changing the proton energy due to a more linear relationship with target depth, a relaxed operating energy range requirement of the ion source, and no reduction in the ion straggle range at shallow target depth (see Fig. 6). A wider ion straggle range allows a larger tolerance of absorber thickness error due to manufacturing variation. The chosen 4.2-MeV proton beam energy has a maximum penetration depth of 160 $\mu$m and an ion straggle range of around 8 $\mu$m, which allows a maximum Al absorber thickness variation of ±4 $\mu$m before the defect concentration degrades by 50% from its peak value.

### B. Irradiation Profile Optimization

The values for main irradiation depth, interface irradiation fluence, and main irradiation fluence were optimized experimentally using indirect resistivity measurement through inductor $Q$-factor [23]. For these optimizations, several on-chip two-turn 1.8-nH differential inductors were fabricated using a 65-nm CMOS process (see Fig. 7). The optimum main irradiation depth was investigated by irradiating several inductors with $2 \times 10^{14}$-cm$^{-2}$ proton fluence at various depths and comparing the measured $Q$-factor. The measurement results in Fig. 8 show the optimum main irradiation depth between 60 and 100 $\mu$m with negligible $Q$-factor improvement at further depths, which is still within the penetration range of 4.2-MeV proton beam energy.

The minimum thermally stable fluence for interface irradiation was investigated by irradiating several inductors with various fluences at the interface while keeping the main irradiation constant at 100-$\mu$m depth with $2 \times 10^{14}$-cm$^{-2}$ proton fluence. The $Q$-factor was measured before and after 1-min 260 °C annealing to emulate the heat treatment of the lead-free reflow soldering process [17]. The measurement results in Fig. 9 indicate that at least $2 \times 10^{14}$-cm$^{-2}$ proton

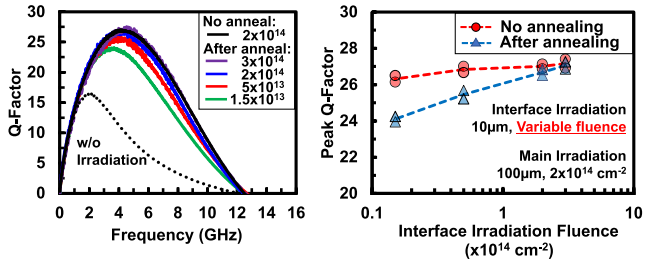


Fig. 9. Measurement results of inductor $Q$-factor across different interface irradiation fluences before and after 1-min 260 °C annealing.

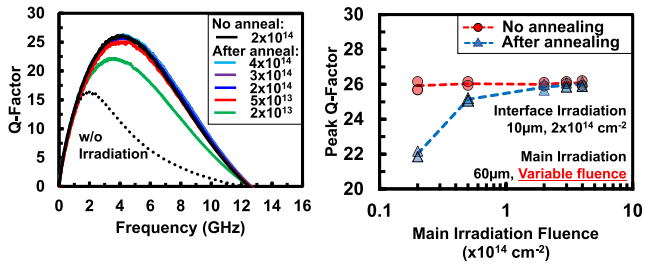


Fig. 10. Measurement results of inductor $Q$-factor across different main irradiation fluences before and after 1-min 260 °C annealing.

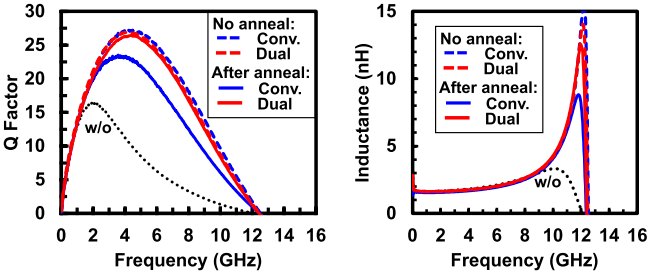


Fig. 11. Comparison of $Q$-factor and inductance measurement results of inductors irradiated with conventional and dual-layer profile listed in Table I before and after 1-min 260 °C annealing.

TABLE I
FINAL IRRADIATION PROFILE

| Condition | Energy (MeV) | Fluence ($cm^{-2}$) | Target Depth (μm) | Absorber (μm) |
|---|---|---|---|---|
| **Dual-Layer** | 4.2 | $2.0\times10^{14}$<br>$2.0\times10^{14}$ | 10 (interface)<br>100 (main) | 150<br>60 |
| Conventional (for comparison) | 4.2 | $4.0\times10^{14}$ | 160 | N/A |

fluence was required to prevent the PSC formation at the interface for 4.2-MeV proton energy. The minimum thermally stable fluence for main irradiation was investigated with the same method previously used on interface irradiation, with the interface irradiation kept constant at 60-$\mu$m depth and $2\times10^{14}$-$cm^{-2}$ proton fluence instead. The measurement results in Fig. 10 show that at least $2\times10^{14}$-$cm^{-2}$ proton fluence was required to prevent thermal resistivity degradation at the deeper region inside the substrate.

The optimized dual-layer irradiation profile is summarized in Table I. This final dual-layer profile was tested and compared with the conventional profile with the same total fluence on the on-chip inductor with measurement results shown in Fig. 11. From the measurement results, the proposed dual-layer proton irradiation profile was able to

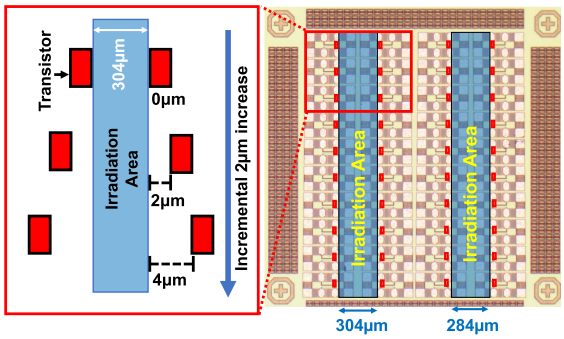


Fig. 12. Structure fabricated in a standard 180-nm CMOS to evaluate margin distance requirement from the mask edge (transistor parameters $W = 2$ $\mu$m, $L = 200$ nm, and finger $= 30$).

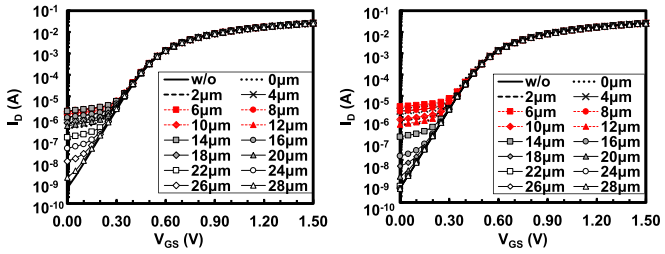


Fig. 13. Measured $I_D$–$V_{GS}$ characteristics of transistors within 0–28-$\mu$m distance from the mask edge after irradiation with (a) conventional and (b) dual-layer profile listed in Table I.

reduce postannealing peak $Q$-factor degradation from around 14% (27.1–23.3) in conventional irradiation to around 1% (26.8–26.5) at the same total fluence. This result also shows that the dual-layer proton irradiated substrate could achieve thermal stability with a total fluence of $4.0\times10^{14}$ $cm^{-2}$, a 60% reduction compared with conventional irradiation, where a fluence of $10^{15}$ $cm^{-2}$ is typically required for thermal stability [14], [15]. No change in inductance value and self-resonant frequency was observed, indicating that proton irradiation has a negligible effect on metal conductivity and dielectric permittivity of the oxide layer and the substrate.

## IV. ACTIVE DEVICE TO MASK-EDGE MARGIN DISTANCE

The structure shown in Fig. 12 was manufactured in a 180-nm CMOS process to measure the minimum margin distance required between the active device and the edge of irradiation area (mask edge) to prevent radiation-induced damage. The structure consists of 20 pairs of transistors placed at the mask edge, with a 2-$\mu$m incremental distance increase between each successive pair, covering a range from 0 to 28 $\mu$m. This transistor pair structure enables mask misalignment correction, and the margin distance can be measured with 2-$\mu$m resolution. The structure was irradiated with conventional and dual-layer profiles from Table I, with the $I_D$–$V_{GS}$ measurement result for both cases shown in Fig. 13. Damaged transistors were identified from the increase in leakage current at $V_{GS} = 0$. The leakage current was plotted over distances from the mask edge, as shown in Fig. 14, where the safe margin distance was determined from the minimum undamaged transistor distance. The measured margin distance for the optimized dual-layer proton irradiation profile was 22 $\mu$m, which is a 56% reduction compared with

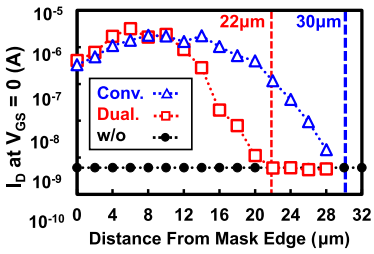


Fig. 14. Comparison of transistor leakage current at $V_{GS} = 0$ across all measured distances from Fig. 13 to determine the margin distance requirement of conventional and dual-layer proton irradiation.

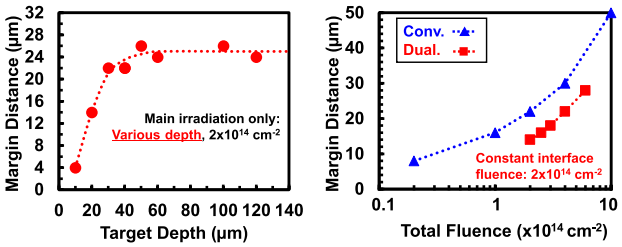


Fig. 15. (a) Measured margin distance across different target depths and (b) measured margin distance across different total fluences on conventional and dual-layer proton irradiation.

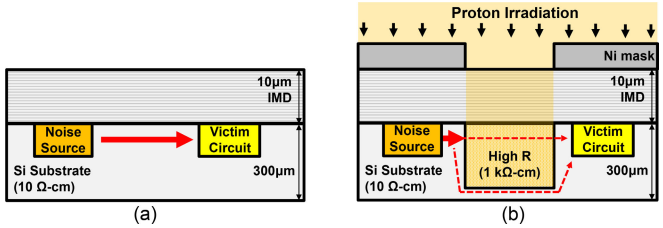


Fig. 16. Substrate noise coupling mechanism: (a) normal condition and (b) with high-resistivity guard band formed through irradiation.

the 50 $\mu$m required in thermally stable conventional proton irradiation with $10^{15}$-cm$^{-2}$ fluence [15] and a 26% reduction compared with the 30 $\mu$m required in conventional proton irradiation with the same fluence. To investigate the cause of improvement, the previous measurements were repeated with constant fluence across various depths and various total fluences for both conventional and dual-layer irradiation. Measurement results in Fig. 15(a) show that below 60 $\mu$m, the margin distance decreased in proportion to the target depth. In the dual-layer case, the margin distance caused by the interface irradiation at 10 $\mu$m was covered by the larger margin distance caused by the main irradiation at 100 $\mu$m. Therefore, the margin distance in dual-layer case was determined solely by the main irradiation fluence, which was only half of the conventional fluence for the profiles in Table I, resulting in margin distance reduction. Comparison between conventional and dual-layer cases measured in Fig. 15(b) also shows that the margin distance in the dual-layer case was similar to the conventional case when only the main irradiation fluence (total fluence minus interface fluence) was considered.

## V. Substrate Noise Coupling Suppression

The ability to control the location and shape of the irradiated area enables the creation of a high-resistivity guard band. As shown in Fig. 16, this guard band separates the

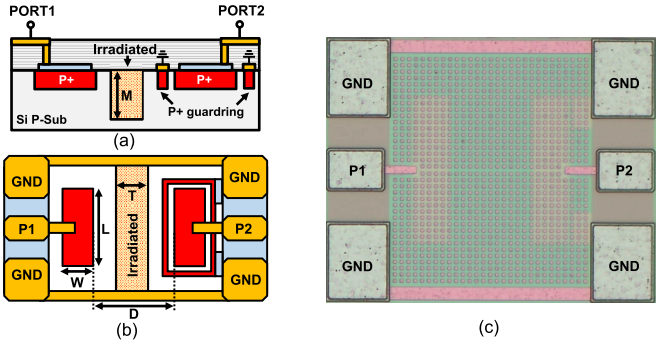


Fig. 17. Structure fabricated in a standard 65-nm CMOS process to evaluate noise coupling suppression ($W = 35$ $\mu$m, $L = 140$ $\mu$m, and $D = 100$ $\mu$m). The effects of guard-band thickness $T$ and depth $M$ on noise suppression were investigated.

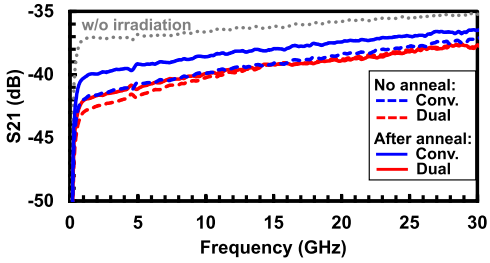


Fig. 18. Measured transmission coefficient of conventional and dual-layer guard band before and after 1-min 260 °C annealing.

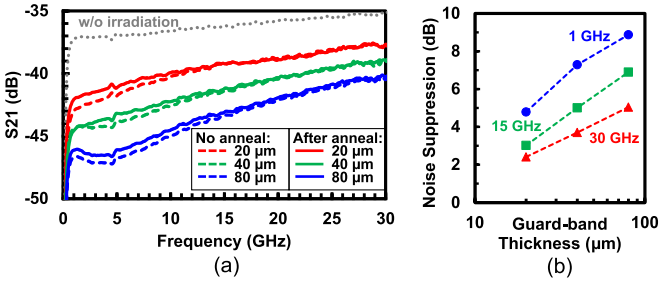


Fig. 19. (a) Measured transmission coefficient of dual-layer guard bands with different thicknesses ($T$) before and after 1-min 260 °C annealing and (b) summarized postanneal noise suppression measurement for different guard-band thicknesses at 1, 15, and 30 GHz.

noise-generating area from other parts of the chip, which helps to reduce substrate noise coupling. To investigate the noise suppression capability of the guard band, a two-tap structure was fabricated in a standard 65-nm process, with detailed dimensions shown in Fig. 17. A guard band with a specific thickness ($T$) and depth ($M$) was formed between the two taps through proton irradiation. The noise coupling between the two taps was measured through the transmission coefficient ($S21$) obtained from a network analyzer, and the noise suppression value was determined by comparing the $S21$ before and after the guard-band formation. The comparison of noise suppression and thermal stability performance between the guard bands ($T = 20$ $\mu$m) formed by conventional and dual-layer irradiation is shown in Fig. 18. Both cases achieved a similar 5-dB noise suppression at 1 GHz before annealing. However, the guard band in the dual-layer case maintained the 5-dB noise suppression after annealing, while in conventional case, the noise suppression degraded to 3 dB. This thermal behavior remains consistent for both cases until 30 GHz. However, as the frequency increases to 30 GHz,

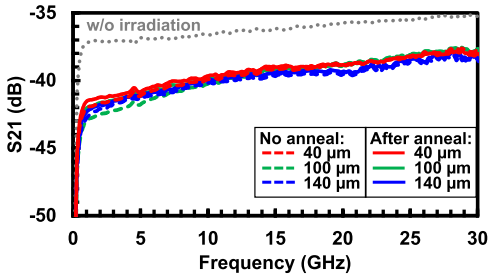


Fig. 20. Measured transmission coefficient of dual-layer guard bands with different main irradiation depths ($M$) before and after 1-min 260 °C annealing with interface irradiation parameters kept constant.

the postanneal noise suppression gradually decreased to 1.5 dB for the conventional case and 3 dB for the dual-layer case. The impact of guard-band thickness ($T$) and guard-band depth ($M$) on noise suppression was examined on the guard bands created through dual-layer proton irradiation. Fig. 19 shows the measured noise suppression across $T$ values from 20 to 80 $\mu$m. The results indicate an additional increase of 2.5-dB noise suppression for each doubling of $T$ at 1 GHz, which gradually decrease to 2 dB at 15 GHz and 1 dB at 30 GHz. The effect of $M$ on noise suppression was investigated by changing the main irradiation depth from 40 to 140 $\mu$m, while keeping the interface irradiation condition constant at $2 \times 10^{14}$-cm$^{-2}$ fluence and 10-$\mu$m target depth. Measurement results in Fig. 20 show negligible change in noise suppression when the main irradiation depth was varied between 40 and 140 $\mu$m.

## VI. Conclusion

In this article, the dual-layer proton irradiation profile was formulated from PSC analysis and successfully optimized to reduce the total fluence requirement to achieve thermal stability. The optimized dual-layer profile reduced the total fluence requirement by 60%, from $10^{15}$ cm$^{-2}$ in conventional irradiation to $4\times10^{14}$ cm$^{-2}$, leading to a proportional reduction in machine operational time and energy costs. The reduction in the total fluence requirement also reduces the mask-edge margin distance requirement from the active devices by 56%, from 50 to 22 $\mu$m, increasing the available area for design. The guard-band formation using dual-layer proton irradiation to suppress substrate noise coupling from the noise-generating area has been demonstrated, resulting in 5-dB noise coupling suppression at 1 GHz for 20-$\mu$m-thick guard band, with a further 2.5-dB increase every time the thickness was doubled.

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