High-Field Transport and Statistical Variability of Nanosheet Oxide Semiconductor FETs With Channel Length Scaling

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***Abstract*— We have investigated the scaling potential of nanosheet oxide semiconductor FETs (NS OS FETs) for monolithic 3-D (M3D) integration in terms of atomic layer deposition (ALD) material engineering, high-field transport, and statistical variability. We have developed and systematically compared InGaO (IGO), InZnO (IZO), and InGaZnO (IGZO) FETs by ALD. The effective mobility (μ_{eff}) characteristics of IGZO are higher than that of IGO and IZO at the same threshold voltage (V_{th}) in the normally-OFF region ($V_{th} > 0$). IGZO benefits from high μ_{eff} of IZO and low oxygen vacancy (V_o) of IGO and thus shows well-balanced characteristics. To study the carrier transport characteristics under a high electrical field, we have fabricated sub-100 nm gate length NS OS FETs and extracted transconductance (g_m) as a metric. While bulk Si FETs show velocity saturation behavior even after parasitic correction, NS OS FETs show unsaturated velocity behavior. We also have obtained statistical variability data of NS OS FETs, which is comparable against bulk Si nFETs and Si SOI nFETs. This work provides evidence of the scalability of NS OS FETs for M3D integration.**

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***Index Terms*— Atomic layer deposition (ALD), high-field transport, monolithic 3-D (M3D), nanosheet (NS) FET, oxide semiconductor (OS), scalability, statistical variability.**

I. Introduction

TODAY'S ever-growing AI applications demand high-performance computing and high memory bandwidth. Because of the power constraint, energy-efficient computing is necessary. However, the conventional von Neumann architecture faces challenges in data transfer between processor and off-chip memory due to the limited bandwidth and high-power consumption in dense memory access. Particularly, the energy cost for data transfer between memory and computing units is relatively high and has to be reduced. In-memory computing (IMC) and near-memory computing (NMC) with an embedded memory are promising solutions to address these issues [1], [2], [3]. Recently, several candidates have been proposed for embedded memory applications such as eDRAM [4], RRAM [5], and MRAM [6]. Although memory elements are placed in a back-end-of-line (BEOL) layer in a conventional embedded memory architecture, access transistors are located in a front-end-of-line (FEOL) layer. Such embedded memory needs extra area other than processors, which is not area-efficient [7], [8].

Monolithic 3-D (M3D) integration architecture aims to place the memory array including access transistors in the BEOL layer. Such M3D integration of memory arrays on a computing unit can significantly improve the memory access bandwidth, achieve high-density integration, and minimize energy cost for data transfer because of its proximity [9] (Fig. 1). In order to realize 3-D monolithic integration of memory units, BEOL-compatible transistor technology is needed. Then, oxide semiconductor (OS) is a promising channel material because of its high mobility, low leakage, and high thermal stability [10], [11], [12], [13], [14]. OS has been widely utilized in flat panel display (FPD) products as thin-film transistor backplanes. The first practical device using amorphous IGZO as a channel material was reported in 2004, which demonstrated high mobility, transparent, and flexible OS TFT fabricated at room temperature [11]. To deposit OS material, sputtering is conventionally used, but it does not

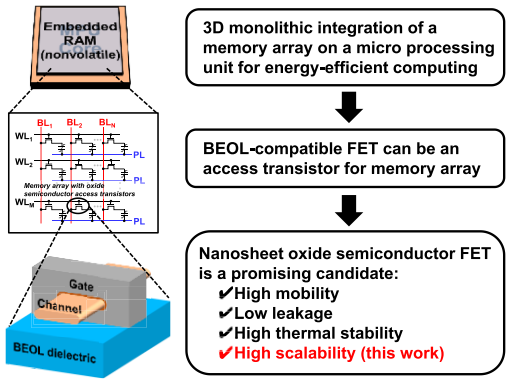

Fig. 1. Schematic illustration of the motivation of this work. The scalability of NS OS FET is studied for M3D integration.

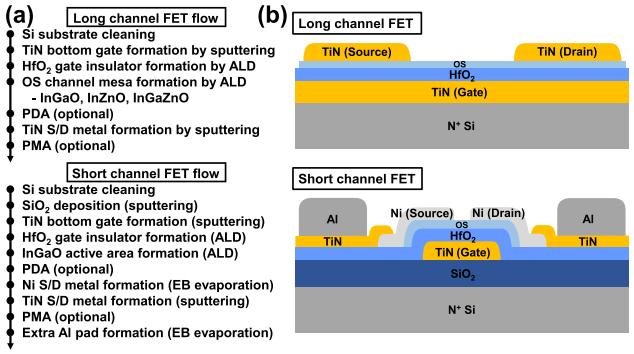

Fig. 2. (a) Device fabrication process flow and (b) Cross-sectional schematics of the fabricated FETs. OS materials are deposited by ALD. EB lithography and evaporation are used for source/drain formation in SC FETs.

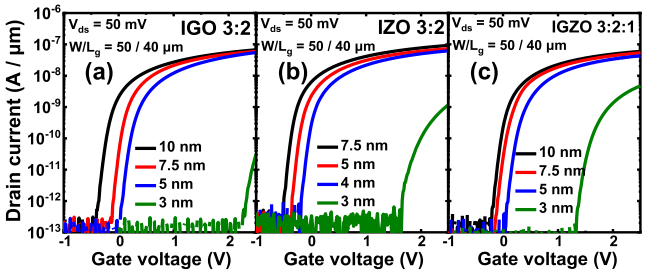

Fig. 3. Measured I_d–V_g curves of the fabricated LS OS FETs with different channel thicknesses. (a) In:Ga = 3:2, (b) In:Zn = 3:2, and (c) In:Ga:Zn = 3:2:1 Sound subthreshold characteristics and expected thickness dependence were observed.

meet the requirements of uniformity and conformality on 3-D structures for LSI applications. Recently, atomic layer deposition (ALD) has been getting attention as a promising method for uniform OS thin film deposition [15], [16], [17], [18], [19].

For high-density memory applications, the scalability of OS FETs is an important issue to be addressed. Although promising device characteristics have been demonstrated in short channel (SC) OS FETs with nanosheet (NS) OS [20], [21], [22], [23], [24], [25], key aspects of high-field transport and statistical variability are not fully explored yet. A systematic study on high-field transport of scaled OS FETs is needed for performance prediction. In addition, statistical variability in OS FETs should be studied for high-volume manufacturing.

In this work, we developed ALD IGO, IZO, and IGZO processes, and fabricated FETs to systematically investigate device characteristics with the channel thickness and composition ratio dependence. We also fabricated SC OS FETs and discussed the scaling potential of NS OS FETs in terms of high-field carrier transport and statistical variability. This article is an extended version of the conference abstract [26], providing more detailed descriptions and comprehensive statistical variability studies of NS OS FETs by comparing them to both Si bulk and Si SOI nFETs.

II. Device Fabrication

We developed a device fabrication process flow of long-channel (LC) and SC NS OS FETs with bottom gate structure using ALD, as shown in Fig. 2(a). Fig. 2(b) shows the cross-sectional schematics of LC and SC NS OS FETs. Both devices have a TiN bottom gate, HfO_2 gate insulator, and OS channel. TiN is deposited by RF reactive sputtering. A 15-nm HfO_2 is deposited by ALD at 250 °C for the gate insulator. OS was deposited by thermal ALD using alkyl-based precursors at 250 °C. Triethyl-indium, triethyl-gallium, and diethyl-zinc with O_3 oxidant were used as precursors for InO_x, GaO_x, and ZnO_x, respectively. For the growth sequence of OS, one or more sub-cycles of InO_x were deposited first, followed by one or more sub-cycles of GaO_x and/or ZnO_x forming one super-cycle of the OS growth. The composition ratio was controlled by varying the ratio of sub-cycles of each material and the film thickness is controlled by varying the number of super-cycles. The highest temperature of the baseline process was 300 °C at post-deposition anneal (PDA), which is compatible with the BEOL process. EB lithography and lift-off process were used for Ni S/D electrode formation of the SC OS FETs. Post-metallization anneal (PMA) was done after TiN S/D extension metal deposition at 250 °C. We also fabricated two test chips. One test chip has various gate lengths (L_g) of OS FETs from 60 nm to 1 μm for L_g dependence study. The other test chip has >1k OS FETs with the same L_g of 60 nm for statistical analysis. For reference, we also prepared wafers of the foundry's 65 nm bulk Si FETs and SOI Si FETs [27].

III. Results and Discussion

A. ALD Material Engineering

First, we systematically investigated ALD-grown IGO, IZO, and IGZO FETs as a continuous work from our previous report [14]. We varied the channel thickness and composition ratio to investigate the optimal conditions for each OS material. Fig. 3 shows typical drain current (I_d)–gate voltage (V_g) curves of IGO, IZO, and IGZO FETs with different thicknesses. All devices were measured in an enclosed probe station with dry-air or N_2 purge conditions. The composition ratios for IGO, IZO, and IGZO FETs are In:Ga = 3:2, In:Zn = 3:2, and In:Ga:Zn = 3:2:1, respectively. All devices show good subthreshold characteristics. V_{th} of all OS FETs increases as OS thickness decreases due to the channel pinch-off operation in junctionless FETs.

Fig. 4 summarizes the device characteristics of subthreshold swing (SS), μ_{eff}, V_{th}, and V_{th} shift (ΔV_{th}) by positive gate

bias stress (PBS). In this work, the PBS test was conducted by applying five consecutive V_g sweeps, with V_g being swept from -3 to 3 V for each sweep [15]. As for composition ratio dependence, μ_{eff} increases with high In% because InO_x forms an electron conduction path with high carrier concentration [28]. As Ga% or Zn% increases, while SS is maintained, V_{th} increases and μ_{eff} decreases down to 5 nm OS thickness by suppressing oxygen vacancy (V_o). IGO tends to have positive V_{th} but also shows large ΔV_{th} by forming subgap trap states due to excess oxygen [29], [30] induced by oxygen-rich ALD process with O_3 oxidant [15]. On the other hand, IZO tends to have negative V_{th} but shows smaller ΔV_{th} and higher μ_{eff} than IGO. As Zn has less oxygen binding energy than Ga, IZO has more V_o and thus higher conduction than IGO [31], and also has less excess oxygen and thus less subgap trap state formation. IGZO has shown well-balanced characteristics between IGO and IZO. While maintaining high mobility, V_{th} tends to be positive and ΔV_{th} is small. For channel thickness less than 5 nm, all OS FETs show large V_{th} and ΔV_{th} and degraded SS and μ_{eff} partly due to the subgap state formation associated with quantum confinement [32], which is the challenge of NS OS FETs.

Fig. 5 summarizes μ_{eff} versus V_{th} as well as ΔV_{th} for all different composition ratios and channel thicknesses of NS OS FETs. It shows a clear tradeoff between μ_{eff} and V_{th} for OS FETs. In the normally-OFF region ($V_{th} > 0$), IGZO FETs show higher V_{th} and higher μ_{eff} than IGO and IZO FETs. IGZO benefits from high μ_{eff} of IZO and low V_o of IGO and thus shows well-balanced characteristics.

B. High-Field Transport in NS OS FETs

Next, we studied the carrier transport characteristics of scaled OS FETs under a high electrical field. We fabricated both LC and SC IGO FETs with varied Ga% and 8 nm-thick IGO NS. Fig. 6 shows the top-down SEM image of the source/drain electrodes for $L_g = 50$ nm. The clean lift-off process and narrow-gap formation with a physical L_g of 50 nm were obtained. Fig. 7 shows the cross-sectional TEM images and the corresponding EDX mapping of the fabricated SC IGO FET. The uniform deposition of ALD IGO and SC formation was confirmed. In addition, a sharp interface was formed between HfO_2 and IGO without significant interdiffusion. Fig. 8 shows the I_d–V_g curves of the LC and SC IGO FETs for different Ga%. Note that all devices have very low leakage current because of the thick HfO_2. Both LC and SC FETs show good subthreshold characteristics. The SC FETs with sub-100 nm L_g show larger ON-current than the LC FETs. In addition, V_{th} reduction by SC effect and drain-induced-barrier-lowering (DIBL) were observed in the SC FETs for different Ga%. The I_d–V_d curves of the LC and SC IGO FETs are shown in Fig. 9. Drain currents show a quadratic increase for both LC and SC OS FETs, which indicates that velocity saturation is not dominant yet for SC IGO FETs. In addition, the larger output conductance in the SC FET was caused by DIBL.

Fig. 10 shows the V_{th} roll-off curves of IGO FETs, which are nearly the same for all Ga% when the effective gate length is below 100 nm. Note that we first extracted gate length

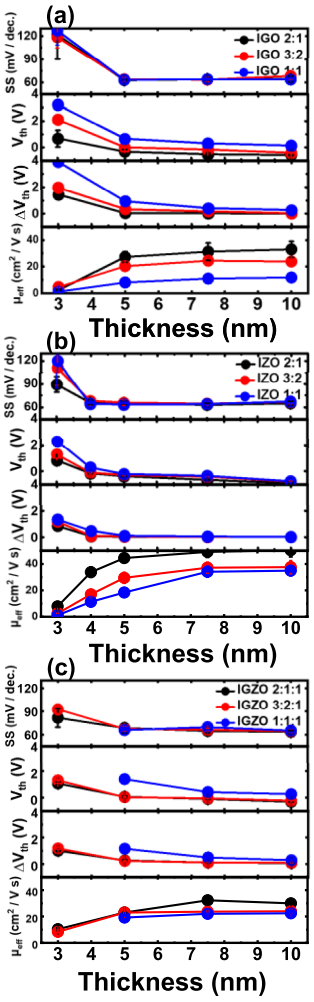

Fig. 4. Extracted SS, V_{th}, ΔV_{th}, and μ_{eff} from the measurement of the fabricated LS OS FETs with different channel composition and thickness for (a) IGO, (b) IZO, and (c) IGZO. Device characteristics are maintained down to the 5 nm thickness of the OS channel.

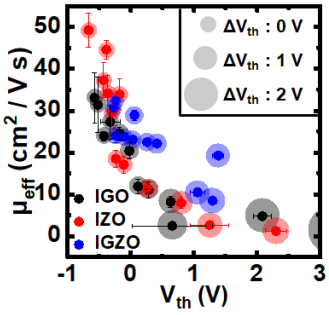

Fig. 5. Trade-off of μ_{eff}, V_{th}, and ΔV_{th} in IGO, IZO, and IGZO FETs with different compositions and thicknesses.

offset (ΔL) for all Ga% FETs by extrapolation method and then obtained the effective gate length. As In% increases, the effective gate lengths are found to decrease, and DIBL increases, which can be due to redox reactions at interfaces between the channel layer and electrode layers. The equivalent oxide thickness (EOT) of IGO FETs is as thick as 4.9 nm to suppress parasitic leakage current. This causes early roll-off which, however, can be overcome by scaled EOT.

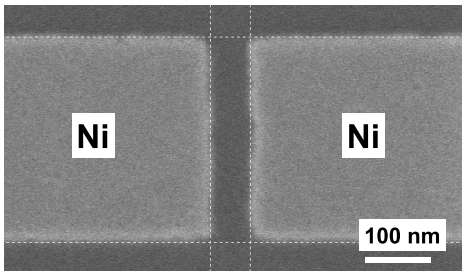

Fig. 6. Top-down SEM image of the S/D Ni electrodes of the fabricated SC FET. The physical L_g of this device is 50 nm.

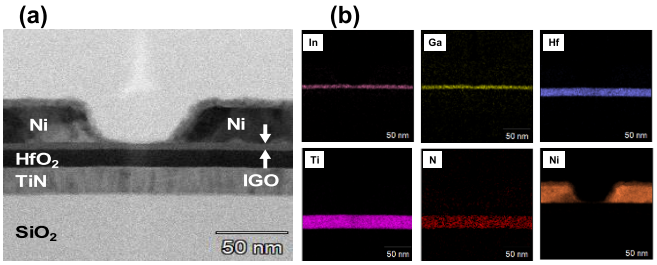

Fig. 7. (a) Cross-sectional TEM images and (b) EDX mapping of the fabricated SC IGO FET.

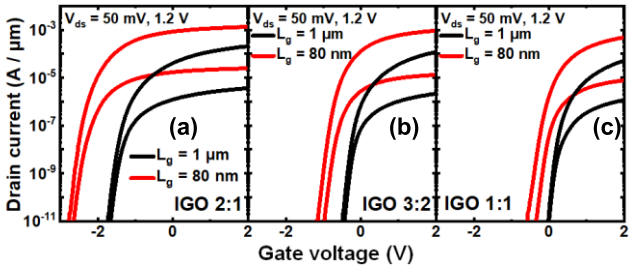

Fig. 8. Measured I_d–V_g curves of the fabricated SC (red) and LS (black) IGO FETs with (a) In: Ga = 2:1, (b) In:Ga = 3:2, and (c) In:Ga = 1:1.

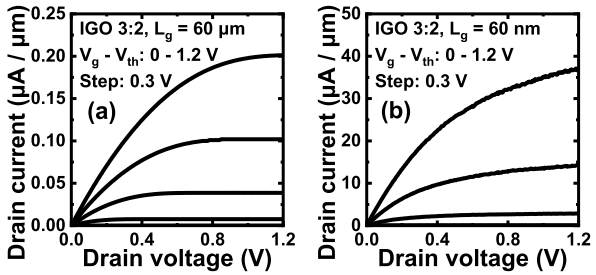

Fig. 9. Measured I_d–V_d curves of (a) LS and (b) SC IGO FETs. Both drain currents show a quadratic increase, while the SC FET shows larger output conductance by DIBL.

Next, we discussed the high-field carrier transport of IGO FETs. Transconductance (g_m) is used as a metric. Fig. 11 illustrates the method to correct g_m by external resistance and extract intrinsic g_m (g'_m) [33]. Based on this method, we studied the L_g dependence of g_m and g'_m for different Ga% IGO FETs and bulk Si FETs as shown in Fig. 12. g_m and g'_m are indicated by open symbols and solid symbols, respectively. Note that the reference bulk Si FETs were fabricated by

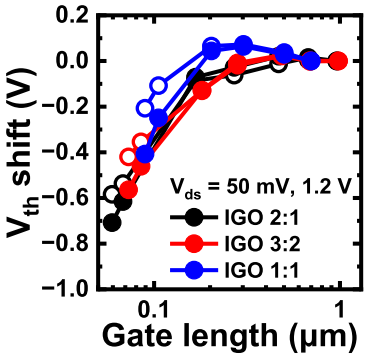

Fig. 10. V_{th} roll-off characteristics of all Ga% IGO FETs in both linear (open) and saturation regions (solid).

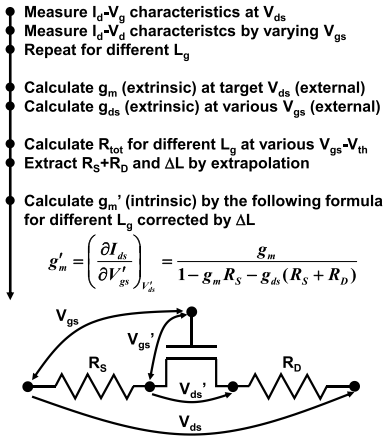

Fig. 11. Calculation method for intrinsic g_m value by correcting parasitic resistance from g_m [33].

foundry 65 nm bulk technology. In the linear region at V_d = 50 mV, g'_m of both NS IGO FETs and bulk Si FETs are inversely proportional to the gate length. However, in the saturation region at V_d = 1.2 V, g'_m of bulk Si FETs show a nonlinear relationship with gate length, whereas all Ga% NS IGO FETs shows a good linear fit to L_g^{-1}. This indicates that, while bulk Si FETs show velocity saturation behavior even after parasitic correction, NS OS FETs show unsaturated velocity behavior. This can be explained by the relatively low mobility of OS materials. Hot electrons are less likely to be generated in the OS FET because of relatively low velocity. Thus, OS FETs in this work may show less susceptibility to inelastic phonon scattering and velocity saturation, unlike Si FETs. I_d–V_d curves in Fig. 9 show quadratic increment even for the SC IGO FET, which is consistent with the unsaturated velocity behavior. Thus, OS FET performance can get closer to Si FET by further L_g scaling and parasitic resistance reduction. Further experiments and characterizations will be needed to elucidate the high-field transport physics in extremely scaled OS FETs.

C. Statistical Variability of NS OS FETs

Next, we studied the statistical variability of scaled NS IGO FETs and conducted a comparative study of NS IGO FETs and Si CMOS FETs.

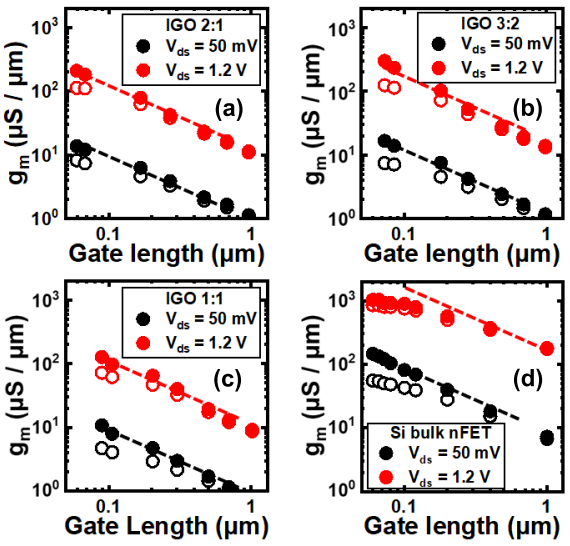

Fig. 12. Measured (open symbols) and corrected (solid symbols) transconductance of (a) In:Ga = 2:1, (b) In:Ga = 3:2, (c) In:Ga = 1:1, and (d) bulk silicon FETs in both linear (black) and saturation (red) regions. A correction was made by using the method in Fig. 11. While bulk Si FETs show velocity saturation behavior, IGO FETs show unsaturated velocity behavior.

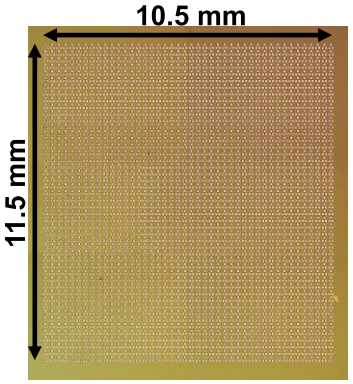

Fig. 13. Top-down microscope image of the fabricated TEG with >1k NS OS FETs of L_g = 60 nm and W_{ch} = 140 nm.

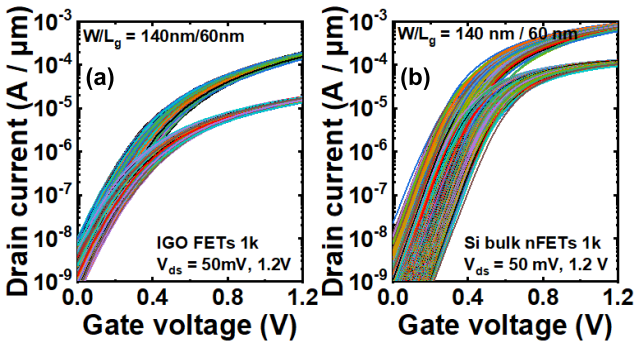

Fig. 14. Measured I_d–V_g curves of (a) 1024 NS IGO FETs and (b) 1024 Si bulk nFETs at V_{ds} = 50 mV and 1.2 V. NS IGO FETs show good subthreshold characteristics and tight V_{th} distribution with less DIBL.

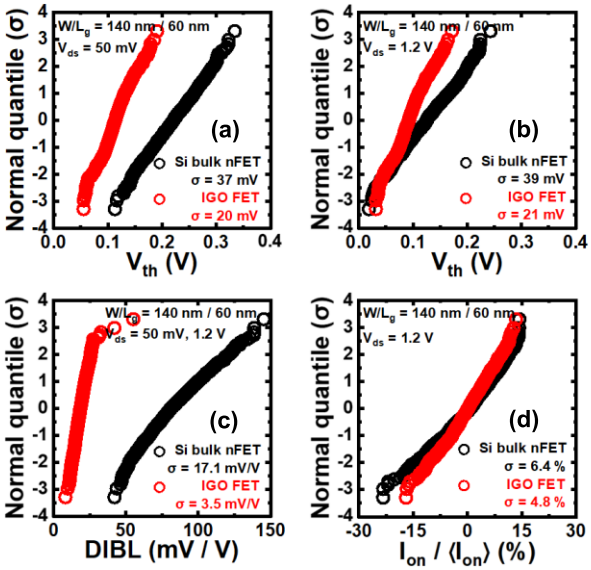

Fig. 15. Cumulative distribution of (a) V_{th} (linear region), (b) V_{th} (saturation region), (c) DIBL, and (d) $I_{on}/\langle I_{on}\rangle$. Compared to Si FETs, V_{th} has a tight distribution, average DIBL and σ are small, and I_{on} also has a tight distribution in IGO FETs.

We fabricated the test chip of 1k (1024) NS IGO FETs with designed L_g of 60 nm, channel width (W_{ch}) of 140 nm, and channel thickness of 7.5 nm in our university lab. The composition ratio of NS IGO FETs is In:Ga = 3:2. Fig. 13 shows the top-down microscope image of the test chip. L_g and W_{ch} of Si FETs are 60 and 140 nm, respectively. Note that the physical L_g of SC IGO FETs is about 50 nm by SEM. The EOT of NS IGO FET is 4.9 nm, which is about 2.3 nm thicker than the reference bulk Si FET to suppress parasitic gate leakage. In addition, contact size and contact resistance are different. Fig. 14 shows the I_d–V_g curves of 1k IGO FETs and Si bulk nFETs. SC IGO FETs show normally-OFF operation, good subthreshold characteristics, and high drive current. Both IGO FETs and bulk Si FETs show variation in terms of V_{th}, DIBL, and I_{on}. The I_d–V_g curves of NS IGO FETs show tighter V_{th} distribution than those of bulk Si FETs.

Fig. 15 shows the cumulative distributions of V_{th}, DIBL, and normalized I_{on} by the mean value $\langle I_{on}\rangle$ for NS IGO FETs and bulk Si FETs. V_{th} is defined as the constant current method at normalized $I_{ds} = 10^{-9}$ A. Tight V_{th} distributions of IGO FETs with σ = 20 and 21 mV are obtained in linear and saturation regions, respectively. These results are comparable to those of bulk Si FETs. The V_{th} of IGO FETs does not completely follow a straight line because systematic variability other than random variability still remains. The small average DIBL value of 18.7 mV/V and tight distribution with σ = 3.5 mV/V are obtained in IGO FETs, which are much smaller than bulk Si nFETs. Normalized I_{on} of IGO FETs has σ = 4.8%, which is 1.6% smaller than bulk Si nFETs. These results can be due to the thin-body structure with well-controlled donor concentration (~10^{17} cm^{-3}) in NS IGO by suppressing V_o.

It is well-known that FD SOI MOSFETs with undoped channels have much smaller V_{th} variability than bulk MOSFETs due to the absence of random dopant fluctuation [27], [34], [35]. Therefore, we also conducted a comparative study of NS IGO FETs and Si SOI nFETs. The SOI layer is undoped and SOI thickness is 13 nm. Fig. 16 shows the I_d–

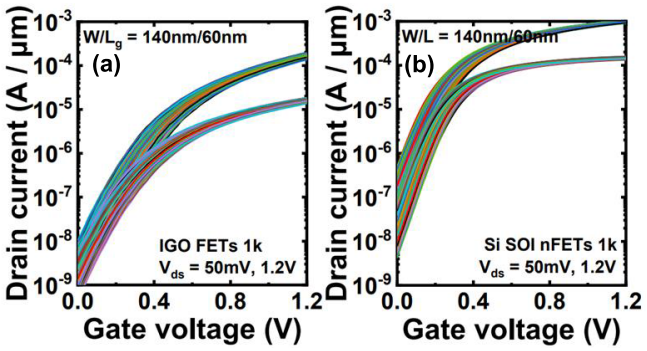

Fig. 16. Measured I_d–V_g curves of (a) 1024 IGO FETs and (b) 1024 SOI nFETs at V_{ds} = 50 mV and 1.2 V. Both NS IGO FETs and SOI nFETs show tight distributions of V_{th}, DIBL, and normalized I_{on}.

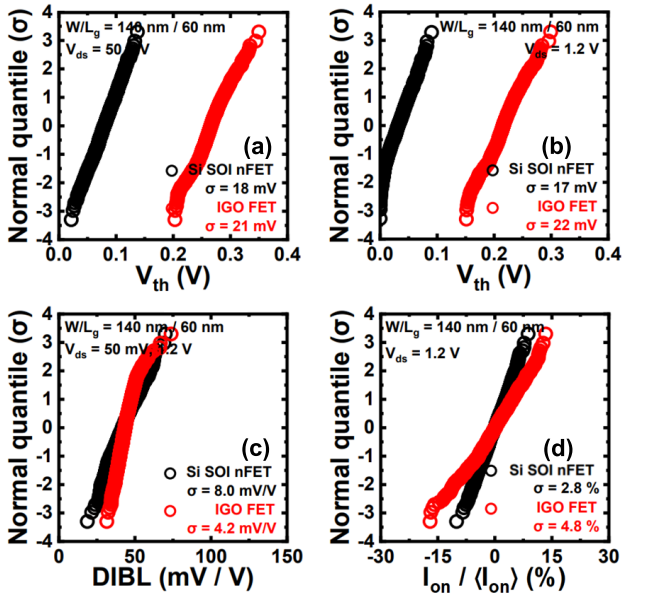

Fig. 17. Cumulative distribution of (a) V_{th} (in linear region), (b) V_{th} (in saturation region), (c) DIBL, and (d) $I_{on}/\langle I_{on}\rangle$. Si SOI nFETs show smaller variation than NS IGO FETs in terms of V_{th} in the linear and saturation region and normalized I_{on}.

V_g curves of 1k IGO FETs and Si SOI nFETs. Compared to bulk Si nFETs in Fig. 14(b), SOI nFETs show well-controlled variability in normalized I_{on}, V_{th}, and DIBL. In addition, good subthreshold characteristics, high drive current, and less DIBL were obtained in SOI nFETs. Fig. 17 shows the cumulative distributions of V_{th}, DIBL, and normalized I_{on} by the mean value $\langle I_{on}\rangle$ for NS IGO FETs and SOI FETs. Note that we used normalized $I_{ds} = 10^{-8}$ A for V_{th} extraction by the constant current method. Si SOI nFETs show tight V_{th} distributions with $\sigma = 18$ and 17 mV in linear and saturation regions, which are smaller than those of NS IGO FETs. Normalized I_{on} of Si SOI nFETs has $\sigma = 2.8\%$, which is 2% smaller than NS IGO FETs. These results show that, although SOI nFETs have better variability control than NS IGO FETs, the difference is not significant. In addition, tight DIBL distributions were obtained in NS IGO FETs with $\sigma = 4.2$ mV/V, which is smaller than Si SOI nFET. Generally, NS OS FETs show comparable or better variability control than Si bulk nFETs and SOI nFETs, which is encouraging for high-density M3D integration.

IV. Conclusion

We developed and systematically compared ALD-grown IGO, IZO, and IGZO FETs. IGZO benefits from high μ_{eff} of IZO and low V_o of IGO and thus shows well-balanced characteristics. We fabricated sub-100 nm L_g NS OS FETs and demonstrated unsaturated carrier velocity behavior. The performance of NS OS FETs can get closer to that of Si FETs as L_g is scaled down. We obtained statistical variability data of NS OS FETs, which is comparable to Si CMOS. The study on high-field transport and statistical variability in NS OS FETs with channel length scaling demonstrated the scaling potential of these devices. This work provides evidence of the scalability of NS OS FETs for 3-D LSI applications.

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