Stochastic Resonance in HfO_2-Based Memristors: Impact of External Noise on the Binary STDP Protocol

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***Abstract*— This article deals with the stochastic resonance (SR) phenomenon experimentally observed in HfO_2-based memristors. The SR impact on the binary spike time-dependent plasticity (STDP) protocol at the device level was investigated. We demonstrate that the two extreme conductance states of the device that represent the synaptic weights in neuromorphic systems can be better distinguished with the incorporation of Gaussian noise into the bias signal. This technique allows setting the memristor conductance which is directly related to the overlap between the pre- and postsynaptic pulses. The study is reproduced in the LTSPICE simulator using the dynamic memdiode model (DMM) for memristors.**

***Index Terms*— Memristor, resistive random access memory (RRAM), spike time-dependent plasticity (STDP), stochastic resonance (SR).**

I. Introduction

THE scientific community and microelectronics industry are highly interested in novel and emerging technologies for RAM memory devices [1], [2]. In this regard, memristors have exceptional properties, including low power consumption and high integration capacity among others. Memristor's conductance can be changed when exposed to a suitable biasing scheme. When bias disappears, memristor's conductance is maintained in a nonvolatile fashion. This makes the memristor a very promising device to be used in a huge range of applications, such as data storage, unconventional computing methods, artificial neural networks (ANNs), and cryptography [3], [4], [5], [6]. Memristors present nonlinear current-voltage characteristics and nonlinear dynamical behavior enabling the utilization of properties linked with nonlinear systems. Despite the noise in electronics is considered as a major drawback and commonly needs to be eliminated, in nonlinear systems it can play a favorable role, such as enhancing the device performance or, in the particular case of memristors, modifying the switching phenomenon. This phenomenon is often referred to as stochastic resonance (SR) and it has been observed in several research fields including biology, physics, and engineering [7], [8], [9], [10]. A detailed description of the well-known SR phenomenon is reported in [11]. SR occurs in nonlinear devices whose characteristic curves present thresholds, like occurs in memristors. From the literature, some works have considered noise as a beneficial element in these devices. For instance, in [12] the impact of additive noise in memristors was investigated using a physical model of a memory resistor. A different SR modeling for manganite-based memristors is presented in [13], which reports good concurrence between theory and measurements. An experimental investigation was conducted in [14], where memristors were exposed to sinusoidal signals with added noise to examine SR. In [15], a study of the effect of the SR in the resistance ratio of HfO_2-based memristors is discussed. In [16], a noisy signal was applied to zirconium and tantalum pentoxide-based memristors. The analysis from both experimental and theoretical viewpoints and the constructive role of noise in these samples is reported. In addition, SR in 2-D materials-based memristors is analyzed in [17].

The use of memristor-based ANNs has gained increasing importance in recent years due to their potential to implement efficient and low-power computing architectures [18]. In neuromorphic systems, the aim consists in reproducing brain performance. In this sense, spike-timing-dependent plasticity (STDP), which is a learning approach inspired by biology, it is widely accepted in the scientific community as a way to describe the brain synapse when implemented with resistive random access memory (RRAM) devices [19]. The STDP process updates the synaptic weight and direction as a function of the time difference or delays between the pre- and postsynaptic spikes [20], [21]. In the specific case of the memristor-based

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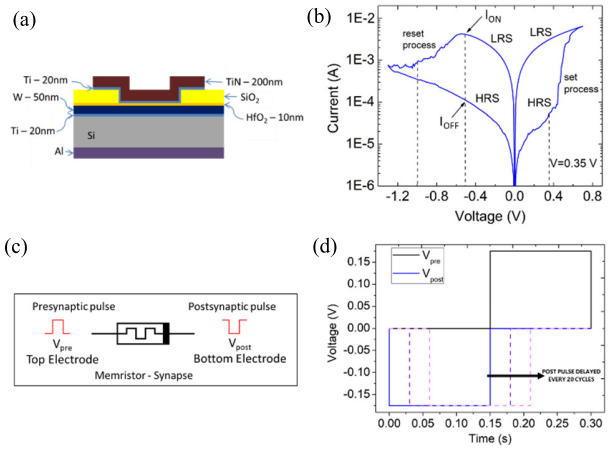

Fig. 1. (a) Device structure and (b) example of a current-voltage characteristic of the memristors studied in this work. (c) Memristor schematics presenting the applied pulses (pre- and postsynaptic) at the top and bottom electrodes, respectively. (d) Initial situation of the applied pre- and postsynaptic pulses (no overlap) is represented with continuous lines. Different situations with delay of the postsynaptic pulse are presented in dash lines.

binary STDP, the resistive switching process is essential for the achievement of the two different states: ON and OFF, which correspond to the memristor low resistance (LRS) and high resistance (HRS) states, respectively [22], [23] (Fig. 1).

Even though ANNs are assumed to work with no noise or spike jitter, neurobiological systems are known to operate in noisy environments. Thus, noise can tune the activation threshold of neurons, enhancing the response of nonlinear circuits. Anderson et al. [24] reported that noise produced in the visual cortex facilitates the perception of the optical signal. In [25], an increase in neuron sensitivity efficiency is reported, ascribing it to the SR effect.

The aim of this work is to experimentally study in detail the role of noise in the binary STDP implemented with HfO_2-based memristors, considering the set, reset, and complete set-reset processes, extending our preliminary work in [26] where only the set process was addressed. In this case, an improvement of the STDP protocol was observed when noise was added under different circumstances considering noise in both memristive state transitions separately and jointly. Moreover, after this analysis, we show that the study of the constructive role of noise in the binary STDP can be reproduced using the LTSPICE simulator with the help of the dynamic memdiode model (DMM) [27], [28]. The external signals with noise were applied to the device and the simulation results were compared with the experimental data.

II. Noise-Induced Binary STDP

This section focuses on the SR effect on memristor-based binary STDP learning rule implementation. The devices used in our study are metal-insulator-metal (MIM) structures consisting of TiN-Ti-HfO_2-W layers, as shown in Fig. 1(a). These devices were fabricated on silicon. The HfO_2 layer was deposited via atomic layer deposition (ALD). A 50 nm-W layer acts as the bottom electrode and a 200 nm-TiN layer over a 20 nm-Ti layer acts as oxygen-gettering material (top electrode). The Al layer at the wafer bottom performs as the bottom contact of the memristors in the wafer. The used devices are square cells with an active area of $5 \times 5\ \mu m^2$. For more information regarding the fabrication process visit [29]. The semiconductor parameter analyzer (SPA) Agilent 4156C was utilized to carry out measurements. The experiments were programmed and launched in MATLAB. Fig. 1(b) represents the typical I–V characteristics after the electroforming event (using a 1 mA current limitation) for the memristors analyzed in this section [30]. Now, the voltage sweeps were from 0 to 0.7 V, 0.7 to −1.3 V, and −1.3 to 0 V. The current was also read simultaneously to the voltage application. During measurements, the current limitation was fixed to 25 mA to avoid any eventual irreversible breakdown of the dielectric film.

In the analysis of the external noise impact on binary STDP, when no noise is applied, the memristor state is ensured not to change. However, the application of noise allows the memristor to switch, activating the set and/or reset processes.

We study binary STDP via the SR phenomenon following three different approaches: 1) activating the set process; 2) activating the reset process; and 3) activating both set and reset processes simultaneously.

To provoke binary STDP, the memristors were subjected to set and reset pulses to reach ON and OFF states, respectively. First, all the set and reset pulses are formed from a pre-synaptic pulse (V_{pre}) applied to the top electrode of the device and a postsynaptic pulse (V_{post}) applied to the bottom electrode. The resultant voltage drop at the memristor reads: $V_{tot} = V_{pre} - V_{post}$ as illustrated in Fig. 1(c). The width of the pre- and postsynaptic pulses was always 150 ms. In addition, we consider two different types of set and reset pulses: fixed and variable. The fixed ones consist of a constant pulse with a voltage amplitude high enough to ensure the memristor state transition. The more complicated variable pulses follow an adaptive pulsewidth scheme that is detailed in the following sections. Depending on each investigated case, the set and reset pulses can be fixed or variable, and with or without noise addition. After completing every transition pulse (set or reset), the memristor conductance state was determined by means of a read voltage pulse, V_{read}, of 150 ms duration applied to the top electrode of the device and grounding the bottom one. In our case $V_{read} = -0.5$ V to ensure a clear separation between HRS and LRS. The complete sequence of applied signals will be presented in the corresponding section.

A fresh device was used for each experiment (one for measuring without noise and one for the noisy measurement). The added noise, for all the different considered test conditions, was Gaussian ($\sigma_{noise} = 150$ mV), which was found to be the suitable value for the SR observation in these samples, after analyzing different values. The resistance ratio is calculated as follows: $R_{ratio} = (R_{Reset}/R_{Set}) = ((V_{Read}/I_{Reset})/(V_{Read}/I_{Set})) = (I_{Set}/I_{Reset})$, where I_{Set} and I_{Reset} consist of the registered currents during the read pulse after the set and reset pulses, respectively. The following sections summarize the information about the complete applied signal and the results corresponding to the three different tests.

A. Set Process Activation

In this first approach, the focus is to improve the binary STDP with the addition of Gaussian noise to the pulse that provokes the set transition. We ensure that the memristor remains in the HRS state by selecting appropriate amplitudes

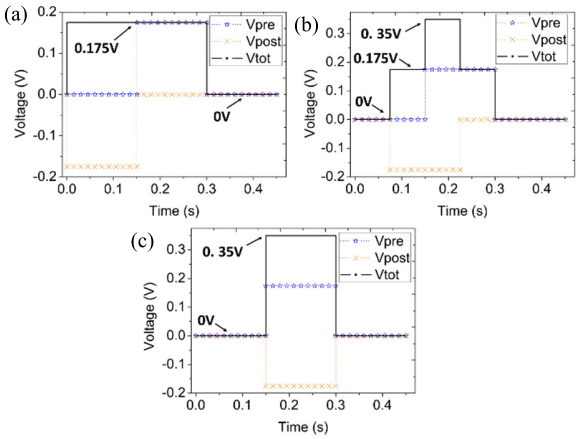

Fig. 2. Total set voltage, V_{tot}, (black line) and pre- and postsynaptic pulses (blue and orange lines) for three different overlap cases (a) no overlap, (b) intermediate, and (c) complete.

for the pre- and postsynaptic pulses without external noise. For this reason, we selected a set voltage, $V_{tot} = V_{set}$, slightly below the voltage required to activate the set transition. This ensures that once the noise is added, there is a probability of overcoming the set threshold voltage. In this study, we set the maximum voltage to $V_{set} = V_{tot} = 0.35$ V.

To induce a change from LRS to HRS, we generate a reset pulse by applying -0.5 V at the top electrode and 0.5 V at the bottom electrode. Thus, the reset pulse consists of $V_{reset} = V_{tot} = -1$ V during 150 ms.

However, generating the set pulse, V_{set}, is more challenging because the postsynaptic pulse must allow for adaptive time-shifting to generate different overlap situations between the pre- and the postsynaptic pulses. This overlap induces the maximum value of V_{set} to have different values. In Fig. 1(d), the initial situation of the pre- and postsynaptic pulses is illustrated. Notice that there is no delay between pulses. The dashed lines in the figure represent the successive delays of the postsynaptic pulse.

For a better understanding, we describe the details of a variable set pulse generation. The duration of the set pulse at a maximum voltage (0.35 V) starts at 0 ms, goes up to 150 ms and drops back to 0 ms following 15 ms steps. Fig. 2 illustrates three cases for a variable set process: (a) the pre- and postsynaptic pulses are not overlapped producing a 300 ms pulse of $V_{set} = V_{tot} = 0.175$ V; (b) a partial overlap situation that generates a three-level voltage pulse. In this situation, the maximum $V_{set} = V_{tot} = 0.35$ V was during approx. 60 ms; and (c) a complete pulses overlap, where $V_{set} = V_{tot} = 0.35$ V pulse that lasts 150 ms [26].

In Fig. 3(a), the complete measurement sequence for this first approach is reported. In every postsynaptic pulse delay (Δt), the sequence is cycled 20× to allow for statistical analysis. At the beginning of the measurement sequence, the pre- and postsynaptic pulses do not overlap, and the 20 cycles are performed. The postsynaptic pulse is then delayed 15 ms, and again the 20 cycles are executed. This process is repeated for each shift. $\Delta t = n \times 15$ ms, where n starts at 0 and grows until 21. Focusing again on Fig. 2(a) presents the initial situation where $n = 0$. As Δt increases, the overlap grows until

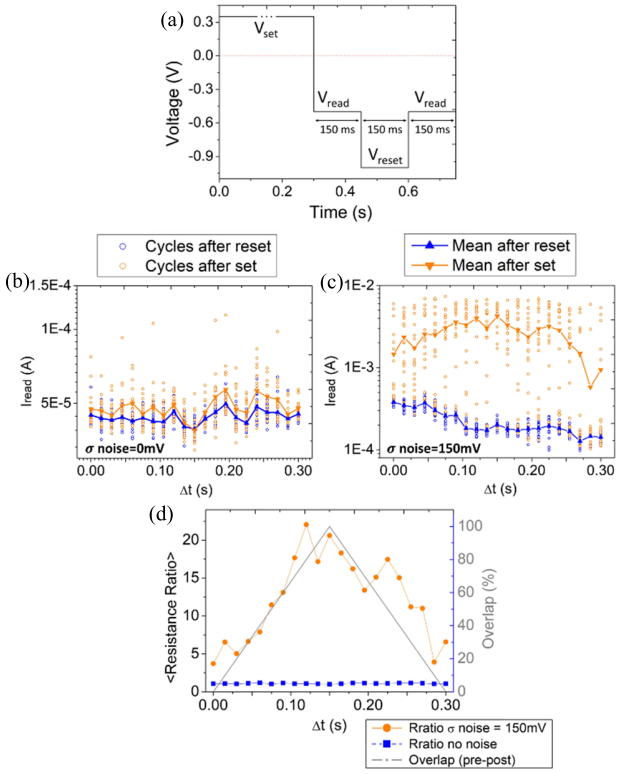

Fig. 3. Set process activated via noise addition. (a) Complete applied signal for this study during one cycle. The maximum value timespan of V_{set} pulse varies every 20 cycles. The current during the 20 cycles for each Δt and mean current evaluated after a set transition, in orange, and after a reset in blue is presented in (b) for the measurements without noise and in (c) including noise ($\sigma = 150$ mV). (d) Mean value of R_{ratio} against Δt is presented. For the measurements without including noise, in blue, and with noise, in orange.

a maximum situation in (c) for $n = 11$. After the maximum overlap situation, n keeps growing until there is no overlap again, for $n = 21$.

The currents for the 20 cycles after each set and reset processes in all the previously mentioned iterations are illustrated in Fig. 3(b) and (c) against Δt for experiments without considering noise and including it, respectively. Orange symbols represent the read currents after a set transition and the blue ones after a reset transition. In addition, in the figures, the mean value of the read current is shown with a solid line of the same color as the respective symbols. The comparison of both figures reveals that noise addition is crucial in identifying resistive states. Without noise, there is no state separation [see Fig. 3(b)]. However, with noise addition, both ON and OFF states are clearly distinguished because the set transition is enhanced. This state separation is proportional to the overlap between pre- and postsynaptic pulses. It is important to highlight that the maximum overlap situation is shown at $\Delta t = 150$ ms. Fig. 3(d) displays the mean resistance ratio as a function of Δt for the measurements without (in blue) and with noise (in orange). The dashed gray line in Fig. 3(d) represents the overlap as a function of Δt, which supports the analysis reported in Fig. 3(b) and (c). about the proportionality between pre- and postsynaptic pulses overlap and the R_{ratio}. In conclusion, the addition of noise to the set transition improves the R_{ratio}.

B. Reset Process Activation

This section presents the opposite situation to the previous approach. Set pulses are fixed while reset pulses are variable. Now, it is the reset process the one intended to be activated via noise addition. Hence, the applied voltages have the opposite sign with respect to case A. The set pulse maximum voltage is fixed to a voltage high enough to ensure the transition to the LRS. Now, the pre- and postsynaptic pulses consist of 0.3 and −0.3 V pulses, respectively, resulting in a 150 ms pulse of $V_{set} = V_{tot} = 0.6$ V, which is the same in all cycles and iterations. However, the complexity appears now in the reset voltage, but the methodology used for its generation is the same as that considered in the previous section resulting, in this case, in a negative voltage pulse with a maximum value $V_{reset} = V_{tot} = -0.55$ V. This value is below the voltage required to activate the reset process. The noise intensity is the same as in the previous section ($\sigma_{noise} = 150$ mV). Here, the delay is in the postsynaptic pulse for the reset process, generating a different overlap condition every 20 identical cycles. In this section, the noise is applied during the reset process.

As reported in the previous section, Fig. 4(a) shows one cycle of the applied signal for this reset process activation, where the set process is a fixed pulse and the reset pulse is variable, changing every 20 cycles, as mentioned above. Fig. 4(b) illustrates an example of a medium overlap situation between the pre- and postsynaptic pulses to form the reset pulses in this section and highlights the resulting voltage values. Fig. 4(c) and (d) shows the currents measured after every transition and cycle as a function of Δt for the experiments without and with noise, respectively. Again, the noise allows the device to switch, but in this case from LRS to HRS with a switching probability proportional to the overlap. This trend is confirmed by the results shown in Fig. 4(e), where the R_{ratio} of the two different situations (with and without noise inclusion) is shown as a function of the postsynaptic pulse delay. The figure includes the dashed gray line showing the overlap evolution as a function of the delay as well. Once it is demonstrated that both set and reset processes can be activated separately with the addition of noise, the key part of this work is to combine both activations simultaneously. This study is presented in the following section.

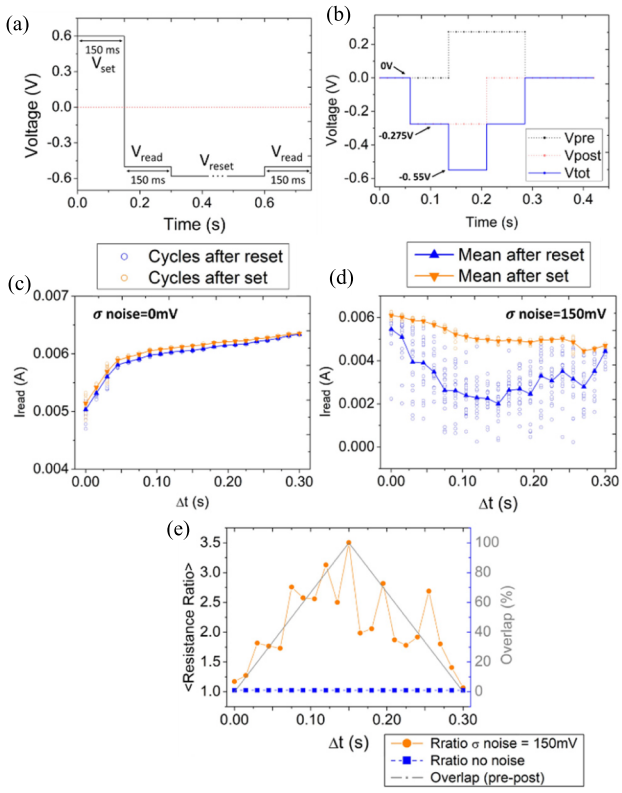

Fig. 4. Reset process activated via noise addition. (a) Complete applied signal for this study during one cycle. (b) Medium overlap situation between the pre- and postsynaptic pulses to build the variable reset pulse. The maximum value timespan of V_{set} pulse varies every 20 cycles. The current during the 20 cycles for each Δt and mean current evaluated after a reset transition, in orange, and after a reset in blue is presented in (c) for the measurements without noise and in (d) including noise ($\sigma = 150$ mV). (e) Mean value of R_{ratio} against Δt is presented. For the measurements without including noise, in blue, and with noise, in orange.

C. Complete Switching Activation

In this section, the combination of the two previous studies is presented. This is the most realistic situation where a system is always driven by a noisy signal. Hence, both set and reset processes will be under noise influence. The applied voltages are $V_{set} = V_{tot} = 0.38$ V and $V_{reset} = V_{tot} = -0.58$ V. Both values are not sufficient to activate the switching. The same noise ($\sigma_{noise} = 150$ mV) was applied. The slight set and reset voltage value differences with respect to the previous sections are a consequence of the inherent device-to-device (D2D) variability. These particular values were selected so as to achieve an initial condition as similar as possible for all the experiments. From the results in several devices (∼25), we identified the optimal voltage ranges to be: V_{set} from 0.35 to 0.4 V and V_{reset} from −0.55 to 0.6 V. In the same line as in the previous sections, Fig. 5 summarizes the experimental study carried out. Fig. 5(a) illustrates the applied voltage signal where both set and reset durations are variable. A key point for the set and reset pulses timing in this section is that the evolution of the pre- and postsynaptic pulses duration is synchronized. This means that the timespan of the maximum value in both set and reset pulses is the same (i.e., the same overlap), for all the cycles. Fig. 5(b) and (c) presents the measured current after every set and reset transition against Δt for the experiments without noise and including it, respectively. The added noise enables both transitions simultaneously. In this section, the overlap between pre- and postsynaptic pulses evolves equally in both set and reset transitions.

It is worth mentioning that there are differences in the resistance ratio values obtained with the three approaches [see Figs. 3(d), 4(e), and 5(d)] described above. In the first approach, where the set process is activated by noise, the maximum resistance ratio value is approximately equal to 20. In the second approach, where the reset process is activated, the maximum value is around 3.5, and in the third approach, with both transitions activated, the maximum value is 9. The resistance ratio differences observed in the three sections can be ascribed to the widely known intrinsic memristor variability, the selection of noise sigma, and the voltage values for the constant pulses for reset and set transitions in Sections II-A and II-B, respectively. The predominant factor is the different abruptness of the set and reset processes in the

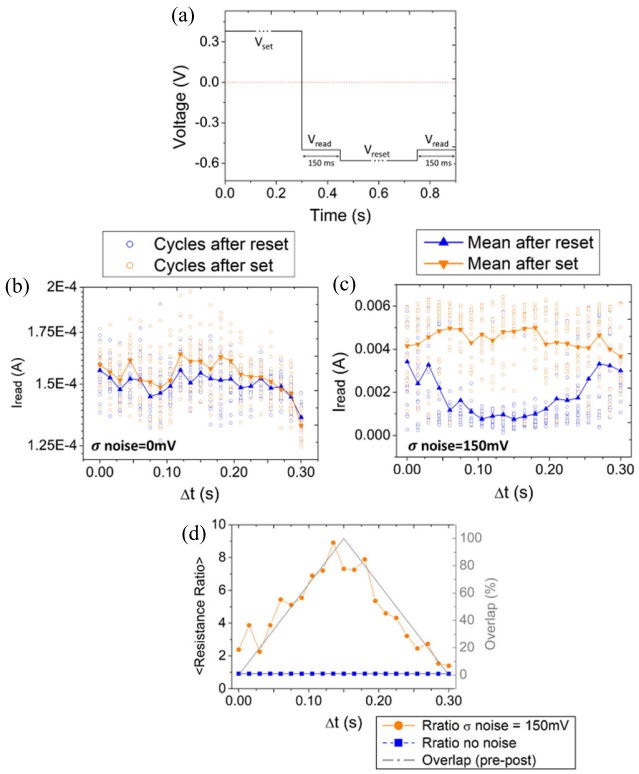

Fig. 5. Set and reset processes activated via noise. (a) Presents the complete applied signal during one cycle. The duration of the maximum values of V_{set} and V_{reset} is the same. The current during the 20 cycles for each Δt and mean current evaluated after a set transition, in orange, and after a reset in blue is presented in (b) for the measurements without noise and in (c) including noise ($\sigma = 150$ mV). (d) Mean value of R_{ratio} against Δt is presented. For the measurements without including noise, in blue, and with noise, in orange.

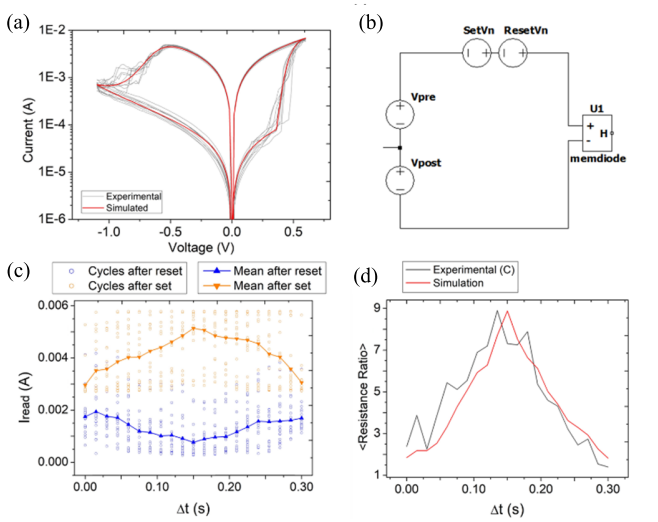

Fig. 6. (a) Comparison of the experimental (gray) and fit (red) I–V characteristics. (b) LTSPICE circuit schematics used to simulate STDP activation via SR. (c) Simulated current during the 20 cycles for each Δt and mean current evaluated after a set transition, in orange, and after a reset transition in blue including noise obtained using the LTSPICE simulator and the DMM model. (d) Experimental (gray) and simulated (red) resistance ratio against Δt showing a good agreement between both curves.

used memristors. Regarding the last issue, in the I–V curve shown in Fig. 1(b), the set process is notably more abrupt than the reset process, which is gradual. Hence, the noise activation of the set (Section II-A) allows an HRS ratio after a complete reset process. However, for Section II-B, the resistance ratio values are lower because of the progressiveness of the reset process; therefore, noise does not allow a large resistance state change during this process.

In this section, a comprehensive investigation into the SR effect within neuromorphic systems utilizing memristors was presented. The study highlighted the positive impact of noise on the binary STDP protocol. Through the strategic introduction of noise in either the set pulse, reset pulse, or both simultaneously, we demonstrated the switching activation. The experiments detailed in this study were replicated using other devices from the same wafer to verify the consistency and reproducibility of the results.

III. Simulating STDP Activation via SR

As part of this study, we report in what follows simulation results using the LTSPICE simulator. The goal is to reproduce the same input signal used for the third and more complex approach presented and to analyze the response of the memristor provided by the considered model. For the simulations, we have used the DMM [27], [28] for RRAM devices, which has demonstrated high versatility for a wide variety of input signals [31], [32]. In this work, the model will be tested with complex and noisy signals. The DMM is implemented in LTSPICE, and it basically consists of two main equations, one for the current-voltage characteristic and another for the memristor memory state. Detailed information about the model and applications can be found in [27] and [28].

Before the simulations, setting the model parameters is a necessary step. The procedure consisted of selecting the model parameters that reproduce the behavior of the devices used in this work, which are obtained by fitting the experimental data to the model equations. The result of this fitting process is shown in Fig. 6(a), where the I–V curves corresponding to ten experimental cycles (in gray) are compared to a simulated curve (in red). In addition, Fig. 6(b) presents the schematics of the LTSPICE circuit used for the simulations containing four voltage sources: the pre- and postsynaptic pulses (V_{pre} and V_{post}), and the noise sources for the set and reset processes (SetVn and ResetVn, respectively).

The complex signals were generated in LTSPICE using the piecewise linear (PWL) function, where time and voltage can be programmed point by point, while the white Gaussian noise signal is added externally. Once the pulsed signals are generated, the noise is included in the transitions, the simulations run, and the results are externally compiled and analyzed in MATLAB. The results reported in Fig. 6(c) (symbols) show the reading current after every set (in orange) and reset (in blue) transitions versus the Δt for a simulation including noise. The continuous line corresponds to the mean value of the LTSPICE simulation. The HRS and LRS reading current values and dependence on the postsynaptic pulse delay obtained through simulation show that the model is able to reproduce the experimental behavior. Fig. 6(d) compares the experimental and simulated resistance ratio against Δt. The simulations demonstrate the binary STDP protocol can be activated through external noise addition in LTSPICE, showing a good agreement between experimental and simulated results.

IV. Conclusion

In this work, the beneficial effect of the addition of an external noise source to the base signal in the performance of HfO_2-based memristors was experimentally demonstrated. We reported a complete experimental study of the SR in STDP protocol implemented with memristors, showing the beneficial role of additive noise on the binary STDP protocol. Our study analyzes the SR phenomenon in a scenario where the memristor's HRS and LRS were not distinguishable. Nevertheless, we have demonstrated that by including noise to the set pulse, reset pulse, or both pulses simultaneously, the resistive switching was activated. The slight impact of the D2D variability forces to definition of a narrow range of input signals for the set and reset transitions activation. The results unveiled the impact of noise was different for the set and reset transitions, being more evident for the set transition. This effect was attributed to memristor variability, noise sigma, selected set, and reset voltage values and to the abruptness of the set event compared with the more gradual reset event. We assessed the positive impact of noise by examining the relationship between the resistance ratio and the duration of the highest value of the noise-triggered transition pulse. Our findings showed that as the duration of the maximum noise-activated transitions (set, reset, or both) increases, the resistance ratio also increases, the case where both (set and reset) transitions were noise-activated was simulated using the DMM in LTSPICE. The obtained results well reproduce the experimental observations. The presented results are promising and offer a potential avenue for further exploration of the SR phenomenon in more complex neuromorphic systems. This includes using multiple memristors for experimental analysis and simulation of ANNs.

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