Circular Architecture for Excellent Uniformity in Amorphous Indium–Gallium–Zinc-Oxide Thin-Film Transistors

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***Abstract*— We report high-performance amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistors (TFTs), in which both rectangular and circular architectures are utilized. In comparison to the commonly used rectangular design, the circular architecture is capable of significantly improving the device-to-device uniformity without obvious deterioration in transistor performance, and the ratio of standard deviation to mean value (variation coefficient) is only 1.29% for threshold voltage (V_{TH}), 1.12% for maximum width-normalized transconductance ($G_{m,max}$), and 0.93% for linear electron mobility (μ_e), among the uniformity records for a-IGZO TFTs. Furthermore, simulations show a good agreement with experimental data and demonstrate that the improvement in device-to-device uniformity of circular architecture originates from the elimination of edge conduction paths compared to rectangular layout.**

***Index Terms*— Amorphous indium–gallium–zinc-oxide (a-IGZO), circular architecture, device uniformity, edge effect, thin-film transistor (TFT).**

I. Introduction

IN RECENT years, considerable attention has been paid to amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistors (TFTs) due to their intrinsic features, including high mobility, high ON/OFF current ratio, low OFF-state (leakage) current, low-temperature processing, and high transparency. Their potential applications include next-generation display drivers for active-matrix organic light-emitting diodes (AMOLEDs), advanced liquid crystal displays (LCDs), and other advanced LEDs, such as micro-LEDs and mini-LEDs [1], [2], [3], [4], [5]. However, there are still many challenges in further improving high-performance a-IGZO TFTs. For instance, more stable and uniform TFTs are required for the operation of gate-on-array circuits for large-area displays; introducing a negative word-line bias scheme is in high demand to offset the shift of cell transistor threshold voltage in a DRAM [6]. It must be emphasized that the device-to-device uniformity is one of the most important issues, because a small variation in threshold voltage (V_{TH}) could cause nonnegligible deterioration of resultant circuits [7]. As a result, much effort has been devoted to solve this problem. For instance, Jang's group proposed a dual-gate device structure, and the extra gate compared to the single-gate device contributed to the bulk accumulation/depletion, resulting in improved device-to-device uniformity [8]. Furthermore, Song's group fabricated ultrathin aluminum oxide as a gate dielectric using solution processing, which efficiently enhanced the dielectric capacitance and resulted in good uniformity of a-IGZO TFTs. Note that the rectangular architecture was generally used in these reports, where the edge of the active layer might have certain effects on the main conduction channel and subsequent transistor performance [9], [10].

In this work, the circular architecture (also known as Corbino structure [11], [12], [13]) is utilized for a-IGZO TFTs, and almost identical transistor performances, including ON/OFF ratio, linear electron mobility (μ_e), and maximum width-normalized transconductance ($G_{m,max}$), to rectangular ones are achievable. More importantly, this circular design significantly improves the device-to-device uniformity, and the ratio of standard deviation (σ) to mean (μ) value is as low as 1.29% for V_{TH}, 1.12% for $G_{m,max}$, and 0.93% for μ_e, respectively. Such excellent uniformity is among the records for a-IGZO TFTs, which is attributed to the elimination of edge conduction paths compared to the rectangular ones according to the TCAD simulations.

II. Experimental Details

A bottom-gate top-contact structure is utilized to fabricate a-IGZO TFTs. 30-nm Mo was deposited by magnetron

Manuscript received 8 January 2024; revised 16 June 2024; accepted 22 July 2024. Date of publication 5 August 2024; date of current version 23 August 2024. This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFA0706100 and in part by the National Natural Science Foundation of China under Grant 62074163 and Grant 62274178. The review of this article was arranged by Editor S.-M. Lee. *(Yanqin Zhang, Xufan Li, and Jianwei Zhang contributed equally to this work.) (Corresponding authors: Mengmeng Li; Lingfei Wang; Zhenzhong Yang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2024.3435179.

Digital Object Identifier 10.1109/TED.2024.3435179

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TABLE I
CHANNEL DETAILS OF IGZO TFTS

Architecture	Rectangular	Circular		
Sample label	R	D300	D600	D800
L (μm)	10	4/10/20	4/10/20	4/10/20
W (μm)	20	942	1884	2512

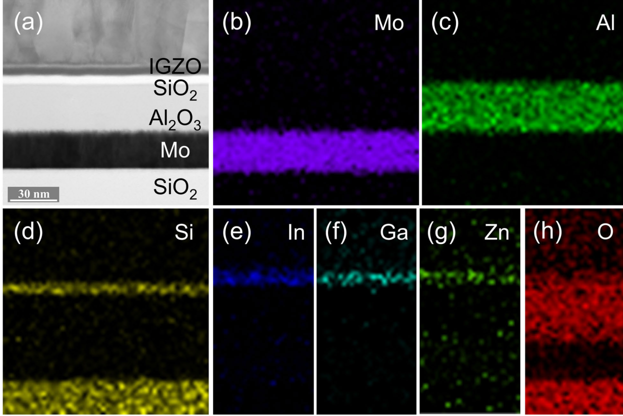

Fig. 1. (a) TEM image and (b)–(h) corresponding EDS mapping of a-IGZO TFT.

sputtering on the commercial SiO_2/Si wafer and then patterned as a gate electrode through conventional photolithography and dry etching. Then, 30-nm Al_2O_3 was deposited by atomic layer deposition (ALD) as a gate dielectric. Afterward, an ultrathin SiO_2 (5 nm) was first deposited as interfacial modification layer using magnetron sputtering, and then, the sequential deposition of 7-nm-thick a-IGZO thin film was conducted as the active layer in the same chamber. Source/drain (S/D) electrodes (5/30-nm Ti/Au) were deposited by electron beam evaporation and then patterned by photolithography. Finally, 30-nm-thick Al_2O_3 was deposited by low-temperature ALD (200 °C) for passivation. The details of channel length/width (L/W) are shown in Table I. The sample for transmission electron microscopy (TEM) was prepared through a FEI Helios G4 UX dual-beam focused ion beam (FIB)/scanning electron microscopy (SEM). Device characteristic simulations were conducted by Silvaco Technology Computer Aided Design (TCAD).

III. RESULTS

Fig. 1 exhibits the cross section TEM image and corresponding energy dispersive spectrometer (EDS) mapping of a-IGZO TFT. It is evident that each layer can be clearly distinguishable, especially for the ultrathin SiO_2 (modification) and a-IGZO (active) layers, in good agreement with the device fabrication mentioned above. Two different architectures (rectangular and circular layouts) are used for TFT fabrication, as shown in Fig. 2(a) and (d).

Ten rectangular devices on the same die are randomly selected and characterized in the linear regime with the drain voltage (V_{DS}) of 0.1 V, all of which exhibit typical linear/saturation and pinch-off behaviors, according to both transfer and output characteristics [Fig. 2(b) and (c)]. The gate leakage current is on the order of pA. However, distinguishable differences in V_{TH} are observed, indicating relatively poor device-to-device uniformity.

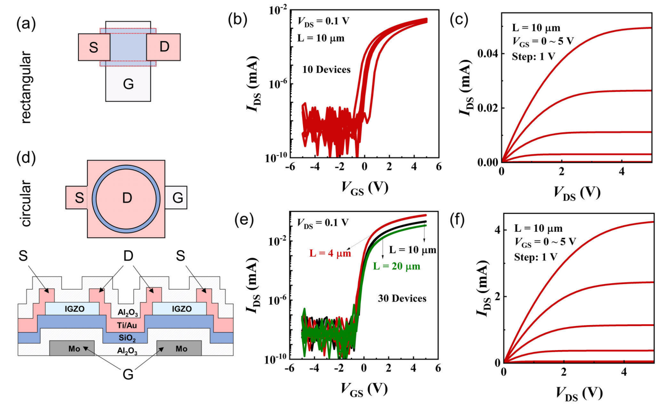

Fig. 2. (a) and (d) Schematic illustration, (b) and (e) transfer, and (c) and (f) output characteristics of a-IGZO TFTs with rectangular (top) and circular (bottom) gate architectures. In (b) and (e), $V_{DS} = 0.1$ V. The channel length for both architectures is 10 μm. The sample for (e) and (f) is D600.

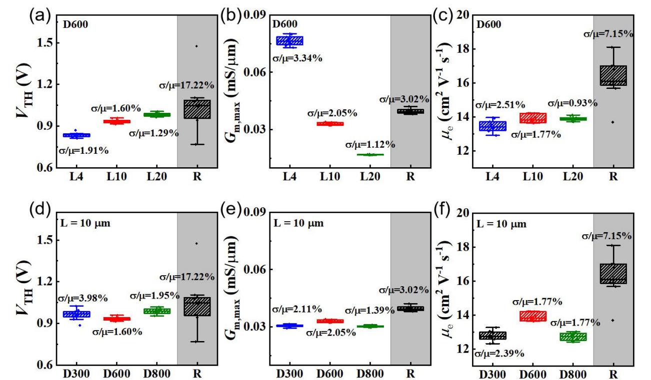

Fig. 3. (a)–(c) Device performances (V_{TH}, $G_{m,max}$, and μ_e) of a-IGZO TFTs as a function of (a)–(c) channel length and (d)–(f) channel width. In (a)–(c), $W = 1884$ μm for circular devices (D600). In (d)–(f), $L = 10$ μm for circular devices. The performance of rectangular devices is shown for comparison (gray frame). Each average value is obtained from ten randomly selected individual devices.

On the other hand, the circular a-IGZO TFTs fabricated using the same process are also investigated [Fig. 2(d)]. Compared to the prior reports on circular TFTs [11], [12], [13], we have not only patterned the semiconductor layer and gate electrode but also focused more on device-to-device uniformity. Almost identical OFF-state current and saturation drain voltage to the rectangular devices are obvious, as shown in Fig. 2(e) and (f). Note that three different channel lengths are used for this circular architecture (30 devices), and it is found that the ON-state current is noticeably enhanced with decreasing channel length. More importantly, such circular architecture results in much improved device-to-device uniformity.

In order to quantify the uniformity in a more precise way, the σ/μ value, which is also defined as variation coefficient, is utilized [14]. Fig. 3(a)–(c) summarizes the device performances of circular a-IGZO TFTs as a function of channel length, including V_{TH}, $G_{m,max}$, and μ_e. The σ/μ coefficient of V_{TH} for rectangular TFTs reaches 17.22%, in accordance with transfer characteristics shown in Fig. 2(b). In sharp contrast, the device uniformity is significantly improved using circular architecture, and σ/μ coefficient of V_{TH} is less than 2%, independent of channel length [Fig. 3(a)]. With decreasing

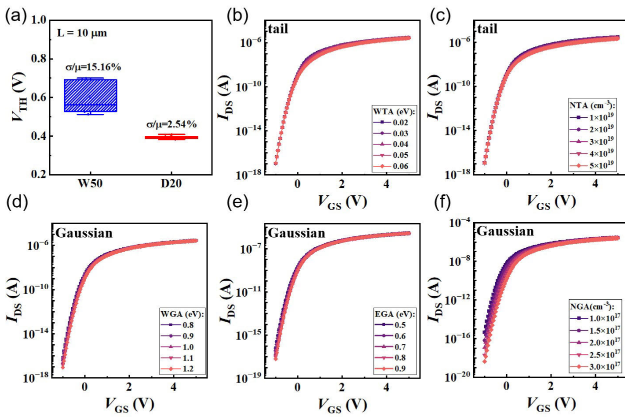

Fig. 4. (a) Experimental V_{TH} summary of rectangular (W50) and circular (D20) a-IGZO TFTs with similar W. (b)–(f) Influence of defects inside a-IGZO on the charge transport simulated by TCAD. (b) and (c) Acceptor-like tail state (WTA and NTA) and (d)–(f) acceptor-like Gaussian state.

TABLE II

SS COMPARISON OF REPRESENTATIVE TFTS

SS (mV/dec)	Rectangular	Circular	
	W20L10	D300L10	D600L4
μ (mV/dec)	170.03	133.15	149.45
σ (mV/dec)	34.06	19.19	23.06
σ/μ (%)	20.00	14.41	15.42

the channel length from 20 to 4 μm, σ/μ coefficient of $G_{\mathrm{m,max}}$ is slightly increased from 1.12% to 3.34%, but $G_{\mathrm{m,max}}$ is enhanced by more than four times [15] [Fig. 3(b)]. Furthermore, the extracted μ_{e} is almost independent of channel length, and the corresponding variation coefficient is much lower than that of rectangular device, further confirming the improved device uniformity due to the circular architecture. Note that the average μ_{e} of rectangular TFTs is slightly higher than that of circular ones, which can be attributed to the stronger electrical field from the rectangular architecture [16]. Herein, the best uniform devices are from the circular architecture with $L = 20$ μm and $W = 1884$ μm (D600), and the corresponding σ/μ coefficients are 1.29% for V_{TH}, 1.12% for $G_{\mathrm{m,max}}$, and 0.93% for μ_{e}, respectively, which are among the uniformity records [8], [14], [17], [18], [19], [20], [21] for a-IGZO TFTs to the best of our knowledge.

The circular a-IGZO TFTs with different channel widths are also investigated, as shown in Fig. 3(d)–(f). First, it is found that the channel width has negligible impact on the performance of circular a-IGZO TFTs. Second, all circular devices exhibit excellent uniformity, and most σ/μ coefficients of V_{TH}, $G_{\mathrm{m,max}}$, and μ_{e} are within 3%, superior to the rectangular ones. Additionally, two architectures with similar channel widths are also compared for device-to-device uniformity, as shown in Fig. 4(a). The circular TFTs with $W = 62.8$ μm (D20) exhibit the σ/μ coefficient of 2.54% for V_{TH}, which further proves: 1) the W-independent device performance of circular TFTs and 2) much better device-to-device uniformity than that of rectangular ones ($W = 50$ μm and $\sigma/\mu = 15.16$%). Additionally, the subthreshold swing (SS) and resultant σ/μ value are slightly improved for circular TFTs (Table II).

The distribution of defect states in amorphous semiconductors dominates carrier density profiles and transport

TABLE III

DETAILED DOS PARAMETERS IN TCAD SIMULATION

VARIABLES	NGA	NTA	WGA	WTA	EGA
	(cm^{-3})			(eV)	
WTA	2×10^{17}	2×10^{19}	1.15	Fig. 4(b)	0.8
NTA	2×10^{17}	Fig. 4(c)	1.15	0.039	0.8
WGA	2×10^{17}	2×10^{19}	Fig. 4(d)	0.039	0.8
EGA	2×10^{17}	2×10^{19}	1.15	0.039	Fig. 4(e)
NGA	Fig. 4(f)	2×10^{19}	1.15	0.039	0.8

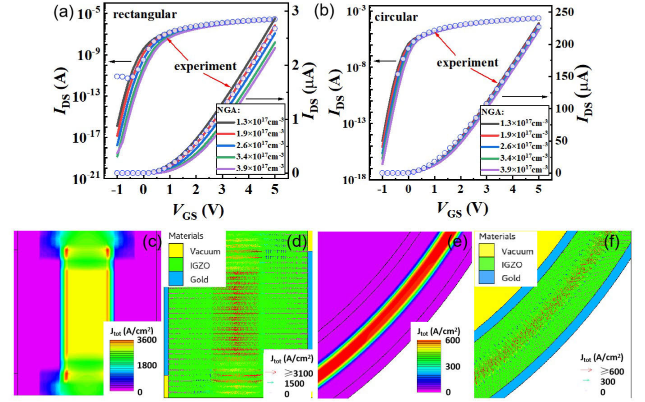

Fig. 5. Simulated transfer characteristics of (a) rectangular and (b) circular a-IGZO TFTs with various NGAs. The experimental data (circular symbols) are used for the calibration of TCAD simulation. (c) and (e) Simulated current density profiles and (d) and (f) enlarged current density profiles with vectors of a-IGZO TFTs. (c)–(f) Circular and rectangular devices, separately. The channel dimension is the same with samples R and D600 ($L = 10$ μm).

mechanisms and is regarded as a major variation source due to composition difference [22]. To explore the mechanisms of uniformity improvement in this circular architecture, TCAD simulations are carried out. Defects inside the semiconductor are equated into acceptor-like tail states, acceptor-like Gaussian states, donor-like tail states, and donor-like Gaussian states [23]. Due to the electron transporting properties of a-IGZO [24], [25], the acceptor-like states were often considered for modeling, where the main parameters include: 1) the trap density per unit energy at the semiconductor conduction band edge (NTA) and the characteristic decay energy (WTA) for the acceptor-like tail state and 2) the Gaussian distribution peak for acceptor-like states (EGA), the trap density per unit energy at the peak of the distribution (NGA), and the characteristic decay energy (WGA) for the acceptor-like Gaussian state [26]. It is evident from Fig. 4(b)–(f) and Table III that NGA in the acceptor-like Gaussian state plays the key role in modulating V_{TH} for amorphous channel TFTs. As a result, different NGA values are introduced into the TFTs with rectangular and circular architectures. The coupling of fringing electric field and contamination or local deformation induced highly doping issues contribute to highly conductive parasitic paths [23]. For circular structure, the elimination of fringing electric field mitigates the coupling effect induced parasitic paths. By altering NGA in the same range, Fig. 5(a) and (b) indicates that maximum V_{TH} shifts for the rectangular and circular structures are 0.7 and 0.2 V, respectively, which is consistent with the experimental results shown in Figs. 2 and 3. Note that the experimental data [circular symbols in Fig. 5(a) and (b)] are used for the calibration of TCAD simulations.

Fig. 5(c) and (d) shows the corresponding nonuniform distribution of current density in rectangular TFT along the width direction, and much higher current density is observed at the edge of the channel close to the corner of S/D electrodes. By contrast, much more uniform current density distribution is present for a circular structure, which might be attributed to the elimination of channel edge conduction paths perpendicular to S/D electrodes [Fig. 5(e) and (f)] [10]. It is one of the main factors induced severe self-heating issue for rectangle structure [27], [28], resulting from distinct current density distributions. Due to the presence of extra edge-current paths, electrical characteristic variations are much closely related to the difference of defect concentration near edges of a-IGZO channel along the width direction. Consequently, such a circular architecture featuring more uniform distribution of current density eliminates edge conduction paths and greatly improves the device-to-device uniformity. In addition, the initial uniformity is important in advanced application for IGZO-based capacitorless DRAM cells [6]. Due to eliminating the capacitor, the charge of the storage node is quite sensitive to the variations of storage transistor in the array [22]. Thus, the proposed fabrication recipe with superior initial uniformity shows great potential in future memory applications.

IV. Conclusion

In conclusion, the circular design is proposed for the fabrication of a-IGZO TFTs, which is capable of significantly improving the device-to-device uniformity in comparison to the widely used rectangular architecture. In particular, variation coefficient is as low as 1.29% for V_{TH}, 1.12% for $G_{\mathrm{m,max}}$, and 0.93% for μ_{e}, which are among the uniformity records for a-IGZO TFTs. Furthermore, the TCAD simulation demonstrates that the elimination of edge conduction paths by circular design is the main reason for such excellent device-to-device uniformity in comparison to the rectangular ones. These results provide new insights in further improving device performance of TFTs.

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