Extraction of the Thermal Resistance and the Thermal Capacitance of GaN Power HEMTs by Using Pulsed I–V Measurements

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***Abstract*— This work presents an extraction method for the thermal resistance and the thermal capacitance of GaN power high-electron mobility transistors (HEMTs). An electro-thermal analytic model is derived describing the current drain degradation in the linear region of the transistor, which is caused by self-heating. This model function is fit to pulsed *I–V* measurement data, and the fitting parameters provide the required thermal parameters. A parameter analyzer and a thermal chuck are used as setups to perform the measurements. A quasi-transient drain current response signal is composed of the measured data, which is used for parameter extraction. The new method is used to extract the thermal parameters of a 650 V class GaN power transistor. The transistor features an integrated temperature sensor. This allows a cross-validation of the results, which are obtained by the new method, with the results which are measured by the temperature sensor. The new extraction method can be easily performed with typical equipment, that is commonly available in labs for electrical characterization of GaN power transistors.**

***Index Terms*— Channel temperature, electro-thermal model, high-electron mobility transistor (HEMT), junction temperature, linear region, pulsed measurement, self-heating, thermal impedance.**

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I. Introduction

THERMAL resistance and thermal capacitance are important device parameters required to estimate the junction temperature of power transistors. The knowledge of these parameters is crucial for designing efficient and reliable power electronics. Many methods to extract-thermal parameters have been described in the literature [1].

This work presents a practice-oriented method to determine the thermal impedance using pulsed measurement data by conventional, commercial parameter analyzer in combination with a defined heat sink temperature enabled by a heat plate or a thermal wafer chuck. Thus, this method can be easily integrated into automated electrical parameter characterization of power transistors without changing the measuring equipment for the extraction of thermal parameters.

In contrast to that, traditional thermal characterization methods [1], such as infra-red thermography [2], [3], Raman thermography [4], or small-signal thermal impedance measurements [5], [6], require often expensive, or self-developed equipment and setups, and need a high degree of expertise. Furthermore, in rare cases, there are special devices developed for the thermal characterization of technology, featuring an ON-chip sensor to measure the junction temperature [7], [8], [9]. However, these special devices are usually not available and each device must be calibrated before measurement.

II. Thermal Characterization Based on Self Heating

Further methods are based on the electro-thermal drain current I_D degradation in the saturation region as a function of a drain–source voltage V_{DS}, which is caused by self-heating [10], [11], [12], [13], [14].

In contrast to that, the method in this work investigates the drain current degradation in the linear region of the output characteristics. The total ON-state resistance R_{ON} of a transistor is composed of various contributions: the drift resistance along the active channel, especially the resistance in the gate region, the contact resistance of the ohmic contacts, and the resistance of the drain and source metallization. In the linear region, the temperature distribution along the

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drift path is almost uniform, as can be observed in TCAD simulations [15]. This is in contrast to device operation in the saturation region, where partial depletion already takes place close to the gate edge on the drain side, resulting in an inhomogeneous heat distribution along the drift length. This leads to a local accumulation of heat and thus to an increase in the thermal resistance. If a power electronic application (e.g., voltage converter and inverter) is optimized for high efficiency the conduction losses of the transistors are usually dominant. These losses are caused by the ON-state resistance and are present in the linear range of the transistor. Therefore, the presented characterization method is particularly suitable for these efficient power applications.

A. Isothermal Assumption

The basic idea of most electro-thermal extraction methods is the assumption, that the junction temperature T_J is equal to the case temperature $T_J \approx T_C$, if no self-heating is appeared. This can be assumed for operation points around zero with very low power $P_{DS} \approx 0$, or for very short time samples after turn-on with higher power $P_{DS}(t \approx 0)$. Under these assumptions, the short-pulsed drain current responses are measured using different case temperatures $I_D(t \approx 0,\ T_J \approx T_C)$. The measurement can be used as a lookup table. In comparison to long pulsewidth drain current responses $I_D(t_{PW},\ T_J \neq T_C)$, the lookup table is used to estimate the junction temperature $T_J(I_D,\ V_{DS},\ T_C)$. Furthermore, the thermal resistance can then be calculated by $R_{TH} = (T_J - T_C)/(I_D{\cdot}V_{DS})$. However, only with ultra-short pulse measurements in sub microsecond range the assumption of the isothermal assumption is adequate, and requires advanced pulse measurement equipment [10], [11], [12], [13], [14], whereas commercial parameter analyzers have minimum pulsewidth in the range of 50–100 μs. Self-heating arises directly after turn-on in particular in the saturation region as shown in [16]. Early drain current degradation falsifies the estimation of the junction temperature. The method in this work takes this error into account.

B. New Approach: Model-Based Extraction of the Thermal Parameters in the Linear Region of the I–V Curve

The extraction method in this work is based on a simple analytic electro-thermal model [see Fig. 1(a)] and uses pulsed drain current versus drain–source voltage (I–V) curves generated by typical commercial power devices parameter analyzer. In the following, we deduce the analytic model of electro-thermal current degradation of power transistors in the linear region of the output characteristics, and then we will demonstrate the method using measurement data, and verify the method by comparing the data with the results extracted by an ON-chip temperature sensor.

III. Derivation of the Electro-Thermal Model

Self-heating in a transistor refers to the phenomenon where the transistor's power dissipation P leads to an increase in its junction temperature T_J by the thermal impedance Z_{TH}. As a result of the increased temperature electron mobility

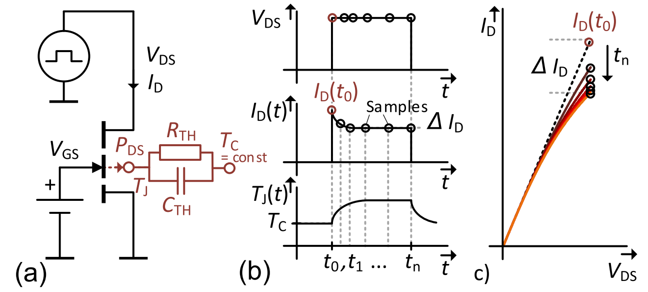

Fig. 1. Electro-thermal behavior of pulsed power transistors. (a) Electro-thermal circuit diagram. (b) Transient pulse responds to drain current and junction temperature. (c) Drain current degradation in the linear region of the output characteristic caused by self-heating.

μ decreases, and therefore, the ON-state resistance R_{ON} of the transistor increases, leading to a degradation in the drain current I_D [see Fig. 1(b)]. In the following consideration, we focus on this effect in the linear region of the transistor [see Fig. 1(c)]. Thus, we assume, that the device operates fully in the ON-state and the gate region channel is un-depleted. Under these conditions, it is possible to derive a simple electro-thermal model. The transient power dissipation and the drain current degradation is given by the following equations:

$$P_{DS}(t) = V_{DS} \cdot I_D(t), \quad \text{with} \tag{1}$$

$$I_D(t) = \frac{V_{DS}}{R_{ON}(T_J(t))}. \tag{2}$$

Furthermore, a linearized thermal dependence of the ON-state resistance is assumed, which is suitable in small discrete thermal steps of about a few to tens Kelvin. The ON-state resistance is given by the following equations:

$$R_{ON}(T_J(t)) = k_{TH}(T_J(t) - T_J(t=0)) + R_{ON,0}, \quad \text{with} \tag{3}$$

$$k_{TH} = \frac{\Delta R_{ON,0}}{\Delta T_C} \tag{4}$$

whereas k_{TH} denotes the thermal increase constant of the ON-state resistance, and $R_{ON,0}$ is the initial ON-state resistance without self-heating, valid under the following condition:

$$R_{ON,0} = R_{ON} \text{ at } (t = 0) \text{ and } (T_J = T_C). \tag{5}$$

Two types of thermal models are commonly used for the thermal modeling of line transistors and power modules: the Cauer and the Foster model [17], [18], [19], which can be mathematically calculated into each other [20]. With higher order models, the thermal behavior of complex layer stacks can be fit with a high degree of accuracy. Such a model could be used in the following analytical solution, but this would lead to unwieldy formulae and is therefore not investigated in this article. For a more convenient solution, we use a first-order thermal low pass [10], [17], which is equal to a one-cell Cauer model and equal to a one-cell Forster model. Thus, the first-order low-pass model of the thermal impedance is given by the following equation:

$$Z_{TH}(t) = \frac{T_J(t) - T_C}{P_{DS}(t)} = R_{TH}\left(1 - \mathbf{e}^{\frac{-t}{\tau_{TH}}}\right) \tag{6}$$

and by using the thermal time constant

$$\tau_{TH} = R_{TH} \cdot C_{TH}. \tag{7}$$

R_{TH} denotes the thermal resistance and C_{TH} denotes the thermal capacitance. It should be clarified here that this thermal capacitance corresponds to the first-order low-pass thermal model. This capacitance is not equal to the thermal capacitance of the substrate material (e.g., carrier or epitaxial layers), thus specific heat capacity c of a material cannot be directly extracted.

The transient drain current as pulse or rather drain–source voltage step responds can be calculated by combining (1)–(7), and is given by the following equation:

$$I_D(t) = \frac{A \cdot \mathbf{e}^{\frac{t}{\tau_{TH}}} - \mathbf{e}^{\frac{t}{2\cdot\tau_{TH}}}\sqrt{\mathbf{e}^{\frac{t}{\tau_{TH}}}(A^2+1)-1}}{\sqrt{k_{TH}\cdot R_{TH}}\left(1-\mathbf{e}^{\frac{t}{\tau_{TH}}}\right)} \tag{8}$$

and with expression

$$A = \left(2\frac{V_{DS}}{R_{ON,0}}\sqrt{k_{TH}\cdot R_{TH}}\right)^{-1}. \tag{9}$$

The junction temperature is calculated by combining (1) and (6), and given by the following equation:

$$T_J(t) = R_{TH}\left(1-\mathbf{e}^{\frac{-t}{\tau_{TH}}}\right)V_{DS}\cdot I_D(t) + T_C. \tag{10}$$

IV. Extraction of the Thermal Resistance and Thermal Capacitance Using Measurement Data

The transient drain current function (8) can be fit to measurement data. The fit parameters are $R_{ON,0}$, k_{TH}, R_{TH}, and C_{TH}. These parameters can be estimated by using the time-discrete, measured dataset of

$$t_{(i)} = \{t_{(1)}, t_{(2)}, t_{(3)}, \ldots, t_{(n)}\}, \quad \text{and} \tag{11}$$

$$I_{D(i)} = \{I_{D(1)}, I_{D(2)}, I_{D(3)}, \ldots, I_{D(n)}\}. \tag{12}$$

Ideally, the drain current data should be available in logarithmic time intervals, and extend over a wide range from hundreds of microseconds to seconds. The currents toward zero and infinity are estimated as follows:

$$dI_D/dt(t\to 0) \approx \frac{I_{D(2)} - I_{D(1)}}{t_{(2)} - t_{(1)}} \tag{13}$$

$$I_D(t\to 0) \approx I_{D(1)} - dI_D/dt(t\to 0)\cdot t_{(1)} \tag{14}$$

$$I_D(t\to\infty) \approx I_{D(n)}. \tag{15}$$

An estimation of the fit parameters can be made using the following formulas derived from (8) and given by the following equations:

$$R_{ON,0} = R_{ON,0@Tc}(t\to 0) = \frac{V_{DS}}{I_D(t\to 0)} \tag{16}$$

$$k_{TH} = \frac{\Delta R_{ON,0}}{\Delta T_C} = \frac{R_{ON,0@Tc(i+1)} - R_{ON,0@Tc(i)}}{T_{C(i+1)} - T_{C(i)}} \tag{17}$$

$$C_{TH} = -\frac{I_D(t\to 0)\cdot k_{TH}\cdot V_{DS}^2}{R_{ON,0}^2\cdot dI_D/dt(t\to 0)} \tag{18}$$

$$R_{TH} = \frac{\tau_{TH}}{C_{TH}} = \frac{-I_D(t\to 0) + I_D(t\to\infty)}{dI_D/dt(t\to 0)}\frac{1}{C_{TH}}. \tag{19}$$

Further optimization of the fit function to the measured data and could be done via numerical optimization algorithms. However, estimation using the limit value (13)–(19) is usually sufficient and needs no further optimization.

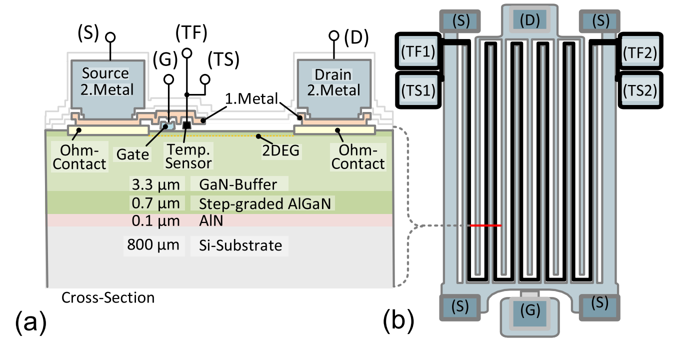

Fig. 2. Device under test: 650 V class GaN-on-Si HEMT with integrated temperature sensor, which is used the verify the proposed method. (a) Cross section of the intrinsic HEMT structure. (b) Chip layout of the interdigital finger structure with a gate width of 10 mm.

V. Experiment Results and Method Verification

A. Device-Under-Test and Measurement Setup

In the following, the proposed extraction method by using pulsed I–V curves is applied to a GaN-on-Si high-electron-mobility transistor (HEMT) and verified against the measurement results of an ON-chip temperature sensor. The cross section and the top view layout of the GaN-on-Si HEMT is illustrated in Fig. 2. The 650 V class HEMT has dimensions of $L_{GD}/L_G/L_{GS} = 15/1/2$ μm. The sheet resistance of the 2-D electron gas was measured to be $R_{SH} = 680$ $\Omega\square$, the ohmic contact resistance is $R_{OHM} = 186$ mΩ·mm, the specific ON-state resistance is $R'_{ON} = 15.1$ Ω·mm, and the sheet resistance of the finger and pad metallization is around $R_{SH,MET} = 0.002$ $\Omega\square$. The comb structure has a total gate width of $W = 10 \times 1$ mm $= 10$ mm and an active area of $A = 290 \times 1000$ μm^2 including the area of ohmic contacts. The device has a depletion-mode isolated gate, with a highly negative threshold voltage of $V_{TH} = -10.6$ V. The gate–source voltage was set to zero $V_{GS} = 0$ V for all performed measurements in this work. Under this condition, the device is fully in the ON-state. The device has a step-graded GaN epitaxie with thicknesses as shown in Fig. 2(a) on a 4 in Si (111) wafer with a thickness of 800 μm. The structure features a integrated temperature resistor, which is placed as a metal meander close to the gate. The structure has already been studied in detail and was published in [8]. For data acquisition, we use a power device analyzer (Agilent B1500a) in pulsed I–V mode. The pulse sequence with increasing pulse widths t_{PW} is shown in Fig. 3(a). It is crucial that only single pulses with subsequent delay time (>10 s) are ever measured. This ensures that the junction temperature T_J drops to the value of the chuck temperature T_C and is not influenced by the previous self-heating. A quasi-transient signal is assembled from these pulse measurements. To compare the measured values with the appropriate model function, pulse widths in logarithmic times are advantageous, starting with the shortest possible pulsewidth up to the longest possible pulsewidth, as shown in Fig. 4. The power device analyzer (Agilent B1500a) is available with different SMUs. In this work, we measured the device with two different SMUs for comparison and verification of the measurements, with the high power SMU (HPSMU) and with the high current SMU (HCSMU). The measurements

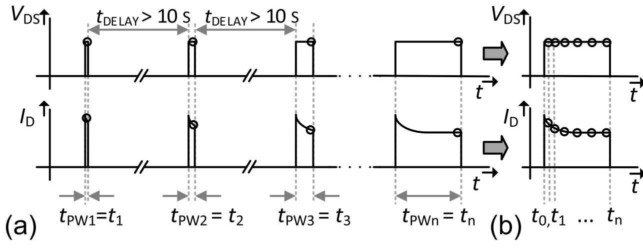

Fig. 3. (a) Pulse sequence measured with pulsed I–V-parameter analyzers. (b) Quasi-transient time signal calculated by the pulse measurements (a).

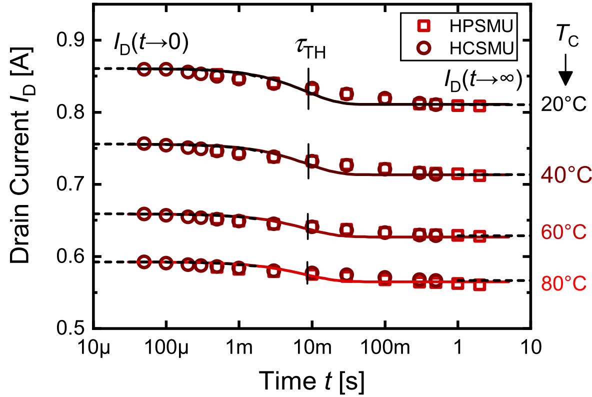

Fig. 4. Drain current pulse responds (current degradation) as a function of the time for different chuck temperatures. The pulse voltage is V_{DS} = 1.3 V. The analytic model function (8), (9) is fit to the measurement data to extract the thermal impedance. The device under test is shown in Fig. 2.

were performed at four different chuck temperatures T_C from 20 °C to 80 °C in 20 °C steps (see Fig. 4). The pulse voltage was set to V_{DS} = 1.3 V, which result in drain current response values below 1 A, which is the maximal current compliance for the used continuous mode of the SMUs.

B. Fit of the Electro Thermal Model Function to the Measured Data and Extraction the Thermal Parameters

The quasi-transient drain current values are shown in Fig. 4. Superimposed are the fit curves of the function from (8). The curve fitting and the determination of the required fitting parameters were estimated with the help of chapter I–V in particular (16)–(19). The thermal time constant τ_{TH} is marked as the point of inflection (in Fig. 4), in case the x-axis is logarithmically scaled. A comparison of the measured values and the fit curves shows good overall agreement. However, the fit curve does not well describe the slope of the thermal behavior around the inflection point. The reason for this is the simple first-order thermal model in (6). A higher order (e.g., third order) thermal model would allow a better fit, but it leads to an extensive model equation and correspondingly more fit parameters, which is not investigated in this work.

Equations (18) and (19) were used to determine the thermal resistance and the thermal capacity for different temperatures T_C. The thermal resistance is about $R_{TH,20\,^\circ C}$ = 12 K/W at a chuch temperature of T_C = 20 °C an it is continuously increasing to $R_{TH,80\,^\circ C}$ = 17 K/W at T_C = 80 °C. We assume that the increase in thermal resistance is caused by the unthinned, highly conductive Si substrate (thickness t_{Si} = 800 μm, resistivity R_O = 0.001–0.005 Ω·cm). The corresponding temperature behavior of highly conductive Si substrates is described in [21], and thus an increase in thermal resistance is to be expected. The thermal capacitance is decreasing from 0.8 to 0.5 m·Ws/K within the same temperature range. We do not have a physical explanation for the drop in thermal capacitance.

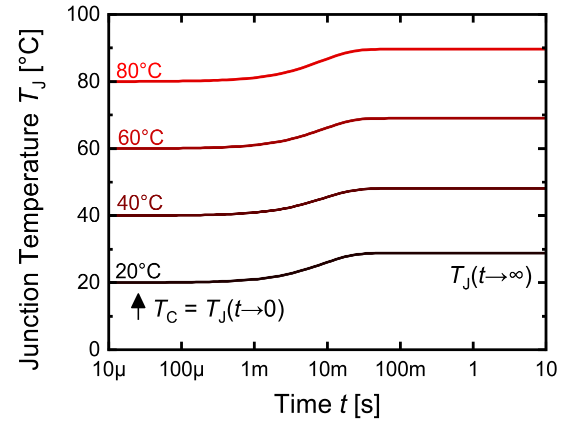

Fig. 5. Junction temperature as a function of the time for different chuck temperatures calculated by model function (9) and thermal impedance extracted by the fit in Fig. 3.

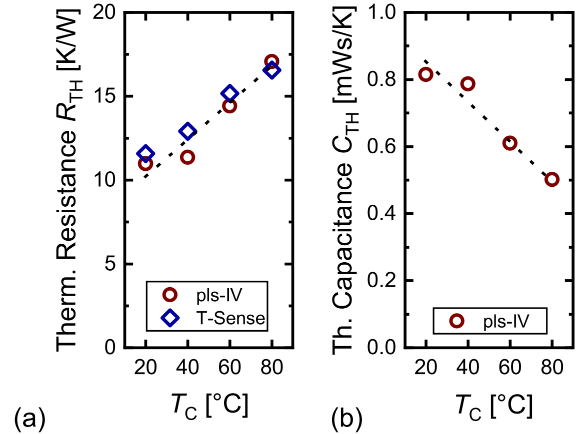

Fig. 6. (a) Extracted thermal resistance as a function of the chuck temperature (red points). The thermal resistance values are compared with the values of the ON-chip temperature sensor (blue diamond-shaped points). (b) Extracted thermal capacitance.

In combination with the remaining extracted fit parameters k_{TH} and $R_{ON,0}$, the junction temperatures T_J can be determined using (10) and are shown in Fig. 5. The extracted values of the thermal resistance and the thermal capacitance as a function of the chuck temperature is plotted in red points in Fig. 6. These resuls are compared in the following by the measurement resuls of the ON-chip temperature sensor, plotted with diamond-shaped marker symbols.

VI. Verification of the Results by the Values of an On-Chip Temperature Sensor

For cross-validation, the thermal resistance is extracted by using the data of an ON-chip temperature sensor, which is integrated into the HEMT [8]. The ON-chip sensor is placed as a metal meander (resistance temperature detector = RTD) close to the gate, as illustrated in Fig. 2. The thermal resistance measured by the ON-chip temperature sensor is also plotted in

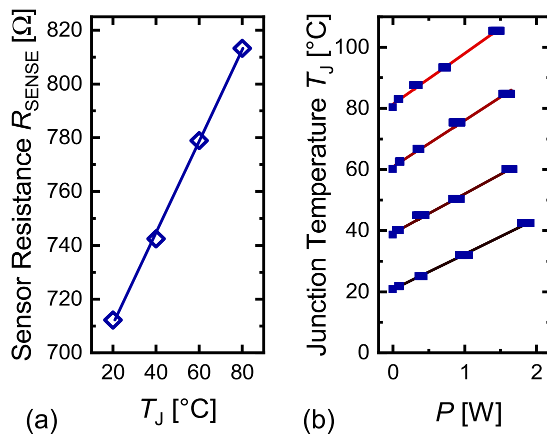

Fig. 7. Characterization data and calibration measurement of the temperature sensor. (a) Sensor resistance as function of temperature. (b) ON-chip temperature as function of the dissipated power in the device-under-test.

Fig. 6(a) and compared with the values found by the proposed extraction method.

Here, it is assumed that the chuck temperature T_C is equal to the ON-chip temperature T_{SENSE} and equal to the junction temperature T_J of the device, in case no power is dissipated by the transistor. The measurement shows that the resistance of the ON-chip metal meander (= temperature sensor) R_{SENSE} is proportional to the temperature $T_C = T_J$, at $P_{DS} = 0$, as shown in Fig. 7(a). Thus, this linear function $R_{SENSE}(T_J)$ is used for calibrating the sensor data. Fig. 7(b) shows the temperature data as a function of the dissipated power in the device, which is linear as well, and measured for different chuck temperatures. The gradients of these curves $T_J(P_{DS})$ are calculated in the thermal resistance values, which are also plotted in Fig. 6(a) with circle-shaped marker symbols.

VII. Conclusion

A commercially available parameter analyzer, pulsed source measurement units, a heat plate, or a wafer prober with a thermal chuck is sufficient for the thermal parameter extraction method, which is presented in this article. The drain current degradation is measured on the transistor-under-test and a model function is fit to the measured data. The fitting parameters correspond to the thermal resistance and the thermal capacitance, which can be easily determined using limit value equations presented in this work.

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