Modeling Gate Leakage Current for p-GaN Gate HEMTs With Engineered Doping Profile

Mojtaba Alaei, Matteo Borga, Elena Fabris, Stefaan Decoutere, Johan Lauwaert, and Benoit Bakeroot

***Abstract*— The forward bias gate leakage current and forward gate breakdown voltage are important properties of p-GaN gate high-electron-mobility transistors (HEMTs). An engineered doping profile in the p-GaN layer results in a higher gate breakdown voltage and a lower forward bias gate leakage current. The use of such a technique puts additional requirements on the compact models that are used for these p-GaN gate HEMTs. An accurate compact model is needed, which considers a change in the doping profile in the p-GaN layer of these devices. This article reviews the relationship between the gate bias and the voltage drops at the different junctions in the gate structure (i.e., at the metal/p-GaN Schottky junction and the p-GaN/AlGaN/GaN junctions) considering an engineered doping profile. This relationship is then used to model the drain–source current (I_{DS}) and gate leakage current (I_G). Three different regimes in the gate current have been considered in the model: Poole–Frenkel (PF) under low bias, thermionic emission (TE) in the medium bias range, and thermally assisted tunneling (TAT) at higher bias.**

***Index Terms*— Breakdown voltage, engineered gradient p-GaN doping, forward bias gate leakage current, gate leakage, junction voltage, p-GaN gate high-electron-mobility transistors (HEMTs), uniform p-GaN doping.**

I. Introduction

GAN-BASED high-electron-mobility transistors (HEMTs) have demonstrated remarkable potential in high-frequency and high-power applications [1], [2], [3]. Particularly, AlGaN/GaN HEMTs with a p-GaN gate structure are attractive due to the possibility of achieving enhancement-mode (E-mode) operation [4]. Yet p-GaN gate HEMTs are not without challenges. They suffer from a relatively high forward bias gate leakage current, which can result in a reduction of their overall efficiency. In the structure of the p-GaN gate HEMT, the layer arrangement resembles that of two back-to-back diodes. A meticulous analysis of these diodes facilitates the development of a comprehensive model, enabling a detailed examination and understanding of the underlying mechanisms governing gate leakage currents. While several studies have previously explored the gate leakage current mechanism in p-GaN gate HEMTs [4], [5], [6], [7], [8], [9], there exists a significant gap in the literature regarding the development of a compact model to encapsulate these mechanisms. The existing research, although insightful, has not yet presented a comprehensive model that begins with a fundamental analysis.

Recently, imec introduced a novel method to enhance p-GaN HEMTs' performance by adjusting the p-GaN doping profile, termed engineered p-GaN doping profile [10]. This enhancement notably improves forward gate breakdown voltage and reduces forward bias gate leakage current, boosting device reliability and efficiency. Expanding on previous advancements, this article endeavors to perform a physics-based analysis to model the influence of an engineered p-GaN doping profile on critical parameters, notably the junction voltage (ΔV_j) across the Schottky diode and the gate leakage current. Our objective is to comprehensively understand and model the mechanisms responsible for the observed improvements.

Consequently, in this study, we employ the developed model to analyze thoroughly and explore the implications stemming from the application of the engineered p-GaN doping profile. The structure of this article is given as follows. Section II describes the structure of the device under study and the engineered p-GaN doping technique. Section III draws the band diagram analysis and voltage distribution model up to breakdown voltage. Section IV presents the drain–source current (I_{DS}) model, which encompasses the validation of the model considering the access regions and temperature dependence induced by self-heating. Section V focuses on modeling the reverse and forward bias gate leakage currents, specifically investigating the influence of a lower doped p-GaN layer in the gate structure toward the Schottky metal. The proposed compact model is validated against measurements on imec's p-GaN gate HEMTs with an engineered p-GaN doping profile [10].

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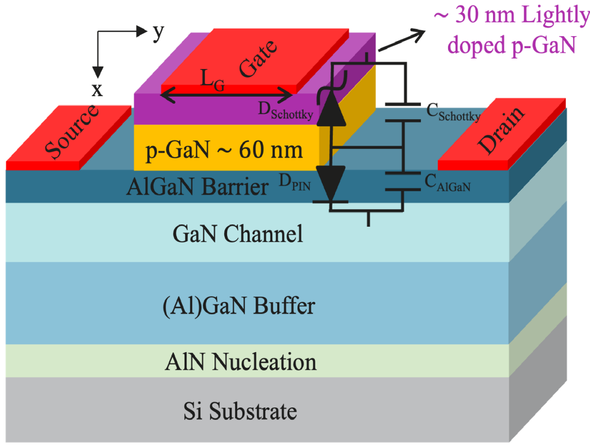

Fig. 1. Three-dimensional schematic view of a p-GaN gate HEMT with a lowly doped p-GaN region.

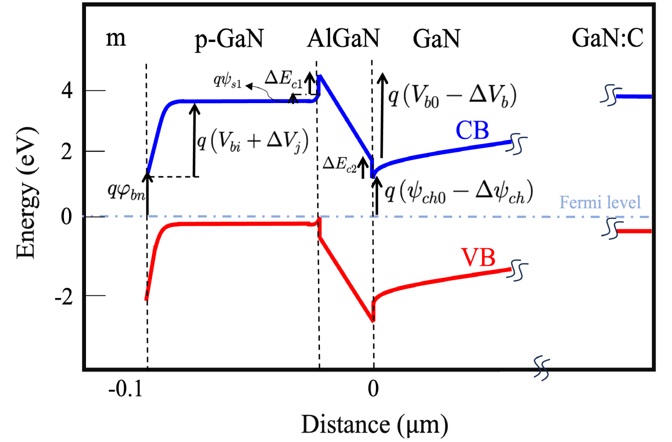

Fig. 2. Energy band diagram of p-GaN gate HEMT for $0 < V_{GS} < V_{TH}$.

II. Device Structure and Engineered p-GaN Doping Technique

The cross section of the AlGaN/GaN HEMTs with a p-GaN gate layer is shown in Fig. 1. An 8-in silicon substrate was used to grow the epitaxial stack using metal-organic chemical vapor deposition (MOCVD). The epitaxial layer comprises an AlN nucleation layer, an AlGaN stress-relief stack, a 300-nm undoped GaN layer forming the channel, a 14-nm AlGaN barrier containing 21.5% aluminum, and a 90-nm p-GaN cap layer doped with Mg. The p-GaN layer consists of two regions: first, a lowly doped GaN layer closer to the Schottky metal: a 30-nm p-GaN layer counter doped with Si ($\sim 0.75 \times 10^{19}$ cm^{-3}), yielding a net p-type active doping of $\sim 5 \times 10^{18}$ cm^{-3}; second, a highly doped p-GaN layer (60-nm Mg doped with $\sim 2.25 \times 10^{19}$ cm^{-3} electrically active Mg). Following TiN gate metal deposition, gate-stack patterning, and passivation ($Al_2O_3 + SiO_2$), a thermal treatment improved gate robustness (gate breakdown voltage $V_{BR} >$ 14 V) and reduced gate leakage current by tenfold, likely due to Schottky junction modifications. This treatment also decreased 2-D electron gas (2DEG) sheet resistance and enhanced device ON-resistance [10]. The arrangement of these layers (metal/pGaN/AlGaN/GaN) results in the formation of two back-to-back diodes: a Schottky metal/p-GaN diode and a p-GaN/AlGaN/GaN "p-i-n" diode. This study presents a comparative analysis between a device featuring the engineered p-GaN doping profile and a device with uniform doping of the p-GaN layer (equal to the highly doped layer in the engineered one). The same layout was used for both device types.

III. Voltage Distribution Analysis in p-GaN HEMT Layers Up To Breakdown

Referring to the energy band diagram depicted in Fig. 2, it can be deduced that the applied gate-to-source voltage (V_{GS}) is distributed among the variation of the junction voltage (ΔV_j), AlGaN barrier voltage (ΔV_b), and energy gap ($\Delta\psi_{ch}$), respectively, in the following manner [5]:

$$V_{GS} = \Delta V_j + \Delta V_b + \Delta\psi_{ch}. \quad (1)$$

The parameter $\Delta\psi_{ch}$ defines the separation between the conduction band energy and the Fermi level at the interface of the AlGaN/GaN channel such that $\Delta\psi_{ch} = E_f + V_{TH}$, where V_{TH} represents the threshold voltage and E_f is the variation of the Fermi level. An accurate self-consistent solution derived from the Poisson-Schrödinger equation is imperative for modeling and determining the Fermi level accurately.

Utilizing the relationships for ΔV_j and ΔV_b [11]

$$\Delta V_b = \frac{q n_{2DEG}}{C_b} \quad (2)$$

$$\Delta V_j = V_{bi}\left(\sqrt[\frac{1}{1-m}]{1 + (q n_{2DEG}) \times \sqrt{\frac{2(1-m)^2}{q N_A \epsilon_{GaN} V_{bi}}}} - 1\right) \quad (3)$$

where C_b is the capacitance of the AlGaN barrier ($C_b = (\epsilon_b/t_b)$), N_A denotes the doping level in the p-GaN, ϵ_{GaN} is the permittivity of GaN, m represents a dimensionless nonideality factor typically varying between 0 and 1, and V_{bi} denotes the built-in voltage.

It is essential to model the 2DEG density (n_{2DEG}) across the entire range of gate-to-source voltage (V_{GS}) up to the forward gate breakdown voltage in order to accurately predict the variation of junction voltage (ΔV_j) and variation of AlGaN barrier voltage (ΔV_b). This model allows the extraction of both ΔV_j and ΔV_b, and the results show that the gate bias division in (1) exhibits three regimes. We summarize the results here shortly. First, for V_{GS} values below the threshold voltage (V_{TH}), the applied voltage is mainly consumed to lower the energy gap $\Delta\psi_{ch}$ (the change in ΔV_j and ΔV_b is approximately zero). Second, when V_{GS} surpasses V_{TH}, the voltage distribution occurs between ΔV_j and ΔV_b as defined by (2) and (3). Third, for $V_{GS} > V_{sat}$ (V_{sat} set at 8 V in our paper), the AlGaN voltage saturates, and the additional portion of V_{GS} will be dropped at ΔV_j. This saturation occurs due to the phenomenon wherein the energy Fermi level is very close to or exceeds the conduction band offset between the GaN channel (and the p-GaN on the other side) and the AlGaN barrier ΔE_{c2}. This phenomenon facilitates the thermionic emission (TE) of electrons from the 2DEG into the AlGaN region and holes from the 2-D hole gas (2DHG) toward the AlGaN barrier, after which the carriers recombine in order to uphold charge

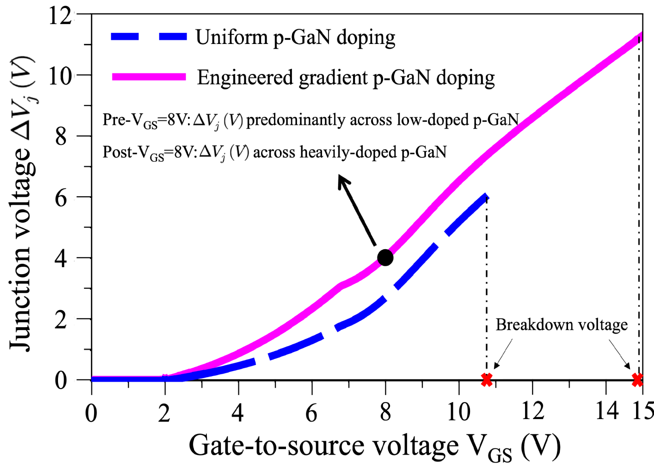

Fig. 3. Variation of the junction voltage (ΔV_j) concerning the gate-to-source voltage (V_{GS}) is depicted both in engineered gradient p-GaN doping and uniform p-GaN doping.

TABLE I
PHYSICAL PARAMETERS UTILIZED IN THE MODEL DERIVATIONS FOR THE P-GAN/ALGAN/GAN HEMT

Parameter	Symbol	Value
AlGaN mole fraction	x	0.215
AlGaN permitivity	ϵ_b	$8.9 - 0.4x$
AlGaN thickness	t_b	14 nm
GaN permitivity	ϵ_{GaN}	8.9
Non-ideality factor	m	0.6
Boltzman constant	k_B	8.6173×10^{-5} eV.K^{-1}
Effective density of satate of GaN	N_C	3×10^{18} cm^{-3}

equilibrium between 2DEG and 2DHG ($\delta n_{\text{2DEG}} = \delta n_{\text{2DHG}}$) [12]. This results in the saturation of both the energy barrier height in the AlGaN barrier and the 2DEG and the 2DHG charge densities. To accurately represent the saturation of the 2DEG charge, it is essential to model the number of electrons emitted throughout the AlGaN layer (referred to as n_{AlGaN}) and subsequently recombined with the 2DHG and then subtract this quantity from the 2DEG charge. n_{AlGaN} can be modeled by using the prevalent estimation approach of the Fermi–Dirac integral in degenerate semiconductors, as detailed in [13], and integrating over the AlGaN layer, the number of electrons for AlGaN charge (n_{AlGaN}) can be derived, as elucidated in [14]. By modeling the 2DEG charge for the entire range of V_{GS}, the junction voltage (ΔV_j) can be easily extracted using (3). Fig. 3 (depicted by the blue dashed line) illustrates the relationship between junction voltage (ΔV_j) and V_{GS} for the device featuring a uniform p-GaN doping profile. In this representation, ΔV_j has been modeled up to the breakdown voltage ($\sim$10.9 V).

Equation (3) shows that a decrease in the p-GaN doping results in an increase of ΔV_j (the depletion width W_d also increases). Consequently, the decrease in the electric field at the junction between the gate metal and the p-GaN results in a higher gate forward breakdown voltage and a reduction of the forward bias gate leakage current.

In this article, our focus centers on examining the reduction of the forward bias gate leakage current in the devices employing the engineered doping profile. Note that the reduction of p-GaN doping in the entire p-GaN layer yields threshold voltage instability. An effective approach to simultaneously achieve lower gate leakage current and enhanced breakdown voltage without altering the threshold voltage is through the utilization of an engineered gradient p-GaN doping technique, hence the necessity to split the p-GaN cap layer in a lowly doped (top) and a highly doped part (bottom). Since this top layer is shallow ($\sim$30 nm), we assume that the lowly doped p-GaN region becomes entirely depleted once ΔV_b reaches saturation (at $V_{\text{GS}} = V_{\text{sat}}$, set at 8 V in our paper). The depletion width (W_d) can be determined using the formula $W_d = (2\epsilon_{\text{GaN0}}(V_{\text{bi}} + \Delta V_j))/qN_A)^{1/2}$. This suggests that assuming complete depletion of the lowly doped layer at V_{sat} is a reasonable assumption. Upon full depletion of the lowly doped p-GaN region, any additionally applied V_{GS} is dropping in the higher Mg-doped region, with an approximate doping concentration of 2.25×10^{19} cm^{-3}. Consequently, ΔV_j in the engineered p-GaN doping device is divided into two distinct regions: For gate-to-source voltages $V_{\text{GS}} \leqslant V_{\text{sat}}$, ΔV_j is determined utilizing (3) as stipulated earlier. Subsequently, for $V_{\text{GS}} > V_{\text{sat}}$, ΔV_j is comprised of the value obtained at V_{sat} plus the additional ΔV_j drop in the uniformly doped p-GaN layer. The inclusion of a lowly doped region in the engineered p-GaN doping device results in a substantial increase in ΔV_j, as depicted in Fig. 3. Table I lists the physical parameters utilized in the analysis and modeling of the p-GaN gate HEMT.

IV. *I–V* CHARACTERISTICS VALIDATION

Fig. 4(a) and (b) presents the transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) characteristics, respectively, for a device characterized by specific geometric dimensions (width $W = 36$ mm, gate length $L_G = 1.5$ μm, gate-to-source distance $L_{\text{GS}} = 0.75$ μm, and gate-to-drain distance $L_{\text{GD}} = 15.75$ μm), where the I–V measurements are represented by median curves.

These characteristics are analyzed for both the device with uniform p-GaN doping and the device with engineered gradient p-GaN doping. To accurately model the drain–source current, we utilized the drift-diffusion model with gradual channel approximation while considering the voltage drop across the junction contact (ΔV_j) [11], [15]

$$I_{\text{DS}} = \frac{\mu_{\text{eff}} C_d W}{L_G\sqrt{1 + \delta \Delta\psi_{\text{ch,ds}}^2}} \left(V_{\text{GS}} - \Delta V_j - \Delta\psi_{\text{ch},m} + V_{\text{th}}\right)\Delta\psi_{\text{ch,ds}} \tag{4}$$

where μ_{eff} represents the effective mobility, C_d denotes the capacitance per unit area between the gate electrode and the 2DEG, crucial for achieving improved matching, δ is the model parameter, and $\Delta\psi_{\text{ch,ds}} = \Delta\psi_{\text{ch},d} - \Delta\psi_{\text{ch},s}$ is the difference between the surface potentials at the drain and source, respectively.

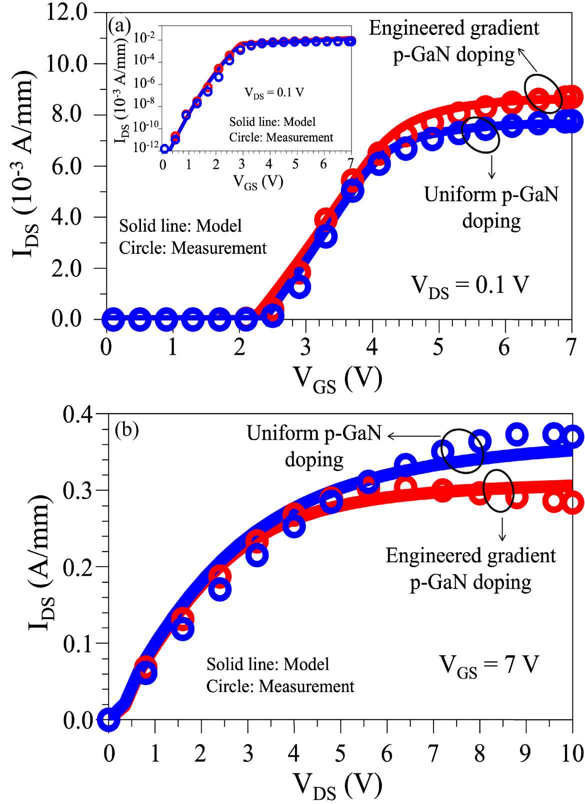

Fig. 4. Plots of (a) I_D–V_{GS} on both linear and logarithmic scales and (b) I_D–V_{DS} characteristics of the p-GaN gate HEMTs ($W = 36$ mm, $L_G = 1.5$ μm, $L_{GS} = 0.75$ μm, and $L_{GD} = 15.75$ μm).

In addition, V_{th} represents the thermal voltage, and $\Delta\psi_{ch,m} = (\Delta\psi_{ch,d} + \Delta\psi_{ch,s})/2$ is the average surface potential between the drain and source. The accurate validation of the model with experimental data necessitates the consideration of various factors, including self-heating, access region characteristics, and temperature effects. A current-dependent nonlinear access region is formulated as follows [16]:

$$I_{acc,s/d} = \frac{1}{R_0} \cdot \frac{V_{acc,s/d}}{\left(1 + \left(\frac{V_{acc,s/d}}{V_{acc,sat}}\right)^{\theta}\right)^{\frac{1}{\theta}}} \tag{5}$$

where $V_{acc,s/d}$ represents the voltage drop across the access regions, while $V_{acc,sat}$ denotes the saturation voltage in the access regions, approximated by $E_{crit} \times L_{acc,s/d}$, where $L_{acc,s/d}$ denotes the access region length. The low-field resistance of access regions, R_0, is given by $(R_{sh}L_{acc,s/d})/W$, where R_{sh} is the sheet resistance of the access regions. The self-heating effect is accounted for by considering two parallel thermal RC networks, incorporating the temperature dependence of several parameters, such as E_{crit}, μ_{eff}, R_{sh}, and V_{th}. The extracted parameters, as shown in Table II, are based on the model's validation with experimental data. Notably, the primary difference in current between uniform p-GaN doping and engineered p-GaN doping is attributed to C_d and a slight reduction in the mobility of engineered p-GaN doping.

TABLE II
EXTRACTED PARAMETERS FOR I–V FITTING

Parameter	Symbol	Value(uniform, engineered gradient)
Gate-2DEG capacitance per unit area	C_d	$0.0034, 0.004\ F/m^2$
Low field mobility	μ_{eff}	$0.14, 0.13\ m^2/Vs$
Sheet resistance	R_{sh}	$580, 590\ \Omega/\square$
Critical electric field	E_{crit}	$2\times10^6, 2\times10^6\ V/m$

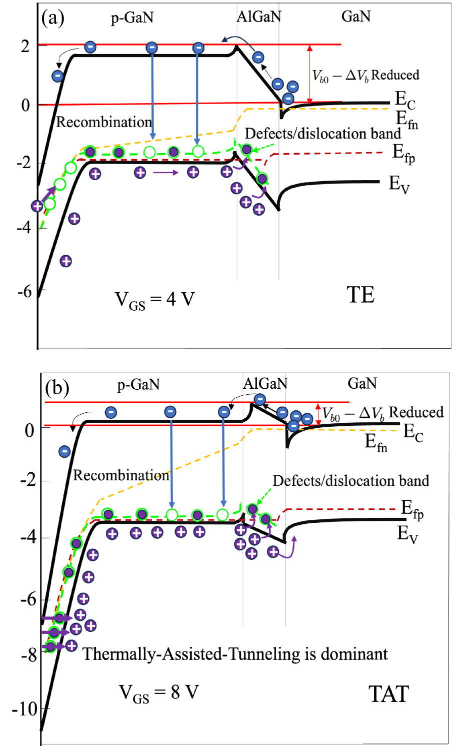

Fig. 5. Simulated band diagram illustrating the leakage mechanisms, including (a) TE and (b) TAT.

V. GATE LEAKAGE CURRENT MECHANISMS

The gate leakage conduction mechanisms in p-GaN HEMTs change depending on the gate voltage. In this section, we utilize the results obtained from modeling the junction voltage ΔV_j for both uniform and gradient p-GaN doping devices to calculate the electric field and gate leakage current. Below the threshold voltage ($V_{GS} < V_{TH}$), Poole–Frenkel (PF) model dominates; for $V_{TH} < V_{GS} < 5$ V, TE prevails. At $V_{GS} > 5$ V, thermally assisted tunneling (TAT) is the predominant mechanism. Fig. 5 presents the simulated band diagram to illustrate the leakage mechanisms, including TE and TAT in p-GaN gate HEMTs.

A. Low Gate Voltage Regime ($V_{GS} \leqslant 2$ V)

In the presence of a negative gate-to-source voltage, the channel is not yet formed (since E-mode devices are considered); it is obvious that the gate current leakage has another origin than under forward gate bias conditions above the

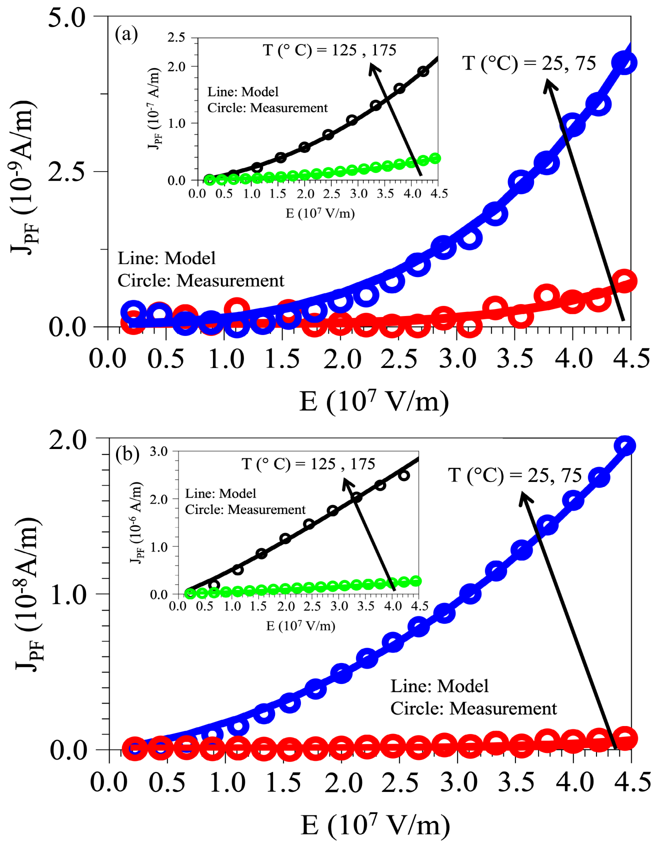

Fig. 6. Comparison of experimental data with curve fitting using the PF model for two cases under reverse bias. (a) Uniformly doped p-GaN and (b) engineered gradient p-GaN doping. The inset shows the fitting of the PF model with experimental data at higher temperatures: 125 °C and 175 °C.

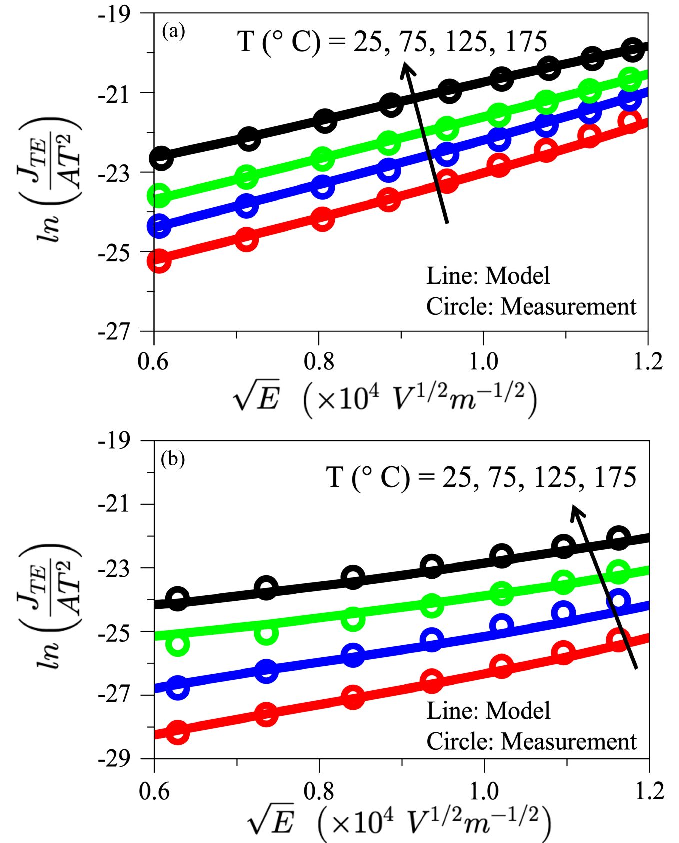

Fig. 7. Comparison between experimental data and curve fitting using the TE model for two cases. (a) Uniformly doped p-GaN and (b) engineered gradient p-GaN doping for various temperatures.

threshold. The gate leakage current's dependence lies on the perimeter rather than the area of the gate. This means that electrons are flowing along the sidewall of the p-GaN in order to reach the gate metal contact. The reduction of this current by several orders of magnitude can be achieved through effective passivation of the p-GaN sidewall, as demonstrated in the research by Stockman et al. [17], and by retracting the gate metal away from the p-GaN sidewall, as explained in [18].

In the range of gate-to-source voltages less than 2 V ($V_{GS} < 2$), it is observed that the PF model provides the most accurate fit to the experimental measurements (at room temperature). The temperature coefficient can be incorporated into the model by multiplying the temperature T with $(T/T_{300})^{\alpha}$, from which α can be extracted when the best fit is achieved for higher temperatures. As can be seen from Fig. 6, the leakage current in this region is higher for the engineered p-GaN doping device compared to the device featuring standard uniform p-GaN. This could be due to the addition of n-doped Si, which could lead to pinning of the Fermi level closer to the conduction band of the GaN (especially at the top part of the gate between the sidewall and the gate metal), resulting in an increased leakage current. Equation (6) corresponds to the PF model. To overcome the perimeter dependence of PF, the length of the device is considered to be an effective length of the gate metal edge where the electrons are injected into the localized traps, which is approximately 10 nm long

$$I_{PF} = C_{PF} \times W \times E \times \exp\left(-\frac{q\left(\varphi_t - \beta_{PF}\sqrt{E}\right)}{k_B T}\right). \quad (6)$$

We introduce the parameter C_{PF}, expressed as $C_{PF0} = q \times N_C \times \mu_n \times L_{eff}$, where q is the elementary charge, k_B is Boltzmann's constant, N_C is the effective density of states, μ_n is the electron mobility, L_{eff} is the effective gate metal edge length, and $E = (V_{GS}/t_{p\text{-GaN}})$ defines the relationship between the electric field (E), V_{GS}, and the thickness ($t_{p\text{-GaN}}$) of the p-GaN layer. In addition, we consider φ_t as the trap depth and define $\beta_{PF} = (q\pi/\varepsilon_{GaN})^{1/2}$, with ε_{GaN} being the relative permittivity of GaN (8.9). The graphical representation in Fig. 6 illustrates the fitting of measurement data at negative V_{GS} values using the PF model at various temperatures. Based on a simplistic electric field analysis, the derived relative permittivity of GaN is 8.1, a value in close proximity to the typical permittivity of 8.9. The derived barrier heights (φ_t) are 0.97 eV for the engineered gradient p-GaN doping device and 0.995 eV for the device employing standard uniform p-GaN.

B. Moderate Regime 2 V < V_{GS} ⩽ 5 V

The Schottky diode is reverse-biased at moderate forward gate voltages, resulting in the p-i-n diode slightly conducting and the current being area-dependent. Based on Fig. 7, the gate leakage current is more dependent on temperature.

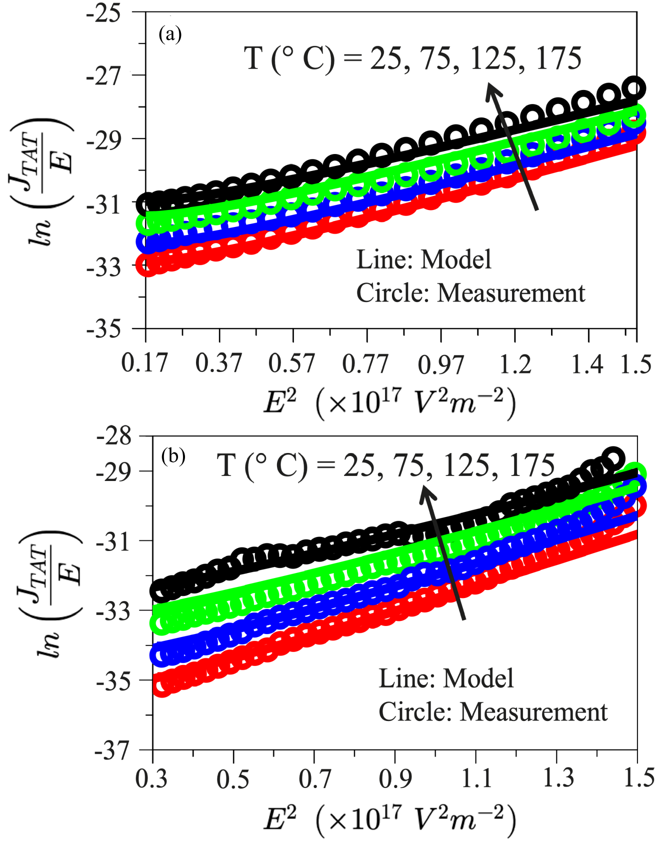

Fig. 8. Comparison between experimental data and curve fitting using the TAT model for two cases. (a) Uniformly doped p-GaN and (b) engineered gradient p-GaN doping for various temperatures.

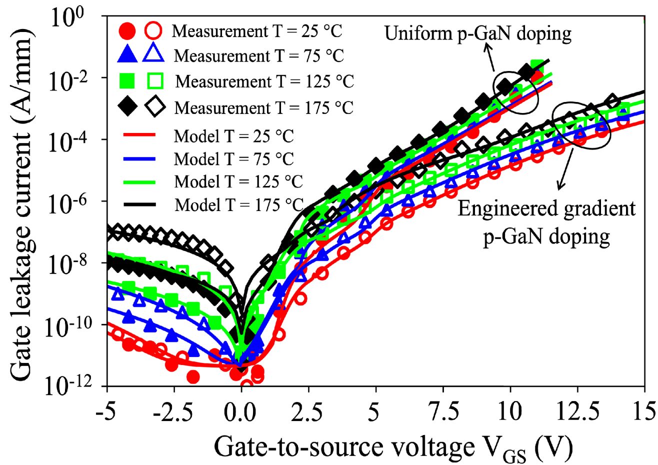

Fig. 9. Gate leakage current versus V_{GS} in engineered p-GaN doping profile and uniform p-GaN doping, PF, TE, and TAT are the main leakage mechanisms involved.

An examination of the measurement results indicates that the most suitable fit is achieved with a model of TE, particularly at room temperature, as depicted in Fig. 7. Fig. 7 illustrates the fitting of measurement data using the TE model, revealing a high degree of agreement across various temperatures. The extracted relative permittivity of GaN from this model is 9.2, close to the typical relative permittivity of GaN. This correlation was previously discussed in [4]. The extracted barrier height (φ_b) is 0.78 eV for the engineered gradient p-GaN doping device and 0.72 eV for uniformly doped p-GaN layer devices, which is significantly lower than the expected barrier height (ϕ_{bn}). The substantial deviation supports the assumption that defect band states are actively involved in TE. Defect band states within the bandgap of the p-GaN material play a significant role in this leakage current. These defects, acting as traps or intermediate energy states, facilitate the emission of holes across the p-GaN barrier under the influence of the applied gate voltage. The presence of these defects provides alternate paths that aid in the movement of holes, contributing to the observed gate leakage current.

TE is modeled by the following equation:

$$I_{\text{TE}} = A \times W \times L_G \times T^2 \times \exp\left(-\frac{q\varphi_b - \beta\sqrt{E}}{k_B T}\right) \quad (7)$$

where A is the Richardson constant, φ_b is effective barrier height, $\beta = (q^3/4\pi\varepsilon)^{1/2}$, and E is the electric field at the effective depletion depth region, which is $E = (\Delta V_j / W_{\text{eff}})$. To analyze the mechanism of gate leakage current in p-GaN HEMTs, an accurate modeling of the electric field is essential. The parameter W_{eff} introduced in [19] represents the effective depletion depth, denoting the region between the gate metal and the edge of the depletion region in the p-GaN where the electric field attains its maximum intensity. It can be expressed as $(W_{\text{eff}}/W_d) = C \times (B/E_{\max})^{-p}$, where the parameters C and p, established as fitting parameters in [19], hold values of 0.6 and 0.41, respectively. The implementation of engineered p-GaN doping techniques leads to an expanded depletion depth at the gate interface, consequently resulting in a reduction of the forward bias gate leakage current.

C. High Voltage Regime $V_{GS} > 5$ V

For high V_{GS}, the gate leakage current follows the thermally assisted-tunneling (TAT) model [4], and the Schottky energy barriers (φ_b^*) are 0.79 eV for the engineered gradient p-GaN doping device and 0.69 eV for the device featuring standard uniform p-GaN, confirming the importance of defect bands that are involved in the leakage mechanism. Defect bands within the p-GaN material's bandgap continue to play a crucial role in this higher voltage-induced gate leakage current. These defects act as intermediate states or traps, aiding in the tunneling process by providing energy levels or pathways for holes to tunnel through the Schottky barrier. The TAT model is expressed by the following equation:

$$I_{\text{TAT}} = C \times W \times L_G \times E \times \exp\left(-\frac{q\varphi_b^* - \frac{1}{6}\left(\frac{hqE}{4\pi k_B T\sqrt{m^*}}\right)^2}{k_B T}\right) \quad (8)$$

where C is

$$C = \sqrt{2\pi m^* k_B T\left(\frac{q}{h}\right)^4}. \quad (9)$$

In (9), h represents Planck's constant, m^* denotes the effective carrier tunneling mass (approximately 0.1 times the mass of a free electron), and q signifies the elementary charge.

Fig. 8 illustrates the fit measurement data using the TAT model at various temperatures. The extracted relative permittivity of GaN from this model remains consistent at 9.2, i.e., the value obtained from the TE model.

Furthermore, it is worth noting that we employed the identical electric field model for both the TAT and the TE regime, which is $E = (\Delta V_j / W_{\text{eff}})$. Fig. 9 illustrates the comparison between the presented model and measured data for gate leakage current versus V_{GS}, revealing a strong agreement between model and measurement.

VI. Conclusion

In this article, we examined the impact of an engineered p-GaN doping profile technique on the reduction of forward bias gate leakage current for p-GaN gate HEMT devices. Our investigation involved the development of a comprehensive model for gate leakage current in both engineered gradient p-GaN doping and uniformly doped p-GaN layer devices. We conducted an in-depth analysis to elucidate the factors contributing to the enhancement of forward bias gate leakage current by modeling fundamental parameters, such as the junction voltage and the electric field at the Schottky metal/p-GaN junction. We have calibrated our model against transfer, output, and gate leakage I–V characteristics, demonstrating a strong agreement over the entire range of V_{GS} values, spanning from negative voltages up to the breakdown voltage.

References

[1] B. Bakeroot, A. Stockman, N. Posthuma, S. Stoffels, and S. Decoutere, “Analytical model for the threshold voltage of p-(Al)GaN high-electron-mobility transistors,” *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 79–86, Jan. 2017.

[2] M. Allaei, M. Shalchian, and F. Jazaeri, “Modeling of short-channel effects in GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3088–3094, Aug. 2020.

[3] A. N. Tallarico et al., “TCAD modeling of the dynamic V_{TH} hysteresis under fast sweeping characterization in p-GaN gate HEMTs,” *IEEE Trans. Electron Devices*, vol. 69, no. 2, pp. 507–513, Feb. 2022.

[4] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, “Schottky gate induced threshold voltage instabilities in p-GaN gate AlGaN/GaN HEMTs,” *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 2, pp. 169–175, Jun. 2021.

[5] S.-W. Tang et al., “Using gate leakage conduction to understand positive gate bias induced threshold voltage shift in p-GaN gate HEMTs,” *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 449–453, Feb. 2023.

[6] A. Stockman et al., “On the origin of the leakage current in p-gate AlGaN/GaN HEMTs,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 4B.5-1–4B.5-4.

[7] K. Liu et al., “The influence of lightly doped p-GaN cap layer on p-GaN/AlGaN/GaN HEMT,” *Semicond. Sci. Technol.*, vol. 37, no. 7, Jul. 2022, Art. no. 075005.

[8] Y. Shi et al., “Carrier transport mechanisms underlying the bidirectional V_{TH} shift in p-GaN gate HEMTs under forward gate stress,” *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 876–882, Aug. 2018.

[9] G. Zhou et al., “Gate leakage suppression and breakdown voltage enhancement in p-GaN HEMTs using metal/graphene gates,” *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 875–880, Mar. 2020.

[10] M. Borga, N. Posthuma, A. Vohra, B. Bakeroot, and S. Decoutere, “Enhancing the forward gate bias robustness in p-GaN gate high-electron-mobility transistors through doping profile engineering,” *Phys. Status Solidi, A*, vol. 10. Apr. 2024, Art. no. 2400043.

[11] N. Modolo, S.-W. Tang, H.-J. Jiang, C. De Santi, M. Meneghini, and T.-L. Wu, “A novel physics-based approach to analyze and model E-mode p-GaN power HEMTs,” *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1489–1494, Apr. 2021.

[12] B. Bakeroot, S. Stoffels, N. Posthuma, D. Wellekens, and S. Decoutere, “Trading off between threshold voltage and subthreshold slope in AlGaN/GaN HEMTs with a p-GaN gate,” in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 419–422.

[13] J. Blakemore, “Approximations for Fermi–Dirac integrals, especially the function $F_{12}(\eta)$ used to describe electron density in a semiconductor,” *Solid-State Electron.*, vol. 25, no. 11, pp. 1067–1076, 1982.

[14] N. Karumuri, S. Turuvekere, N. DasGupta, and A. DasGupta, “A continuous analytical model for 2-DEG charge density in AlGaN/GaN HEMTs valid for all bias voltages,” *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2343–2349, Jul. 2014.

[15] S. Khandelwal, F. M. Yigletu, B. Iñiguez, and T. A. Fjeldly, “Analytical modeling of surface-potential and drain current in AlGaAs/GaAs HEMT devices,” in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Nov. 2012, pp. 183–185.

[16] D. R. Greenberg and J. A. del Alamo, “Velocity saturation in the extrinsic device: A fundamental limit in HFET’s,” *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1334–1339, Aug. 1994.

[17] A. Stockman et al., “Gate conduction mechanisms and lifetime modeling of p-Gate AlGaN/GaN high-electron-mobility transistors,” *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5365–5372, Dec. 2018.

[18] S. Stoffels et al., “Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–10, doi: 10.1109/IRPS.2019.8720411.

[19] P. Mars, “Temperature dependence of avalanche breakdown voltage temperature dependence of avalanche breakdown voltage in p–n junctions,” *Int. J. Electron.*, vol. 32, no. 1, pp. 23–37, Jan. 1972.