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A novel plasma etching technology of RIE-lag free TSV and dicing processes for 3D chiplets interconnect

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***Abstract*—This paper presents the development and application of a dual-frequency ICP etching system for the fabrication of 3D-IC. The system is designed to address the increasing need for efficient CPUs and HBM in data centers, in response to the global exponential growth of data. The dual-frequency ICP etching system enhances the etching process by increasing the electron temperature inside the plasma, promoting the dissociation of the process gas. The system's application in non-Bosch TSV etching technology and plasma dicing demonstrates its potential in providing smooth sidewalls and ensuring the long-term reliability of logic stacked devices. Furthermore, the introduction of a new etching method, the Dual TSV Process, minimizes aspect ratio dependent RIE-lag, enabling the fabrication of TSVs of two different diameters at a uniform depth. This technology increases the device design flexibility and enables the fabrication of higher density devices.**

***Keywords*—Dual-frequency ICP, TSV, Non-Bosch etch, Plasma dicing, RIE-lag free etch**

I. Introduction

In recent years, the global implementation of artificial intelligence (AI) technologies across various industries has led to a significant increase in the amount of information. The volume of data generated, acquired, replicated, and consumed worldwide annually is expected to continue its exponential growth, rising from 15.5 ZB (zettabytes, 10^{21} bytes) in 2015 to 64.2 ZB in 2020, and is projected to reach 181 ZB in 2025 [1]. In light of this global trend, the need to enhance the efficiency of central processing unit (CPU) and high bandwidth memory (HBM) for data centers has emerged as a societal issue. Three-dimensional integrated circuit (3D-IC) technology has been recognized as a promising means to realize high performance computing (HPC) as described above [2]. 3D-IC technology has already been applied to products with stacked memory such as HBM, and in recent years, the stacking of heterogeneous chips such as logic and logic or logic and memory has also been actively considered. For instance, Intel's Foveros [3], tsmc's SoIC [4], and Samsung's 3.5D [5] are each designing HPCs with their own unique technologies. Through silicon via (TSV), which enables electrode formation on the back side of the silicon substrate, is primarily used for 3D fine interconnections, and chips such as logic circuits and memories designed using TSV are arranged three-dimensionally to realize 3D-IC. The Bosch method using 13.56MHz radio frequency (RF) inductively coupled plasma (ICP) is a common method for etching. In this study, we developed a dual-frequency ICP etching system in which a different RF frequency is superimposed on the 13.56 MHz RF, and developed a new TSV etching technology.

II. Equipment and Technology Overview

A. Equipment Configuration

Figure 2 provides an overview of the dual-frequency ICP etching system. The antenna for dual-frequency ICP, which is a feature of this system, is placed above the dielectric window at the top of the chamber so that the center of the coil aligns with the center of the stage. The shape of the antenna is a spiral, and C1020 oxygen-free copper was used as the material. Two coils were placed on the coaxial antenna, with the inner antenna connected to a 13.56 MHz RF and the outer antenna to a lower frequency RF than the inner antenna via matching circuits. An alumina nozzle supplying the process gas was placed in the center of the dielectric window. Gas inlet ports were also placed evenly around the perimeter of the chamber to allow control of the gas flow in the chamber. The stage is designed to apply 400 kHz RF as a bias, and Electrostatic Chuck (ESC) are placed on the surface to fix the wafer. The surface of the ESC is cooled by a two-zone He cooling system. A turbo molecular pump is

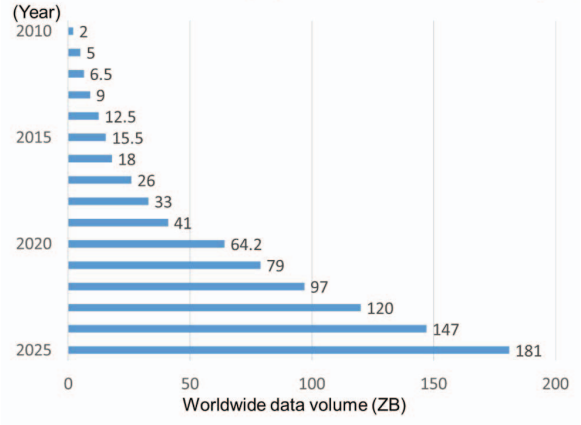

Fig. 1 The volume of data generated worldwide [1].

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connected for exhaust and a pendulum type control valve is used to regulate the pressure in the chamber.

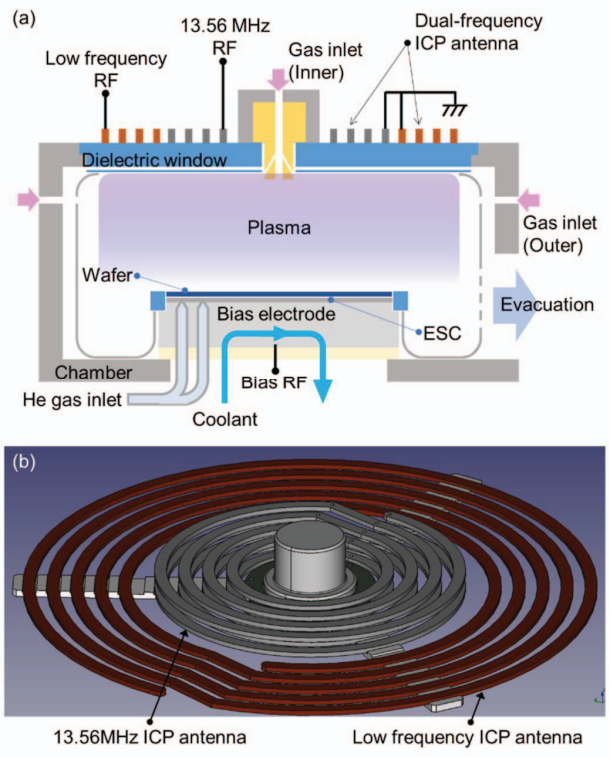

Fig. 2 (a) Overview of the dual-frequency ICP etching system, (b) 3D Computer Aided Design (CAD) drawing of the antenna dedicated.

B. *Effects of Dual-frequency ICP*

As mentioned at the beginning of this document, general ICP etch systems use 13.56 MHz RF for ICP generation. This is because it is in the industrial scientific and medical (ISM) band, which is industrially accessible, and also because it is an easy frequency to fabricate ICP antennas in terms of circuit constants. In this system, 13.56 MHz RF is applied to the inner ICP antenna and low frequency RF is applied to the outer ICP antenna. The increase of electron temperature inside the plasma by applying 2 MHz RF to the 13.56 MHz plasma was reported by Ju-Ho Kim et al [6] and Anurag Mishra et al [7]. According to this report, an effective electron temperature increase cannot be obtained by increasing the 13.56 MHz power input alone, and a higher electron temperature can be obtained only by superimposing a low-frequency RF. This is a useful report as a physical basis for applying the effect of our intended high electron temperature to the etching of Si, by promoting the dissociation of the process gas. Figure 3 provides an overview of Si etching when only 13.56 MHz RF is used as the plasma source and when 13.56 MHz RF and low frequency RF are superimposed. The process gases are basically SF_6 and O_2, and necessary gases may be added depending on the situation. The fluorine radical obtained by dissociating SF_6 with plasma is used as an etching species to etch silicon, and Nakano et al. reported how SF_6 dissociates

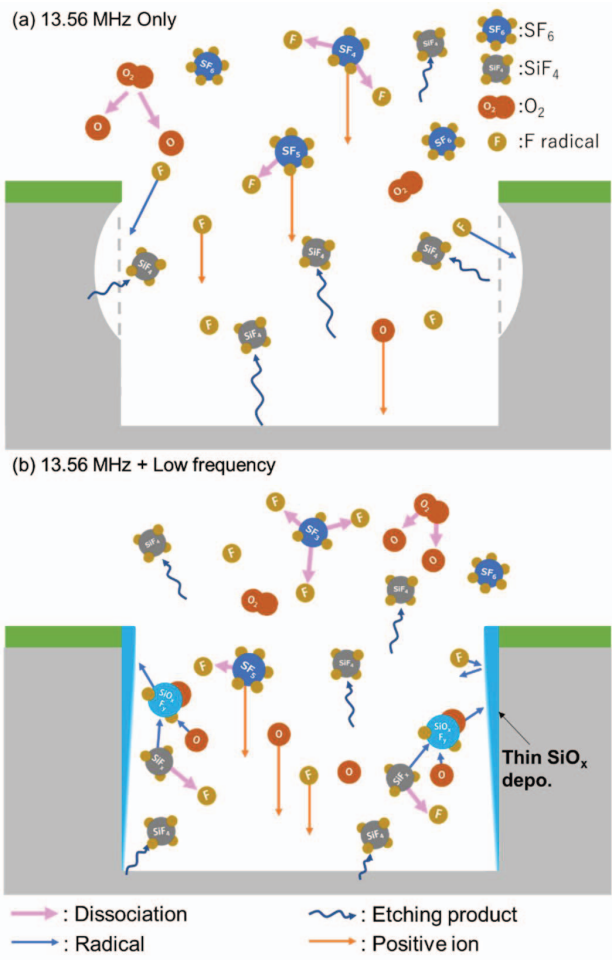

Fig. 3 Mechanism of process gas dissociation and silicon etching in non-Bosch silicon etching. (a) with 13.56 MHz RF, (b) with 13.56 MHz RF superimposed on low frequency.

upon collision with electrons to form the fluorine radical [8]. In addition, silicon reacts with the fluorine radical to form SiF_4 and volatilizes to form SiF_4, resulting in etching of silicon [9].

Particles that dissociate and become single fluorine atoms are ionized into fluorine ions, which are given a vertical direction of motion by the bias, and fluorine radicals, which have free molecular motion as neutral particles. Since a large proportion of the fluorine radicals have a horizontal motion component, they strike the sidewalls of the etching surface and cause bowing, which is undesirable for TSVs, where a copper seed layer must be deposited to form through-hole wiring, because such a bowing shape causes the seed layer to be cut off or to be non-uniform. ICP with a superimposed low frequency of 13.56 MHz produces an ICP with a high electron temperature, which promotes dissociation of the process gas, as mentioned above, resulting in a relative increase in the amount of fluorine radicals and fluorine ions obtained by SF_6 dissociation and an increase in the silicon etching rate. The etch product, SiF_4, is volatilized and exhausted out of the TSV in the usual ICP using only 13.56 MHz. On the other hand, in ICP with superimposed low frequency, SiF_4 molecules can dissociate due to the high

electron temperature and combine with oxygen atoms dissociated from O_2 gas to form SiO_xF_y, which adheres to the etched surface to form a SiO_x film [10]. The film has a thickness of less than 10 nm in the case of normal processes. This film acts as a protective film on the sidewall and prevents etching of the sidewall by fluorine radicals. Although SiO_x film is also formed on the bottom of TSV, etching is dominant only at the bottom due to anisotropy caused by ion attraction by bias RF, resulting in etching progressing only in the vertical direction. As a result, TSVs with vertical and smooth sidewalls can be formed by continuous etching.

III. Overview of the Etching Process

A. Non-Bosch TSV Etching

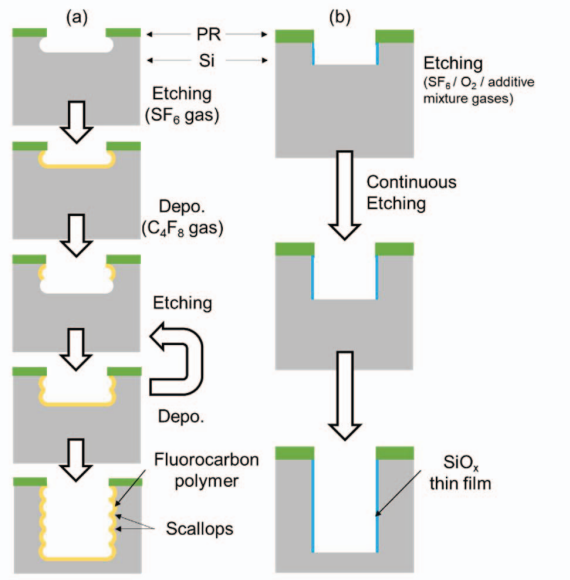

Fig. 4 Comparison of TSVs processed by the Bosch method using ordinary ICP and those processed by the non-Bosch method using dual-frequency ICP. (a) with the Bosch method, (b) with the non-Bosch method.

TABLE I. Comparison of TSV etching by the Bosch method using a conventional 13.56 MHz ICP and TSV etching by the non-Bosch method using a dual-frequency ICP

	TSV Fabrication Method	
	Non-Bosch TSV	***Bosch TSV***
Process	Continuous	Cyclic
Selectivity	about 20	Infinite
Verticality	Variable(85-95 deg)	Vertical only
Scallop	No scallop	With scallop

The non-Bosch TSV etching technology holds promise for ensuring the long-term reliability of logic stacked devices. Figure 4 shows an overview of the normal Bosch process and the Non-Bosch process and Table 1 shows Difference in

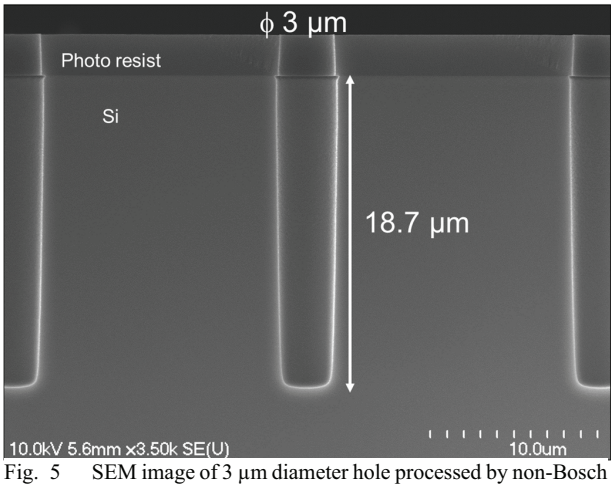

Fig. 5 SEM image of 3 μm diameter hole processed by non-Bosch etching.

properties by TSV processing method. This is due to its ability to facilitate TSV processing in a single step, without the need for the Bosch method, and its provision of smooth sidewalls. Unlike memory, which possesses redundant circuits, wiring defects are not tolerated in logic circuits. TSVs formed by the Bosch method, a conventional technology, exhibit characteristic sidewall steps known as scallops. These steps pose an obstacle during seed layer deposition and can lead to issues such as increased leakage current, thereby deteriorating device characteristics [11] [12]. Scallops are known to occur due to repetitive etching and protective film formation. The TSV obtained by continuous etching, which deviates from the Bosch method, has the potential to eliminate such defects. Figure 5 shows scanning electron microscope (SEM) images of TSVs processed by the non-Bosch method using a dual-frequency ICP

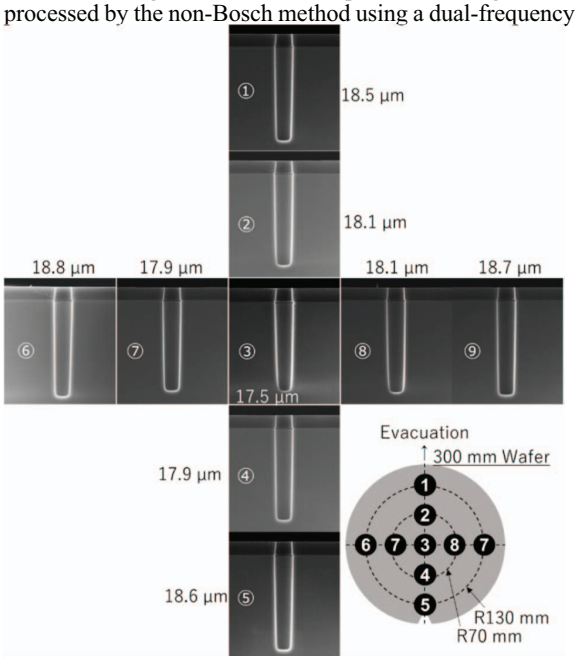

Fig. 6 Distribution of TSVs with a diameter of 3 μm processed by the non-Bosch etching method.

etching system. Continuous silicon etching was performed on a 3 µm diameter hole pattern using SF_6/O_2 and additive gases. The plasma source and equipment were the dual-frequency ICP etching system described above. The hole patterns were fabricated with an i-line stepper and a 3.5 µm thick resist. As a result, an aspect ratio of 6.2, an etching depth of 18.7 µm, and an etching rate of 9.5 µm/min were achieved. The SEM image shows that no surface roughness such as scalloping, which occurs in the Bosch method, was observed. Figure 6 shows the results of the comparison of shapes within the wafer plane. It can be seen that the etching depth distribution is 3.6%, and the same vertical shape is obtained in the entire in-plane area.

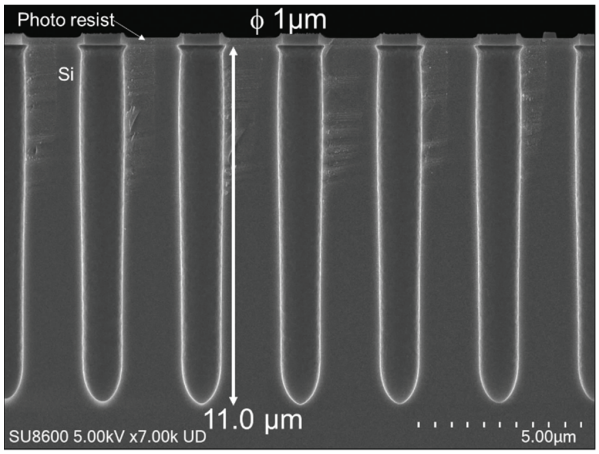

Fig. 7 SEM image of 1 µm diameter hole processed by non-Bosch etching.

Based on the above etching results, we attempted to develop a process for "small TSV" etching with a diameter of 1 µm. The resulting SEM image is shown in Figure 7. The hole pattern was fabricated with an i-line stepper and a 0.8 µm thick photoresist was used. By optimizing the etching gas flow ratio and stage temperature, an aspect ratio of 11, etching depth of 11.0 µm, and etching rate of 5.5 µm/min were achieved. The selectivity ratio with photoresist at this time was 20. In this result, it can be confirmed that the smooth sidewall shape due to continuous etching is maintained. The impact of the non-Bosch process on the sequential steps of TSV fabrication, including barrier/seed layer deposition and metal Eelectro chemical deposition(ECD), versus TSVs using the Bosch process, and the full flow of TSV fabrication when the non-Bosch process is introduced for etching holes in silicon have been verified in the past, and similar verification will be done for TSVs of the sizes fabricated in this report[13].

B. Plasma Dicing with Non-Bosch Etching

Plasma dicing was performed using a non-Bosch process to continuously etch silicon. Blade dicing using rotating blades has long been used to chip wafers, but there have been issues such as damage caused by blade impact and particles from chips. Recently, a method using a converging laser called stealth dicing has also been used, but it has problems with damage caused by internal stresses in the dicing line and roughness in the side wall shape. Plasma dicing is expected to solve these problems. Since it is basically a dry process and etch products are discharged as gases, there are few particles and no physical damage to the wafer or chip. Figures 8 and 9 show the results of Si dicing by the non-Bosch method. Figure 8 shows the result of processing a 40 µm thick chip placed on top of the adhesive layer with a 3 µm thick photoresist. The processing was perpendicular to the dicing line with a width of 12 µm and smooth side walls. The etching rate was 10 µm/min. Figure 9 shows the result of plasma dicing with a 10 µm thick photoresist on a silicon wafer. The dicing line width was 50 µm. As a result, a 230 µm deep profile with smooth sidewalls was obtained with an etching rate of 14 µm/min. The aspect ratio of dicing can be up to about 10, and by optimizing the width of the scribe line and the thickness of the photoresist, it is possible to cut wafers before thinning to, for example, 775 micrometers.

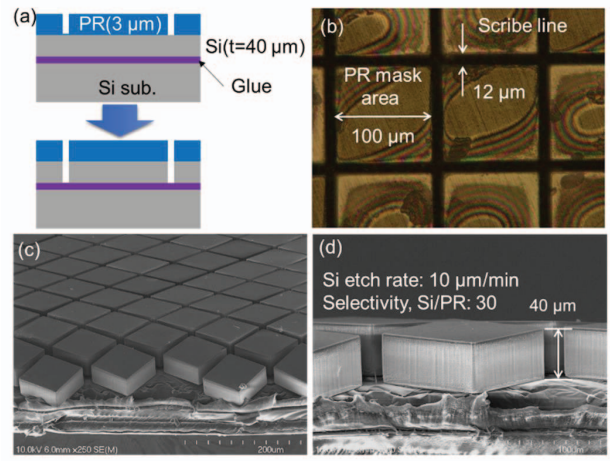

Fig. 8 Result of plasma dicing of 12 µm wide scribe line by non-Bosch etching using dual-frequency ICP. (a) experimental overview, (b) optical micrograph after processing (×1000), (c) overall SEM image of plasma dicing result, (d) Detailed SEM image of plasma dicing process result.

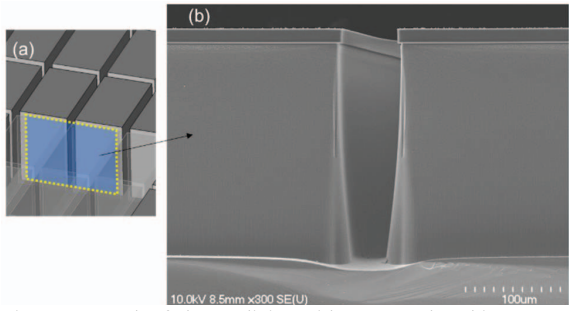

Fig. 9 Result of plasma dicing with non-Bosch etching on a 50 µm wide scribe line using dual-frequency ICP. (a) Cracked area (dashed line), (b) Cross-sectional SEM image of plasma dicing process result.

At the same time, we attempted to process Die Attach Film (DAF). The DAF(LINTEC Corporation: Adwill LE5000S) was etched with O_2 plasma through a 30 µm wide dicing line between 50 µm thick chips and the DAF placed underneath it, resulting in an etching rate of 1.13 µm/min. The DAF etching tested this time was an etching evaluation of DAF before molding and before hard cure. Etching of substrates that have already been molded, such as 2.5D, will also be evaluated in the future.

C. *Dual TSV Process*

A new etching method called Dual TSV Process was developed using a dual-frequency ICP etching system. Normally, when Via with different diameters are processed at once, a difference in etching depth called Reactive Ion Etching (RIE)-Lag occurs. Our new silicon etching technique achieves the minimization of aspect ratio dependent etching lag, and thus contributes to fabricating TSVs of two different diameters at a uniform depth, which enable high density wiring by reducing the area occupied by TSVs in the wiring area. Figure 10 shows a comparison of the conventional Bosch process and the Dual TSV process. The Bosch process is widely used as an effective means of silicon deep etching. The Dual TSV process is an improved version of the Bosch process. In the Bosch process of repeated deposition and etching, thicker deposition can generate inverse micro-loading effect, slowing the progression of larger diameter via and reducing the RIE-lag between smaller and larger via. In addition, by conducting deposition using C_4F_8 gas with Dual ICP, the Bottom part / Top part (B/T) ratio, which is the ratio of the thickness of the film on the surface layer around the via (Top part) to the thickness at the bottom of the via (Bottom part), can be increased from 0.22 to 0.44, allowing more effective use of the inverse micro-loading effect can be more effectively utilized.

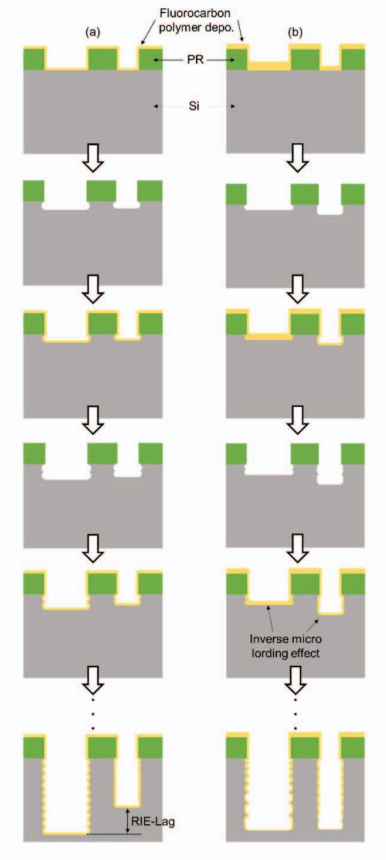

Fig. 10 Process flow diagram for batch processing of TSVs with different diameters. (a) using the conventional Bosch method, (b) using the Dual-TSV.

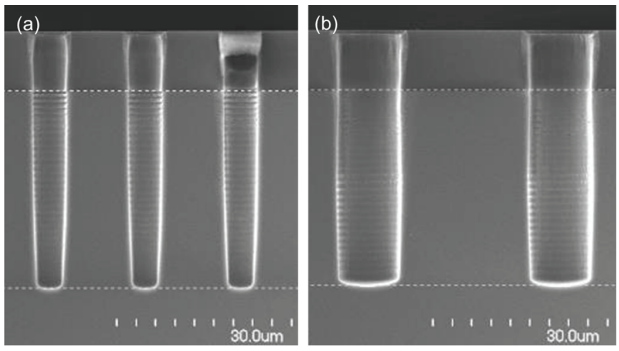

Fig. 11 Results of Dual TSV Process using dual-frequency ICP on different diameter vias on the same wafer. (a) Dual TSV Process results for a 5 μm diameter hole, (b) Dual TSV Process results for a 10 μm diameter hole.

Figure 11 shows SEM images of the results of applying the Dual TSV process to simultaneously process 5 μm diameter via and 10 μm diameter via. A photoresist thickness was 10 μm, the same conditions as for the Non-Bosch process were applied for the etching step, and C_4F_8 gas was used for the deposition step. In TSV processing with adjusted RIE-lag, the RIE-lag was almost 0 % when etching 5 μm diameter via and 10 μm diameter via to a depth of 30 μm. As mentioned above, it was found that by applying the Dual TSV process, Via with different diameters can be simultaneously processed to the same depth. This allows the diameters of the signal and power lines connecting to the memory chip to be set to different diameters without process changes. By designing smaller signal lines, the diameters of the associated lands can also be reduced. Figure 12 shows a cross section of a 3D-IC chip and a schematic diagram of the interconnect layers. In a typical design, signal lines and power lines are designed with the same diameter. In the figure, the hole diameter is 5 μm, and the land diameter is 8 μm. If the pitch between holes is 13 μm and the design rule for interconnections is Line / Space = 1 / 1 μm, the number of interconnections that can pass between holes is 3. The number of interconnections that can be passed between the holes is four. This increases the

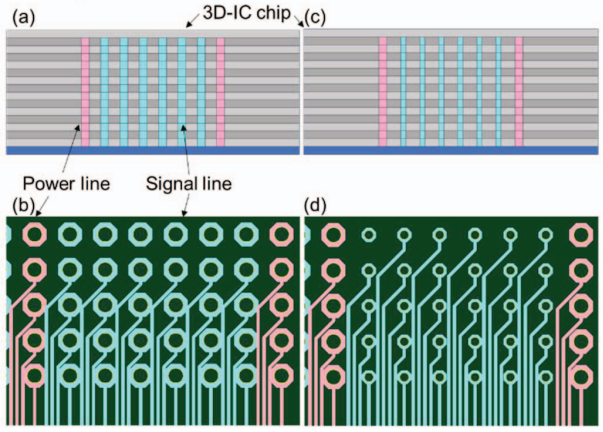

Fig. 12 Cross-section of 3D-IC chip and schematic diagram of wiring layers. (a) Same diameter power and signal lines using conventional Bosch process (b) Smaller diameter signal lines using Dual TSV process.

degree of freedom in designing the interconnect layers, enabling the creation of smaller, higher-density devices.

IV. Conclusion

TSV etching with smooth sidewalls of 1 μm in diameter was achieved using a dual-frequency ICP etching system. This technology is expected to be useful for 3D-IC, especially in the fields of Logic-Logic stacking and SRAM-SRAM stacking.

In addition, non-Bosch plasma dicing of device chips with smooth sidewalls was attempted using the same system, and dicing of device chips with smooth sidewalls was achieved at a processing speed of 14 μm/min. The etching rate of DAF was confirmed to be 1.13 μm/min when the dicing line was 50 μm.

The Dual TSV process was developed by taking advantage of the characteristics of the dual-frequency ICP etching system, and it was possible to simultaneously process a 5 μm diameter via and a 10 μm diameter via to a depth of 30 μm. This technology increases the degree of freedom in device design and enables the fabrication of higher density devices.

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