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RESEARCH ARTICLE

Low Loss and Low EMI Noise Trench IGBT with Shallow Emitter Trench Controlled P-Type Dummy Region

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Abstract — A novel trench insulated gate bipolar transistor (TIGBT) with a shallow emitter trench controlled P-type dummy region (STCP-TIGBT) is proposed. Compared with the conventional TIGBT with floating P-type dummy region (CFP-TIGBT) and TIGBT with floating P-type dummy region and normally on hole path (HFP-TIGBT), the proposed STCP structure not only speeds up the extraction of excessive holes in the turn-off process but also reduces the Miller plateau charge (Q_{gc}). Therefore, both the power loss and electromagnetic interference (EMI) noise are significantly reduced. Simulation results show that the Q_{gc} of the proposed device is only 501 nC/cm^2, which is reduced by 58.5% and 26.4% when compared to the CFP-TIGBT and HFP-TIGBT, respectively. At same on-state voltage drop (V_{ceon}) of 1.02 V, the turn-off loss (E_{off}) of the proposed device is 13.49 mJ/cm^2, which is 64.6% and 67.6% less than those of the CFP-TIGBT and HFP-TIGBT, respectively. Moreover, the reverse recovery dV_{ak}/dt of the freewheeling diode at same turn-on loss (E_{on}) of 31.8 mJ/cm^2 for the proposed STCP-TIGBT is only 2.15 kV/μs, which is reduced by 91.3% and 57.2% when compared to 24.69 kV/μs and 5.02 kV/μs for the CFP-TIGBT and HFP-TIGBT, respectively. The reduced dV/dt significantly suppresses the electromagnetic interference noise generated by the proposed device.
Keywords — Trench insulated gate bipolar transistor, On-state voltage drop, Turn-off loss, Turn-on loss, Electromagnetic interference noise, Shallow emitter trench, P-type dummy region.
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I. Introduction

Trench insulated gate bipolar transistor (TIGBT) is one of the mainstream power switching devices used in the power electronic systems due to its superior device performance and reliability [1], [2]. As a bipolar device, one of the primary tasks for the design of a high performance TIGBT is to improve the trade-off relationship between the on-state voltage drop (V_{ceon}) and turn-off loss (E_{off}) [3], [4]. In the last few decades, various TIGBTs with different injection enhancement (IE) techniques, such as narrow mesa [5]–[7], carrier stored (CS) layer [8], [9], and floating P-type (FP) dummy region [10], have been proposed. These proposed IE techniques not only enhance the conductivity modulation but also optimize the carriers' distribution in the N-drift region, which derives an improved IGBT device performance. However, for the TIGBT with narrow mesa, such as IGBT with partially narrow mesa structure (PNM-IGBT), fin P-body IGBT or side gate HiGT, their fabrication process are complex and still not mature. For the TIGBT with CS layer (CSTBT), the highly-doped n CS layer brings a negative impact on the breakdown voltage (BV), which limits the further improvement of the device [11], [12]. And for the conventional TIGBT with FP dummy region (CFP-TIGBT), although the IE effect derived from the relatively wide FP dummy region improves the V_{ceon}-E_{off} trade-off relationship, the interaction between the gate

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and FP dummy region not only increases the gate charge (Q_g), especially the miller plateau charge (Q_{gc}) but also deteriorates the gate controllability on the dV/dt of the devices, especially on the reverse recovery dV_{ak}/dt of freewheeling diode (FWD). The large Q_{gc} limit the further improvement of the E_{off} and the poor gate controllability on the dV_{ak}/dt of FWD limits the further improvement of the trade-off relationship between the electromagnetic interference (EMI) noise and turn-on loss (E_{on}). To overcome the drawback of the CFP-TIGBT, improved TIGBT structures, such as separate floating P-layer TIGBT, floating N-well TIGBT, trench shielded gate IGBT and L-shaped shielding gate TIGBT, have been proposed to separate the FP region from the gate, which improves the gate controllability on the dV/dt of the devices as well as reduces the Q_{gc} at certain extent [13]–[17]. However, the wide FP region still limits the extraction of the hole in the turn-off process, which increases the turn-off time (t_{off}) and E_{off} of the device. To speed up the extraction of the hole in the turn-off process, the FP-TIGBT with normally on hole path (HFP-TIGBT) is proposed [18], [19]. However, the normally on hole path increases the V_{ceon} since the additional hole path also exists in the forward conduction state. To further improve the device performance, FP-TIGBTs with gate-controlled structure were proposed in our previous work [20], [21]. However, the gate-controlled structure inevitably increases the Q_g and also makes the fabrication process a little bit complex since the introduced structure is a depletion structure. In this paper, a novel TIGBT with a shallow emitter trench controlled P-type dummy region (STCP-TIGBT) is proposed. The proposed STCP structure not only speeds up the extraction of excessive holes in the turn-off process but also reduce the Q_g at negligible cost of the V_{ceon}. Hence, not only improved V_{ceon}-E_{off} trade-off relationship but also improved trade-off relationship between the E_{on} and reverse recovery dV_{ak}/dt of FWD are obtained for the proposed device. Utilizing the load effect of etching process, the shallow emitter trench and gate trench can be fabricated at the same time. Hence, the fabrication process of the proposed STCP-TIGBT is fully compatible with that of the CFP-TIGBT.

II. Device Structure and Mechanism

The schematic cross-sectional view of the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT are illustrated in Figures 1(a), 1(b) and 1(c), respectively. The three structures all have a P-type dummy region next to the gate trench on the upper surface. Compared to the CFP-TIGBT, an additional emitter-connected dummy gate trench and a P-type/P+ region is introduced in the surface of the HFP-TIGBT, which forms a normally on hole path. The normally on hole path increases the V_{ceon} since the additional hole path also exists in the forward conduction state. Different from the HFP-TIGBT, the proposed STCP-TIGBT has a shallow emitter trench in the P-type dummy region and a highly-doped N-type buried layer (N-BL) is inserted between the P-type dummy region and emitter-connected P+ layer. The shallow emitter trench can be formed at same process step with the gate trench and fully encapsulated by the P-type dummy region. The P-type dummy region, N-BL, emitter trench and emitter-connected P+ layer form a gate-drain connected P-type trench metal-oxide-semiconductor (TMOS) structure. During turn-on process of the proposed STCP-TIGBT, the TMOS is turned off since the decrease of the collector-emitter voltage (V_{ce}) induces a reduced potential of the P region (V_P). Considering the highly-doped N-BL acts as a hole barrier to prevent the hole flows from the N-drift region to the emitter, the formed structure does not impact the conduction modulation effect in the N-drift region in the forward conduction state, which has negligible impact on the V_{ceon} of the device. During turn-off process of the proposed STCP-TIGBT, with the increase of the V_{ce}, the V_P is increased accordingly. The TMOS is turned on when the V_P is larger than the absolute value of threshold voltage of the TMOS. The turn on of the TMOS clamps the V_P and then forms a hole path.

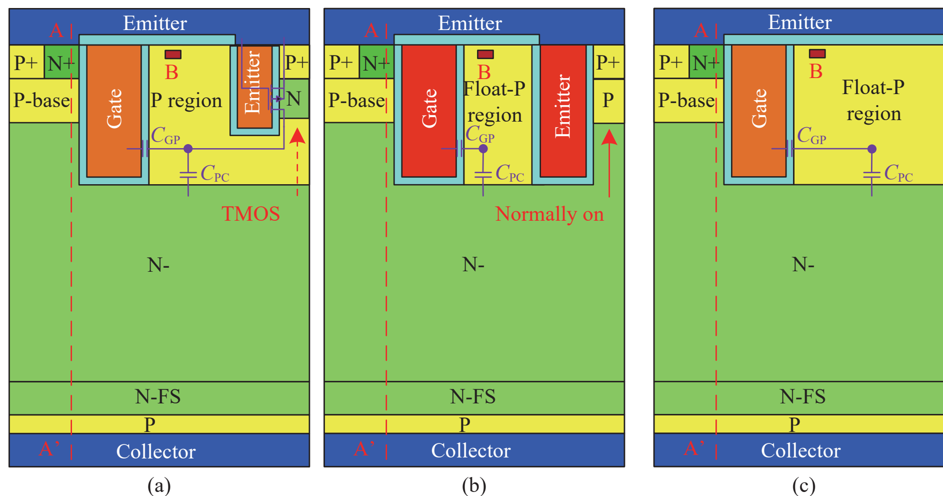


Figure 1 Schematic cross-sectional view of the three TIGBTs. (a) Proposed STCP-TIGBT; (b) HFP-TIGBT; (c) CFP-TIGBT.

Considering the electron and hole current paths, Figures 2(a)–(f) show the equivalent circuits of the three structures during turn-on and turn-off processes, respectively. Moreover, as different capacitances illustrated in the Figure 1, the P dummy region for the proposed device transforms the gate charge between the gate and P-type dummy region from the Q_{gc} to Q_{ge} when the TMOS is on, which reduces the Q_{gc}. The turn on of the TMOS forms a hole extraction path during turn-off process, which reduces the turn-off time and E_{off} of the device. The STCP structure not only speed up the extraction of excessive holes in the turn-off process but also reduce the Q_{gc} at negligible cost of the V_{ceon}. As a result, improved V_{ceon}-E_{off} and E_{on}-dV_{ak}/dt trade-off relationships are obtained for the proposed STCP-TIGBT, which simultaneously reduces the power loss and suppresses the EMI noise.

Numerical analysis with Medici software [22] is performed for the three TIGBTs, and Table 1 lists the main device parameters used in the simulation.

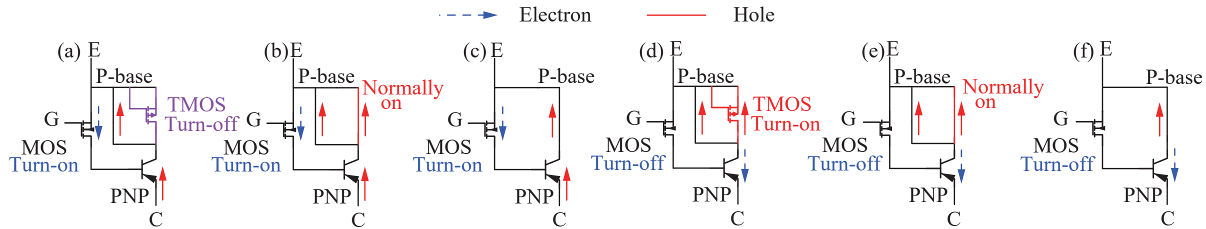


Figure 2 Equivalent circuit for the three TIGBTs considering the electron and hole current paths. (a) Turn-on of the proposed STCP-TIGBT; (b) Turn-on of the HFP-TIGBT; (c) Turn-on of the CFP-TIGBT; (d) Turn-off of the proposed STCP-TIGBT; (e) Turn-off of the HFP-TIGBT; (f) Turn-off of the CFP-TIGBT.

Table 1 Main device parameters used in simulation

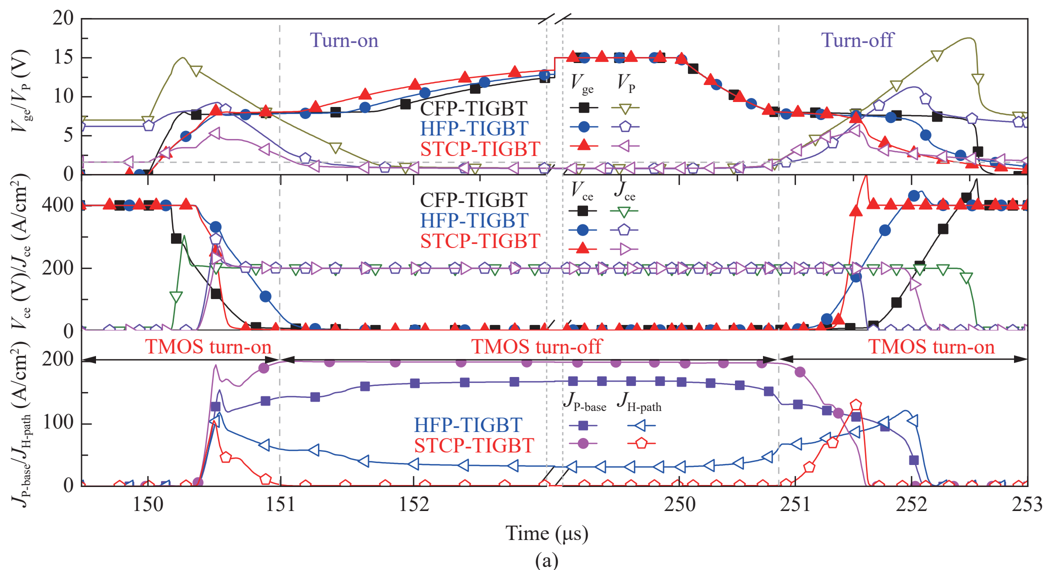
Structure parameters	STCP-TIGBT	HFP-TIGBT	CFP-TIGBT
Half-cell pitch (μm)	3	3	3
Silicon depth (μm)	60	60	60
P+ emitter depth (μm)	0.5	0.5	0.5
P+ emitter doping (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
N+ emitter doping (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
P-base width (μm)	0.3	0.3	0.3
P-base junction depth (μm)	3	3	3
P-base doping (cm^{-3})	1.3×10^{17}	1.3×10^{17}	1.3×10^{17}
Gate trench width (μm)	0.8	0.8	0.8
Gate trench depth (μm)	5	5	5
Gate oxide thickness (μm)	0.1	0.1	0.1
Emitter trench width (μm)	0.4	0.8	–
Emitter trench depth (μm)	4	5	–
Emitter oxide thickness (μm)	0.1	0.1	–
N-BL doping (cm^{-3})	1×10^{17}	–	–
N-BL thickness (μm)	1.5	–	–
P-type dummy region doping (cm^{-3})	1×10^{17}	1×10^{17}	1×10^{17}
N-drift doping (cm^{-3})	2×10^{14}	2×10^{14}	2×10^{14}
N FS doping (cm^{-3})	2×10^{16}	2×10^{16}	2×10^{16}
N FS thickness (μm)	2	2	2
P collector doping (cm^{-3})	1×10^{17}	1×10^{17}	1×10^{17}
P collector thickness (μm)	0.5	0.5	0.5

The key models used in the simulation include the shockley-read-hall recombination, auger recombination model, slotboom bandgap narrowing model, impact ionization model, enhanced surface mobility model, parallel electric field component mobility model and perpendicular electric field component mobility model. To have a meaningful comparison, other than the hole path related region, device parameters for the three TIGBTs are kept

to same.

III. Results and Discussion

Figure 3(a) shows switching waveforms for the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT, respectively. The V_P at the point B marked in the Figure 1 for the three devices are also shown in the figure. To have a better understand on the effect of the additional hole path on the switching process for the proposed STCP-TIGBT and HFP-TIGBT, other than the J_{ce}, the current density flows to the P-base ($J_{\text{P-base}}$) as well as normally on or STCP hole path region ($J_{\text{H-path}}$) are also shown in the figure. The $J_{\text{P-base}}$ includes both the hole current density flows to the P-base region and the electron current density flows via the MOS channel. The sum of the $J_{\text{P-base}}$ and $J_{\text{H-path}}$ is equal to J_{ce} for the two devices with additional hole path. The results are obtained using a clamped inductive load with a gate resistance (R_g) of 10 Ω, J_{ce} of 200 A/cm^2 and bus voltage of 400 V. The gate signal starts to turn on from 0 V to 15 V at $t = 150$ μs and turn off from 15 V to 0 V at $t = 250$ μs, respectively. It can be seen that at the initial forward



(a)

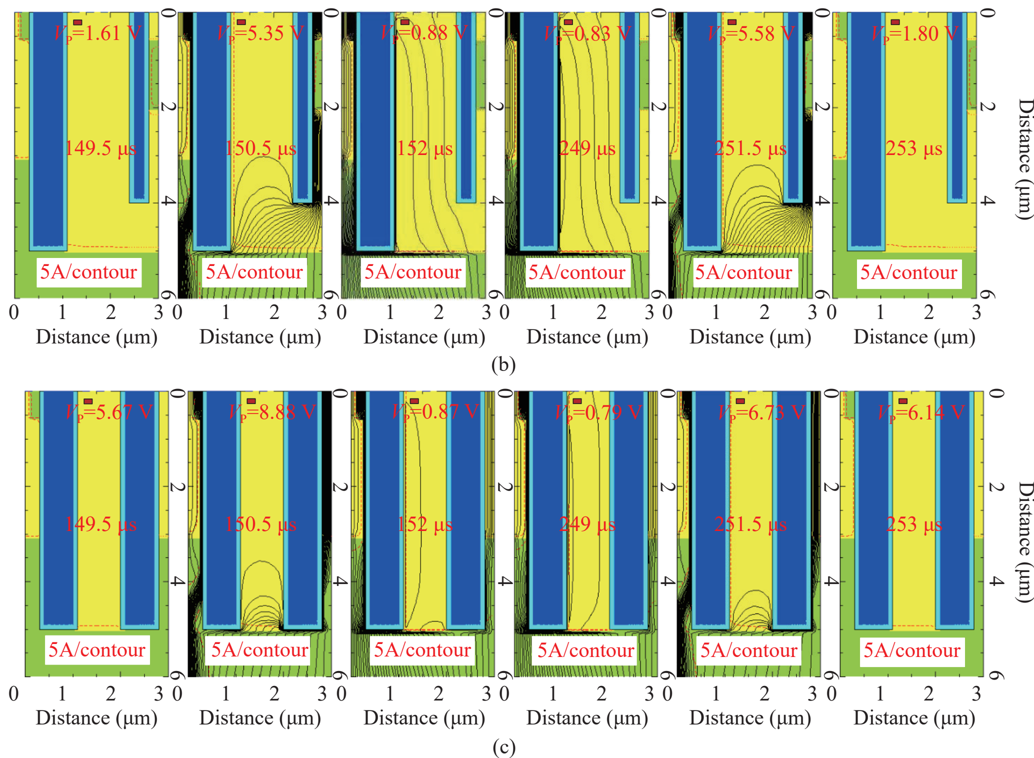


Figure 3 Comparison of switching characteristics for the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT. (a) Switching waveforms; (b) Current flow line distributions for the proposed STCP-TIGBT at different time points; (c) Current flow line distributions for the HFP-TIGBT at different time points.

blocking state before $t = 150$ μs, the V_P of the proposed device is lower than those of the HFP-TIGBT and CFP-TIGBT since the TMOS is on and it clamps the V_P of the proposed device to 1.61 V via the TMOS channel. When the devices turn on, the V_P increases with the V_{ge} at the beginning due to the coupling effect between the gate and P-type dummy region and then it gradually decreases with time as the V_{ce} decreases for the three devices. The change of the $J_{H\text{-path}}$ has similar trend as that of the V_P for the proposed STCP-TIGBT and HFP-TIGBT. For the two TIGBTs with additional hole path, the $J_{H\text{-path}}$ reaches the maximum value at almost same time as that of the V_P and after that, the $J_{H\text{-path}}$ and V_P gradually decrese and reach their steady-state value. For the proposed device, the $J_{H\text{-path}}$ reduces to about zero at steady forward conduction state since the TMOS turns off after the V_P is lower than the absolute value of threshold voltage of the TMOS. However, for the HFP-TIGBT, the $J_{H\text{-path}}$ keeps at a higher current density since the hole path is normally on. These three devices have similar V_P at steady forward conduction state due to the similar V_{ceon}. During turn off process, when the V_{ge} reduces to miller plateau voltage, the V_{ce} starts to increase for the three devices, which makes the V_P increases accordingly. The change of the V_P as well as the $J_{H\text{-path}}$ shows similar trend as those in the turn on process. For the proposed STCP-TIGBT, when the V_P lager than the absolute value of threshold voltage of the TMOS, the hole extraction path turns on and $J_{H\text{-path}}$ starts to increase. The $J_{H\text{-path}}$ for the proposed device increases much faster than that of the HFP-TIGBT. For both the proposed STCP-TIGBT and HFP-TIGBT, the $J_{H\text{-path}}$ reaches the maximum value at the time when the V_P achieves the maximum value. The turn on of the TMOS extracts the excessive hole carrier in the drift region, which speeds up turn-off speed of the proposed device. According to the simulation results, the extracted threshold voltage of TMOS is −3.4 V with the current density of 1 mA/cm^2, and the current flow line distributions for the proposed STCP-TIGBT and HFP-TIGBT at different time points are shown in Figures 3(b) and (c), respectively. It can be seen that at $t = 152$ μs and 249 μs, there is no current flow line at the hole path region for the proposed device. While for the HFP-TIGBT, parts of the current flow line distributes at that region. At $t = 150.5$ μs and 251.5 μs, current flows via the hole path region for both the proposed STCP-TIGBT and HFP-TIGBT devices. It also can be seen that at $t =$ 251.5 μs, most of the current flows from the TMOS to the emitter for the proposed device.

Figure 4(a) shows comparison of the forward conduction I-V characteristics for the three TIGBTs. It can be seen that the proposed STCP-TIGBT has almost same forward conduction I-V characteristics as that of the CFP-TIGBT, which is better than that of the HFP-TIGBT. At the J_{ce} of 200 A/cm^2, the V_{ceon} of the proposed STCP-TIGBT, CFP-TIGBT and HFP-TIGBT are 1.06 V, 1.05 V and 1.10 V, respectively. The inserted figure in the Figure 4(a) shows the hole concentration distribution along the A-A′ line at J_{ce}=200 A/cm^2 for the three devices. It can be seen that the STCP-TIGBT and CFP-TIGBT have almost same hole concentration distribution. However, for the HFP-TIGBT, the hole concentration is much lower than those of the STCP-TIGBT and CFP-TIGBT, especially in the emitter side of the drift region.

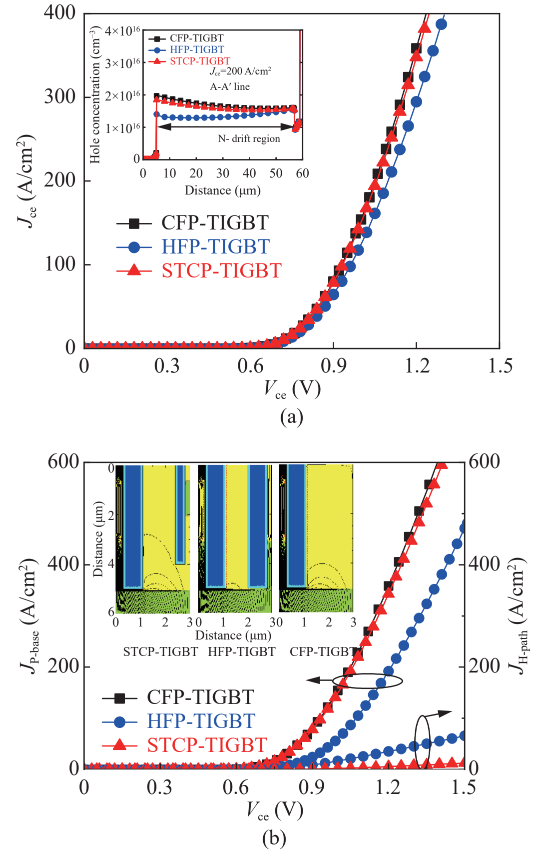


Figure 4 (a) Comparison of the forward conduction I-V characteristics for the three TIGBTs (the inserted figure shows hole concentration distribution along the A-A′ line for the three devices at J_{ce}= 200 A/cm^2, respectively); (b) Comparison of the $J_{P\text{-base}}$ and $J_{H\text{-path}}$ as a function of the V_{ce} for the proposed STCP-TIGBT and HFP-TIGBT (the inserted figure shows current flow line distributions at J_{ce}=200 A/cm^2 for the three devices, respectively).

Figure 4(b) shows comparison of the $J_{P\text{-base}}$ and $J_{H\text{-path}}$ as a function of the V_{ce} for the proposed STCP-TIGBT and HFP-TIGBT. The $J_{P\text{-base}}$, which is equal to J_{ce} for the CFP-TIGBT is also shown in the figure. It can be seen that the $J_{P\text{-base}}$ of the proposed STCP-TIGBT is almost same as that of the CFP-TIGBT since the TMOS is turned off in the forward conduction state and the highly-doped N-BL acts as hole barrier to prevent the hole flows from the N-drift region to the emitter. However, for the HFP-TIGBT, the $J_{H\text{-path}}$ is much larger than that of the proposed device, which impact the conductivity modulation effect in the N-drift region. The current flow line distributions at $J_{ce} = 200$ A/cm^2 for

these three devices are compared in the inserted figure in the Figure 4(b). It shows similar distributions as those shown in Figures 3(b) and (c) at $t = 152$ μs and 249 μs. It can be concluded that the TMOS has very subtle impact on the forward conduction I-V characteristics and current flow line distributions for the proposed device.

Figure 5 shows electric field distributions along A-A′ line for the three devices at breakdown, respectively. It can be seen that the peak electric field at the trench corner for the proposed STCP-TIGBT is suppressed and lower than those of the CFP-TIGBT and HFP-TIGBT. Therefore, the electric field distribution in the N-drift region for the proposed STCP-TIGBT is a little bit higher than those of the CFP-TIGBT and HFP-TIGBT. The better electric field distribution brings a relatively larger BV for the proposed device. The BV of the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT are respectively 729 V, 717 V and 716 V. Further investigation result shows that the larger BV for the proposed device is derived from better shielding effect provided by the P region, which is clamped to a fixed voltage after the TMOS is turned on.

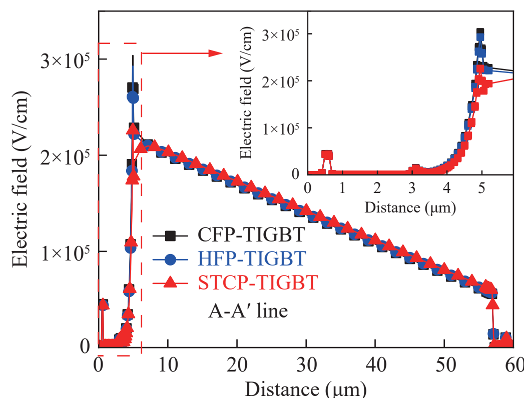


Figure 5 Electric field distributions along A-A′ line for the three devices at breakdown.

Figure 6 shows simulated gate charge (Q_g) characteristics for the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT, respectively. The inserted figure is the circuit used in the simulation. It is found that compared to the CFP-TIGBT and HFP-TIGBT, the miller plateau is much shorter for the proposed device. The Q_{gc} is reduced from 1208 nC/cm^2 of the CFP-TIGBT and 681 nC/cm^2 of the HFP-TIGBT to 501 nC/cm^2 of the proposed STCP-TIGBT. Compared with the CFP-TIGBT and HFP-TIGBT, the Q_{gc} for the proposed device is reduced by 58.5% and 26.4%, respectively. It also can be seen that with the V_{ge} increases from 0 V to 15 V, the total Q_g is 1880 nC/cm^2, 1943 nC/cm^2 and 2275 nC/cm^2 for the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT, respectively. Compared to the CFP-TIGBT and HFP-TIGBT, the total Q_g for the proposed device is reduced by 17.4% and 3.2%, respectively.

Figure 7 shows turn-on characteristics of the three TIGBTs with different R_g at the J_{ce} of 20 A/cm^2 (0.1 of

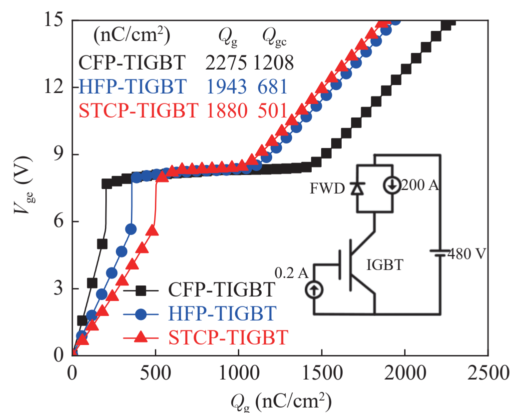


Figure 6 Simulated gate charge characteristics for the proposed STCP-TIGBT, HFP-TIGBT and CFP-TIGBT (The inserted figure is the circuit used in simulation).

the rated J_{ce} of 200 A/cm^2), respectively. It can be seen that with the increase of R_g, the dV_{ce}/dt and current overshoot for the three devices are all decreased. Compared to the CFP-TIGBT and HFP-TIGBT, the current overshoot is much sensitive to the R_g for the proposed device. When the R_g is changed from 10 Ω to 100 Ω, the maximum current overshoot (I_{peak}) for the CFP-IGBT and HFP-TIGBT is only reduced by 41.1% and 53.6%, respectively. While, the I_{peak} is reduced by 60.4% for the proposed STCP-TIGBT at the same condition. The trade-off relationship between the E_{on} of the IGBT at J_{ce}=200 A/cm^2 and reverse recovery dV_{ak}/dt of the FWD at J_{ce}=20 A/cm^2 for the three devices are shown in Figure 8, respectively. The curves are obtained with changing of the R_g. It can be found that compared to the CFP-TIGBT and HFP-TIGBT, the proposed STCP-TIGBT demonstrates much better E_{on}-dV_{ak}/dt trade-off relationship. At same E_{on} of 31.8 mJ/cm^2, the reverse recovery dV_{ak}/dt of the FWD is reduced from 24.69 kV/μs and 5.02 kV/μs for the CFP-TIGBT and HFP-TIGBT to 2.15 kV/μs for the proposed STCP-TIGBT. Compared with the CFP-TIGBT and HFP-TIGBT, the reverse recovery dV_{ak}/dt of the FWD for the proposed STCP-TIGBT is reduced by 91.3% and 57.2%, respectively. The result is consistent with the result of V_P and I_{peak} for the three TIGBTs in the Figure 3 and Figure 7, respectively. The lower reverse recovery dV_{ak}/dt of the FWD significantly reduces the EMI noise for the proposed STCP-TIGBT.

Figure 9 shows comparison of the trade-off relationship between the V_{ceon} and E_{off} for the three structures under inductive load condition. The simulation result is obtained by changing the P collector doping concentration (P_c) of the devices. It can be seen that the V_{ceon}-E_{off} trade-off relationship for the HFP-TIGBT is even worse than that of CFP-IGBT. For the proposed STCP-IGBT, it demonstrates the best V_{ceon}-E_{off} trade-off relationship among these three devices. At same V_{ceon} of 1.02 V, the E_{off} is reduced from 38.12 mJ/cm^2 of the CFP-IGBT and 41.59 mJ/cm^2 of the HFP-IGBT to 13.49 mJ/cm^2 of the

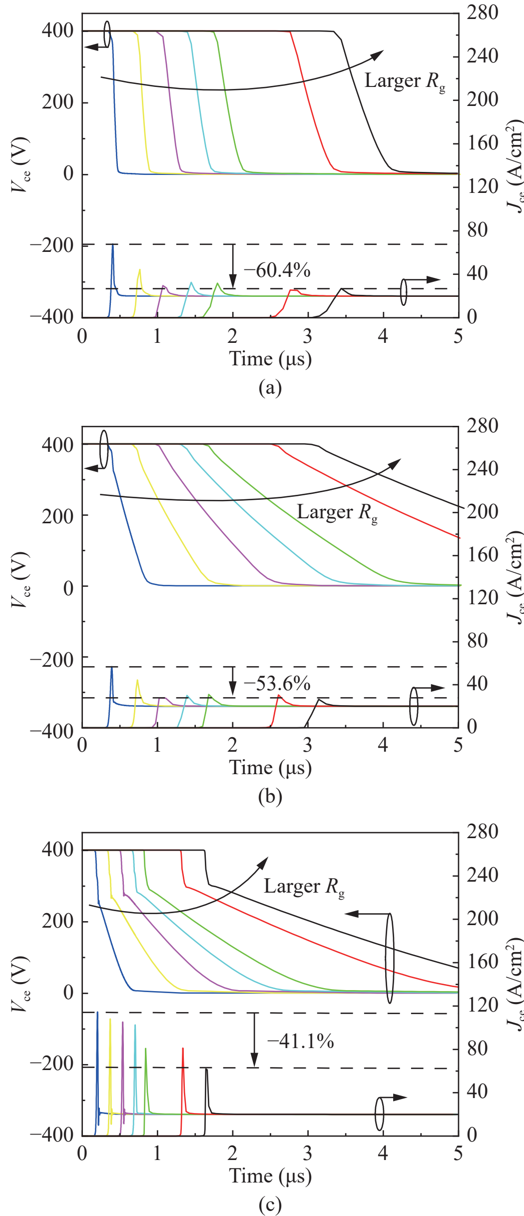


Figure 7 Turn-on characteristics of the three TIGBTs with different R_g at the J_{ce} of 20 A/cm^2 (0.1 of the rated J_{ce} of 200 A/cm^2). (a) Proposed STCP-TIGBT; (b) HFP-TIGBT; (c) CFP-TIGBT (From left to right, the R_g is 10, 20, 30, 40, 50, 80 and 100 Ω, respectively).

proposed STCP-IGBT. Compared with the CFP-IGBT and HFP-IGBT, the E_{off} for the proposed device is decreased by 64.6% and 67.6%, respectively. The inserted figure in Figure 9 shows the hole concentration distribution along the A-A′ line at V_{ceon}=1.02 V for the three devices. The P_c used is 2 × 10^{17} cm^{-3}, 4.5 × 10^{17} cm^{-3} and 2.2 × 10^{17} cm^{-3} for the CFP-IGBT, HFP-IGBT and proposed STCP-IGBT, respectively. Much higher P_c has to be used for the HFP-IGBT to obtain same V_{ceon}. It can be found that the proposed STCP-IGBT keeps almost same carrier concentration distribution with the CFP-IGBT. However, for the HFP-IGBT at same V_{ceon}, it has much worse carrier concentration distribution due to the

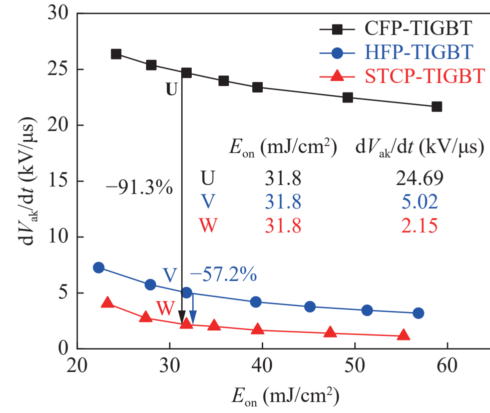


Figure 8 Simulated trade-off relationship between the E_{on} of the IGBT at J_{ce}=200 A/cm^2 and reverse recovery dV_{ak}/dt of the FWD at J_{ce}=20 A/cm^2 for the three devices.

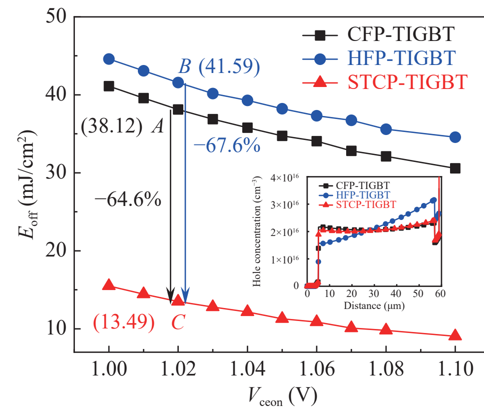
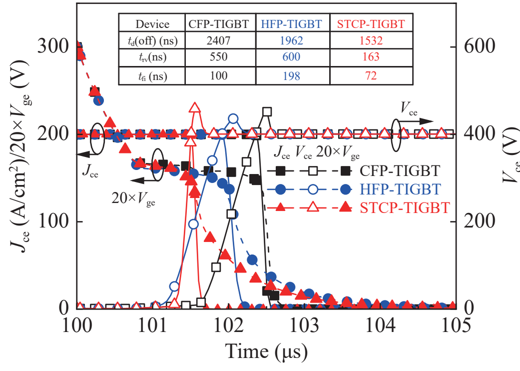


Figure 9 Comparison of the trade-off relationship between the V_{ceon} and E_{off} for the three devices.

hole extraction in the on-state via the normally on hole path.

Figure 10 and Figure 11 show simulated turn-off current and voltage waveforms as well as dissipated power density over time during turn-off process for the point A, B and C shown in the Figure 9, respectively. The gate signal starts to turn off from 15 V to 0 V at t = 100 μs. The power loss contributed by the collector voltage rising period and collector current falling period is marked as $E_{v,\text{off}}$ and $E_{i,\text{off}}$, respectively. It can be seen that the proposed STCP-IGBT demonstrates fastest turn-off speed both in the collector voltage rising period and collector current falling period among these three TIGBTs. The rise time (t_{rv}) for the collector voltage rises from 10% to 90% of the bus voltage and fall time (t_{fi}) for the collector current falls from 90% to 10% of the J_{ce} are only 163 ns and 72 ns for the proposed STCP-IGBT, respectively. However, t_{rv} and t_{fi} are 550 ns/100 ns and 600 ns/198 ns for CFP-IGBT and HFP-IGBT, respectively. The turn-off delay time ($t_{d(\text{off})}$) from the gate signal starts to turn off to the collector current falls to 90% of the J_{ce} is 2407 ns, 1962 ns and 1532 ns for the CFP-IGBT, HFP-IGBT and proposed STCP-IGBT, respectively. As a result, the proposed STCP-IGBT shows both lowest $E_{v,\text{off}}$ and $E_{i,\text{off}}$ among these three structures.



Device	CFP-TIGBT	HFP-TIGBT	STCP-TIGBT
t_d(off) (ns)	2407	1962	1532
t_{rv}(ns)	550	600	163
t_{fi} (ns)	100	198	72

Figure 10 Simulated turn-off current and voltage waveforms for the point A, B and C shown in the Figure 9.

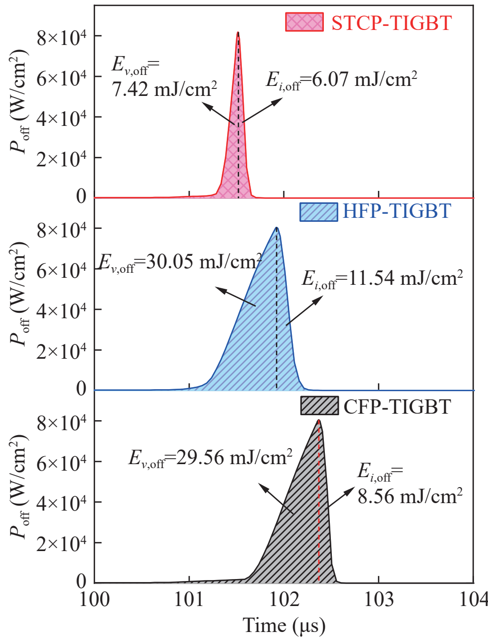
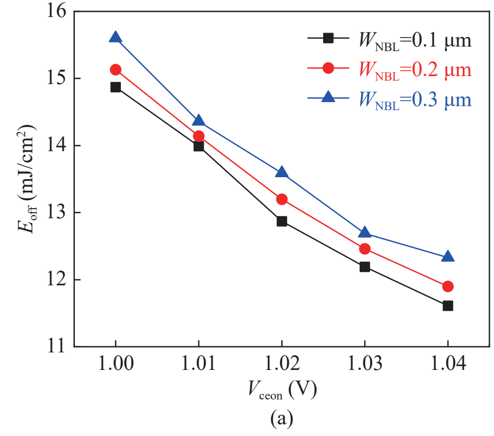


Figure 11 Dissipated power density over time during turn-off process for the point A, B and C shown in the Figure 9.

The impact of the N-BL width (W_{NBL}) on the V_{ceon}-E_{off} trade-off relationship for the proposed STCP-TIGBT is shown in Figure 12(a). It can be found that as the W_{NBL} decreases from 0.3 μm to 0.1 μm, the trade-off relationship between V_{ceon} and E_{off} is slightly improved. Further investigation results show that with the W_{NBL} decreases, the number of holes cross the barrier formed by the N-BL is slightly reduced. Therefore, a slightly enhanced conductivity modulation happens in the N-drift region and then an optimized on-state carrier distribution is obtained, which reduces the V_{ceon} and improves the V_{ceon}-E_{off} trade-off relation-ship for the proposed STCP-TIGBT. The impact of the emitter trench depth (D_{ET}) on the V_{ceon}-E_{off} trade-off relationship for the STCP-TIGBT is also shown in the Figure 12 (b). It can be seen that the D_{ET} has little influence on the V_{ceon}-E_{off} trade-off relationship for the STCP-TIGBT. This is because that the emitter trench is fully encapsulated and shielded by the P-type dummy region. Therefore, it has



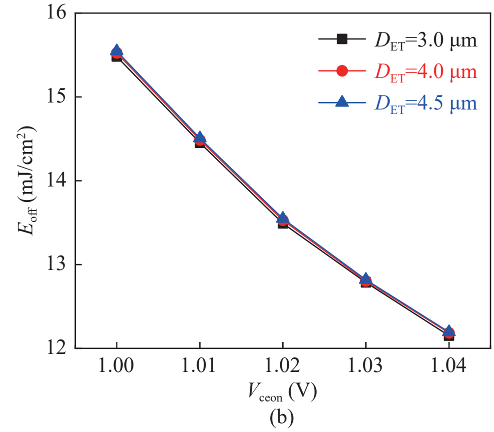


Figure 12 Impact of (a)W_{NBL} and (b)D_{ET} on the V_{ceon}–E_{off} trade-off relationship for the proposed STCP-TIGBT.

little impact on the V_{ceon} and E_{off} characteristics.

Figures 13(a)–(h) show the proposed brief fabrication process flow for the STCP-TIGBT. The overall process flow is similar and fully compatible with that of the CFP-TIGBT. Compared to the CFP-TIGBT, only an additional process step of high-energy N-type ion implant is needed to form the highly-doped N-BL, which is shown in the Figure 13(f). Thermal annealing of the N-BL can share the annealing process used for the N+ and P+ region. Considering the wider trench has faster etching rate than the narrow one, named as the load effect of etching process, deep gate trench and shallow emitter trench can be obtained in a single etching step. And then oxide layer is formed by thermal oxidation and poly-silicon electrode are deposited at the same time for the gate and emitter trenches. Therefore, for the emitter trench as well as the P+ layer above the N-BL, both can be formed simultaneously with the gate trench and the P+ emitter, respectively. The process steps are shown in the Figures 13(b), (c) and (g), respectively.

IV. Conclusion

A novel high performance STCP-TIGBT is proposed and analyzed in detail in this paper. The proposed STCP structure not only speeds up the extraction of excessive holes in the turn-off process but also reduces the Q_{gc} at

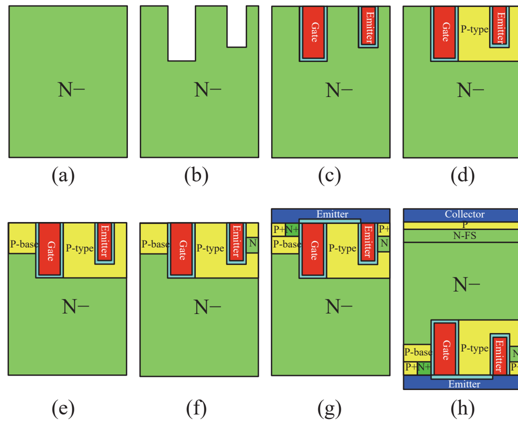


Figure 13 Proposed brief fabrication process flow for the STCP-TIGBT. (a) Selecting lightly-doped N-type float-zone (FZ) wafer as starting material; (b) Dry etching to form gate and shallow emitter trench; (c) Thermal oxidation to form oxide layer and then depositing poly-silicon electrode; (d) Ion implant and thermal annealing to form P-type region; (e) Ion implanting and thermal annealing to form P-base region; (f) High-energy ion implant to form highly-doped N-BL; (g) Process steps to form N+ and P+ region and emitter electrode; (h) Backside substrate thinning and process steps to form N-FS, P-collector region and collector electrode.

negligible cost of the V_{ceon} for the proposed device. Simulation results show that the Q_{gc} of the proposed STCP-TIGBT is only 501 nC/cm^2, which is 51.6% and 38.6% lower than that of the CFP-TIGBT and HFP-TIGBT, respectively. At same V_{ceon} of 1.02 V, the E_{off} of the proposed STCP-TIGBT is 13.49 mJ/cm^2, which is 64.6% and 67.6% less than those of the CFP-TIGBT and HFP-TIGBT, respectively. Moreover, at the same E_{on} of 31.8 mJ/cm^2, the reverse recovery dV_{ak}/dt of the FWD for the proposed STCP-TIGBT is only 2.15 kV/μs, which is reduced by 91.3% and 57.2% when compared with 24.69 kV/μs and 5.02 kV/μs for the CFP-TIGBT and HFP-TIGBT, respectively. Therefore, both V_{ceon}-E_{off} and E_{on}-dV_{ak}/dt trade-off relationship are improved for the proposed device. The lower reverse recovery dV_{ak}/dt of the FWD significantly reduces the EMI noise for the proposed STCP-TIGBT.

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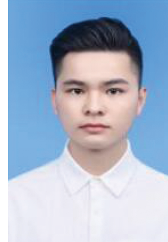

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