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RESEARCH ARTICLE

A Multi-Channel CMOS Analog Front-End Interface IC with 157.8 dB Current Detection Dynamic Range

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Abstract — A high dynamic range and low-noise CMOS (complementary metal-oxide-semiconductor transistor) front-end interface integrated circuit (IC) with multi-channel detection is presented in this paper. Two different current detection channels, composed of a trans-impedance amplifier (TIA) and an integrator-differentiator TIA, are used to boost the current detection range. A capacitance-coupled instrument amplifier (CCIA) is also included to realize high precision voltage detection. A fourth-order sigma-delta modulator using a second-order loop filter and a second-order noise shaping integral quantizer is adopted to realize effective number of bits above 16 bits. The presented interface IC is implemented in 0.18-μm CMOS process with supply voltage of 3.3 V, and a proto-type electrochemical sensor platform with miniaturized sensor array is developed to verify the functionality of the interface IC. Measurement results indicate that the designed interface IC achieves 157.8 dB current detection dynamic range, and the measured input-referred current noise and voltage noise floor are 1.04 pA and 58.4 nV within 10 kHz integration bandwidths, respectively.

Keywords — Readout integrated circuit, Sigma-delta modulator, Complementary metal-oxide-semiconductor transistor, Current detection dynamic range.

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I. Introduction

In the field of environmental monitoring, rapid and real-time acquisition of all kinds of pollution variables is always necessary. For example, in a water quality monitoring system, temperature, pH value, heavy metal ion concentration and non-metal ion concentration are all needed to be monitored by different sensors, the output signal of these sensors are different from each other. For electrochemical sensors, the output current ranges from ±10 pA to ±1 mA, while for pH sensors, the output voltage ranges from ±1 mV to ±1 V [1]. Moreover, heavy metal ions are usually tested by the potentiostat method, a programmable waveform generator is usually needed. Some printed circuit-board level monitoring system has been developed [2], however, many peripheral devices are needed in these systems, and this makes these systems complicated and highly cost. Integration of multi-sensor CMOS (complementary metal-oxide-semiconductor transistor) analog front-end (AFE) chips has become the main solution for multi-variable real-time monitoring. Recently, such CMOS AFE interface integrated circuits (ICs) have been reported [3]–[12]. However, these interface ICs are designed for specific sensors and their dynamic detection range is limited, which makes them inappropriate for various signal measurements, such as water monitoring. Amperometric readout circuit with 140 dB detec-

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tion range was implemented in [13], [14], while it does not have programmable bias voltage generator for potentiostat sensors. In [15], a three-electrode AFE chip with a current detection dynamic range of 120 dB is proposed, it can basically meet the detection of heavy metal ions in liquid. However, the chip cannot convert multiple input types of signals, and the system linearity is low, which makes it difficult to apply to a comprehensive water quality inspection system. Hence, new AFE interface circuits with wide input range of all kinds of signals and necessary bias voltages are needed. In order to meet the requirements of single AFE chip docking of various types of sensors, it is necessary to design a chip that can process multiple types of input signals and has large dynamic range. In this paper, to meet the requirements of connecting with various water quality monitoring sensors, it is necessary to realize the ability to process voltage and current signals, and the dynamic range of voltage signal monitoring above 60 dB and the dynamic range of current signal monitoring above 150 dB. A multi-channel CMOS AFE interface IC with 157.8 dB current detection dynamic range and 60 dB voltage detection dynamic range is proposed in this paper. An integrator cascade differentiator TIA (trans-impedance amplifier) structure is adopted to improve the current detection precision to 10 pA. A capacitance coupled instrumentation amplifier is also embedded to monitor small differential voltage signal and calibrate the offset of PGA (programmable gain amplifier). Moreover, low noise amplifiers, correlated double sample (CDS) and chopping techniques are also used to obtain high precision detection.

II. System Architecture

The block diagram of the system is shown in Figure 1. It includes two current detection channels with input IIN1 and IIN2, a single-ended voltage detection channel with input VIN, and a differential voltage detection channel with input VAP and VAN. One current channel is composed of integrator cascade with differentiator (I-D), and it is used to detect current from 10 pA to 1 μA. The other current channel is composed of a traditional TIA and it is used to detect current from 1 μA to 1 mA. The switch between two channels is controlled by a feedback loop composed of PGA, ADC (analog to digital converter), data processing module, and I^2C bus. When the data processing module detects the current corresponding to the ADC output code value detected is greater than 100 nA at I-D TIA detecting channel, it will send a channel switching signal to the chip through the I^2C bus changing the current detecting channel to TIA channel. When the detection channel is TIA channel, the working state is opposite. Single voltage signal VIN is converted to current first through V to I circuit, and then is sent to either I-D TIA or TIA depend on its amplitude. V to I module is composed of resistors, and the resistance value is controlled by the digital circuit. According to the feedback information of the quantized value, the appropriate resistance value is used to convert the input voltage. The small differential voltage signal is processed by capacitive-coupled instrumentation amplifier (CCIA). After I-D TIA, TIA and CCIA, a PGA is followed. The PGA is used to amplifier the converted signal of all channels and changes the single-ended signal to differential signal. Then a 16 bit ΣΔ ADC is used to convert the analog signal to digital code, and the digital code is output through SPI bus. All voltage references (VRES), which includes the common mode voltage (VCM), high voltage reference (VH), and low voltage reference (VL), is provided by a bandgap (BG) and then using a buffer to increase the drive capability of VRES. Digital circuit generates all the clocks and the control signals, and I^2C bus is used to configure the internal registers of the digital circuit. A 10 bit DAC is also included to generate static voltage and dynamic

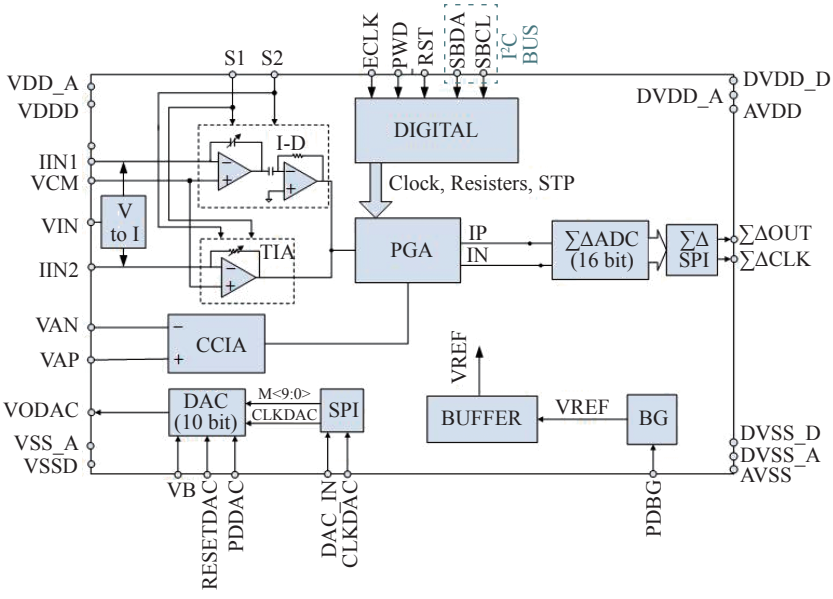

Figure 1 Graphical representation of the concept lattice.

sweeping voltage used for heavy metal sensors. Low dropout regulator (LDO) provides power for digital circuit. In order to reduce power consumption, each module of the chip uses an independent power down signal, so that when only few modules are used, the other modules can be closed.

III. Circuit Implementation

In order to achieve a very high dynamic range of current detection and a higher dynamic range of voltage detection, both the current detection channel and the voltage detection channel adopt a unique structure. In addition, a new type of ADC with high dynamic range and low power consumption is proposed in this article. These three circuits will be described in detail below.

1. Current detection channel

I-D TIA and TIA are the first part of current detection channels. They work alternatively, according to the input current. In order to improve the accuracy of low current measurements, a differentiator is cascaded after the current integrator, as shown in Figure 2(a). The first stage integrator consists of an operational amplifier and an integrating capacitor. The second stage differentiator is consisted of an operational amplifier, and a capacitor-resistor path. The input current is converted into a ramp wave after passing through the I-D TIA channel. The ramp wave is then converted to a DC voltage decided by the slope of the ramp wave after passing through the differentiator. Due to the high-pass filtering of the differentiator, the noise will be much smaller than the traditional integrator structure.

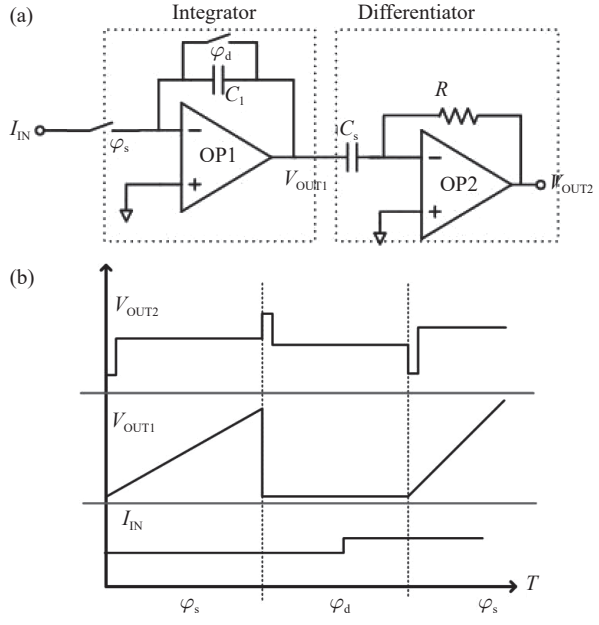

Figure 2 (a) The circuit diagram of the I-D TIA; (b) Output voltage of integrator and differentiator.

At φ_d phase, the integrator is reset to the initial state. At φ_s phase, the integrator integrates the input current shown in Figure 2 (b). The output of the integrator can be calculated by the following formula:

$$V_{OUT1} = \frac{I_{IN} \cdot T}{C_I} \tag{1}$$

where T represents the integrating time, which is φ_s, 50 μs in this design, C_I represents the integrating capacitor. The pulse signal in the output signal of the differentiator is the error that occurs when the integral voltage has an inflection point. Since the output signal of the differentiator at the end of the two phases is sampled by the subsequent circuit, the error pulse at the beginning of the phase will not affect the accuracy of the circuit. The output of the differentiator can be expressed as

$$V_{OUT2} = RC_s \cdot \frac{dV_{OUT1}}{dt} = RC_s \cdot \frac{I_{IN}}{C_I} \tag{2}$$

The overall current to voltage gain is C_sR/C_I. In this paper, R is set to 400 kΩ, the capacitors C_s and C_I are chosen to be 120 pF and 20 pF, respectively, thus the transimpedance gain of this current input channel is 63.8 dBΩ.

In order to achieve the current detection accuracy of 10 pA, the input equivalent current noise must be less than 10 pA. The main noise source is composed of four parts: input current noise, resistance noise on the differentiator, first-stage operational amplifier noise, and second-stage operational amplifier noise. The output noise of the integrator is given by

$$v^2_{ITGR,OUT} = v^2_{fn,OP1} + \frac{KT}{C_s} \tag{3}$$

where $v^2_{ITGR,OUT}$ represents the output mean-square noise voltage of the integrator, A represents the gain of the amplifier, $v^2_{fn,OP1}$ represents the flicker noise of the first operational amplifier. KT/C_s represents the thermal noise sampled by capacitor C_s. The input equivalent noise can be derived as

$$i^2_{ITGR,IN} = \left(v^2_{fn,OP1} + \frac{KT}{C_s}\right) \Big/ \left(\frac{T_{time}}{C_I}\right)^2 \tag{4}$$

To calculate the noise spectral characteristics, we need to Fourier transform the differentiator. After Fourier transform, the transfer function of the differentiator can be expressed as

$$H(\omega) = \omega C_s R \tag{5}$$

According to (3), the output mean-square noise voltage of the differentiator is given by

$$v^2_{n,OUT} = \omega^2 C_s^2 R^2 \cdot \left(v^2_{fn,OP1} + \frac{KT}{C_s}\right) + 4kTR + v^2_{n,OP2} \tag{6}$$

In this equation, $4kTR$ and $v^2_{n,OP2}$ are the noise generated by resistor and operational amplifier (OPAMP) 2

(OP2 in Figure 2). All the thermal noise from resistors will from the next level KT/C noise, which cannot be changed. When calculating the input equivalent noise, the second-order noise will be suppressed by the channel gain so that it is much smaller than the first-order noise and can be ignored. Since ω equals to $2\pi f$ which is proportional to frequency, the flicker noise of integrator and KT/C noise are canceled after multiplied by ω^2. Hence, the input equivalent noise can be derived as

$$i_{n,\mathrm{IN}}^2 = \frac{\omega^2 C_\mathrm{s}^2 R^2 \times \left(v_{\mathrm{fn,OP1}}^2 + \dfrac{KT}{C_\mathrm{s}}\right) + 4kTR + v_{\mathrm{n,OP2}}^2}{\left(\dfrac{C_\mathrm{s}R}{C_\mathrm{I}}\right)^2} \quad (7)$$

The differentiator not only cancels the low frequency noise of the integrator, but also brings much higher gain to suppress the second stage noise. Compare formula (4) with (7), the total input equivalent noise of the I-D TIA is lower than the integrator.

TIA circuit diagram is shown in Figure 3. The gain of TIA can be expressed by

$$V_{\mathrm{OUT3}} = -I_{\mathrm{IN}} \cdot R_\mathrm{f} \quad (8)$$

To cover the current detect range from 1 μA to 1 mA, the resistor R_f has 8 gears, which can be changed from 1 MΩ to 6.25 kΩ. To reduce quiescent current, an amplifier with class-AB output stage is used in OP3.

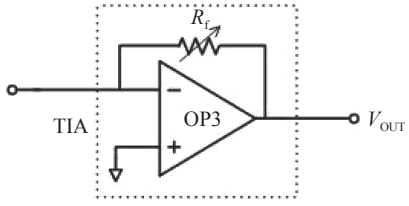

Figure 3 The circuit diagram of TIA.

2. Capacitive-coupled instrumentation amplifier

A CCIA [16]–[21] is used to detect the differential input voltage. Figure 4 shows the circuit diagram of the capacitive-coupled wideband chopper current-feedback instrumentation amplifier [22]. It comprises a main amplification stage, a chopper stage, a low noise ripple reduction loop (RRL) [23], a DC-servo loop (DSL) [24], positive feedback loop (PFL) [25], and a voltage sum capacitor feeding network. The input signal is chopped to reduce offset voltage and $1/f$ noise. The main amplification stage is based on a two-stage Miller-compensated OPAMP, which consists of an input transconductance GM1 and an integrator built around GM2, the closed-loop gain is set by feedback capacitance C_{fb} and input capacitance C_{in}:

$$\mathrm{Gain} = \frac{C_{\mathrm{fb}}}{C_{\mathrm{in}}} \quad (9)$$

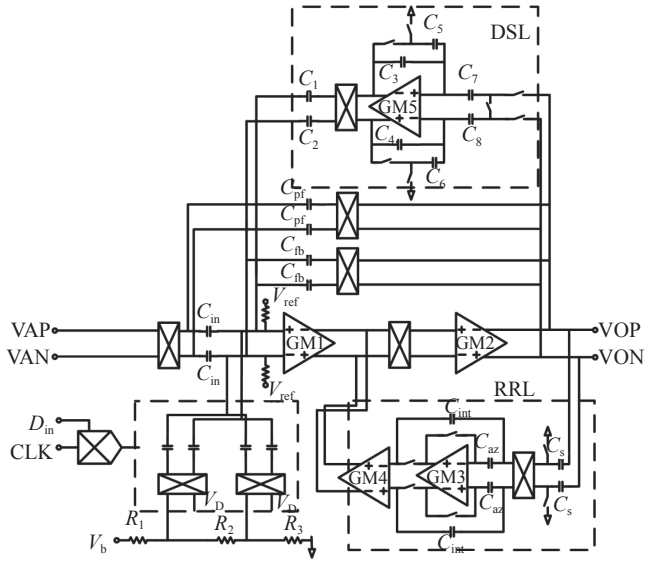

Figure 4 The circuit diagram of CCIA.

The PFL comprising feedback capacitance C_{pf} and input capacitance C_{in} increases the input impedance. If C_{pf} equals to C_{fb}, the input impedance is

$$Z_{\mathrm{in\_pf}} = \frac{G}{2 \cdot f_{\mathrm{chop}} C_{\mathrm{in}}} \quad (10)$$

where $Z_{\mathrm{in\_pf}}$ is the input impedance of the positive feedback path, G is the gain of the CCIA, f_{chop} is the chopping frequency. The RRL loop integrate voltage ripple caused by chopping and feedback between GM1 and GM2 to cancel the impact of voltage ripple. The ripple voltage at V_{out} is sensed by C_s, demodulated by chopper, and integrated by GM3 to generate voltage singal via C_{int}. The DC signal is then converted to current by transconductance GM4 to compensate for the offset of GM1. The output ripple after compensating is given by [19]

$$V_{\mathrm{out,ripple}} = V_{\mathrm{OS1}} \times \frac{1}{G_{\mathrm{M3}} G_{\mathrm{M4}} C_{\mathrm{L1}}} \times G_{\mathrm{M1}} G_{\mathrm{M2}} \times \frac{1}{2\pi f_{\mathrm{chop}}} \quad (11)$$

V_{OS1} represents the offset voltage of GM1. $V_{\mathrm{out,ripple}}$ is independent of C_s. A reduced $V_{\mathrm{out,ripple}}$ can be achieved by increasing either GM3 or GM4.

The DSL is used to eliminate the large DC offset that may arise from electrochemical processes at the electrode-tissue interface. It integrates the DC voltage signal at V_{out} through a switch-capacitor integrator, then the generated signal is up modulated by chopper, and is fed back to the input of GM1. The transfer function of the integrator is given by

$$H(z) = \frac{C_{7,8}}{C_{5,6} + C_{3,4} - C_{3,4} z^{-1}} \quad (12)$$

The combination of capacitor $C_{7,8}$ and switch can be regarded as equivalent resistance. Because capacitor $C_{5,6}$ is embedded in the loop, the bandwidth of the integra-

tor in DSL is different from normal integrator. The optimized bandwidth is given by

$$f_0 = \frac{f_s C_{5,6}^2}{2\pi C_{3,4}^2} \tag{13}$$

where f_s is the operating frequency. By choosing the value of $C_{3,4}$ and $C_{5,6}$ at 1250Cu and Cu (Cu is the unit capacitor about 100 fF composed by CMOS), f_0 can be set to 0.01 Hz, which will make the integrator has a fast time domain response toward the DC offset voltage signal.

Moreover, a coarse DC offset compensation composed of a 3-bit DAC is also used to accelerate the total compensation speed. Through changing the control D_{in}, the circuit can obtain a compensation voltage from VL to 8VL, where VL is 10 mV.

3. Programmable gain amplifier

The PGA stage shown in Figure 5 converts the single input voltage or differential voltage into differential output voltage and provides amplification. The offset voltage of the amplifier is stored at the top plate of CC during φ_1 equals high, and it will be canceled at φ_2 becoming high. When it is single input mode, the input voltage is connected to V_{IN}, and common mode voltage VCM is connected to V_{IP}. The output voltage of PGA is

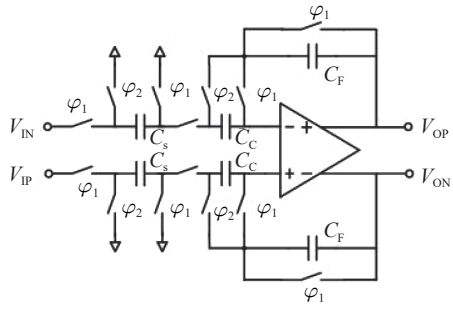

Figure 5 The circuit diagram of PGA.

$$V_{OUT} = \frac{C_F}{C_s} V_{IN} \tag{14}$$

V_{IN} is the input voltage. When it is single input mode, V_{IN} equals to (VIN-VCM).

4. Sigma-delta modulator

A fourth order ΣΔ modulator composed of a traditional second order ΣΔ modulator and a second order noise-shaped integrating quantizer (NSIQ) [26]–[28] is presented in this paper, the proposed modulator architecture is shown in Figure 6. With the aid of the digital integration in the loop [29], the NSIQ provides effective 5-bit quantization levels and two extra orders of noise-shaping using only four counting clock edges.

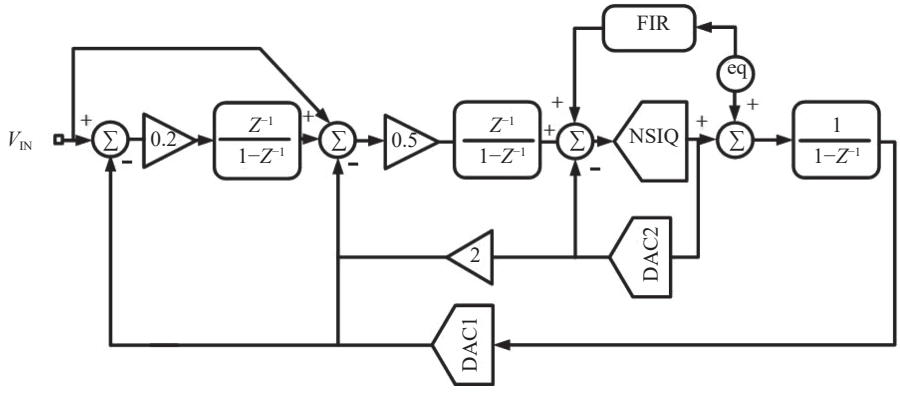

Figure 6 Proposed modulator architecture.

In this paper, the modulator adopts the structure of [28], and the main circuit is divided into three parts, the feedforward integration path, the second-order NSIQ quantizer and the back-end digital integrator.

The feed-forward integration path ensures an overall two-stage noise shaping capability. The second-order NSIQ quantizer provides additional second-order shaping capability. The back end integrator ensures the stability of the circuit. The overall transfer function of the proposed structure is derived as

$$D(z) = X(z) + (1 - z^{-1})^4 \mathrm{EQ}(z) \tag{15}$$

where $D(z)$ represents the z transform of the output digital code, $X(z)$ represents the input signal, $\mathrm{EQ}(z)$ represents the quantization noise.

IV. Results

The analog front-end circuit was fabricated in a 0.18 μm CMOS process, the chip size is 3.2 mm × 2 mm, and the photograph of the whole chip is shown in Figure 7. The measured power consumption is 16.5 mW @3.3 V.

1. Single module test result

The measured output voltage noise spectrum of the I-D TIA channel is shown in Figure 8. During the channel noise test, all circuits except the test channel are turned off. The input of the test channel is connected to the DC common mode voltage VCM, and its noise spectrum characteristics are tested by a spectrum analyzer. After integrating the noise power density, the output noise is 30.9 μV_{RMS} at 10 kHz bandwidth. The gain of

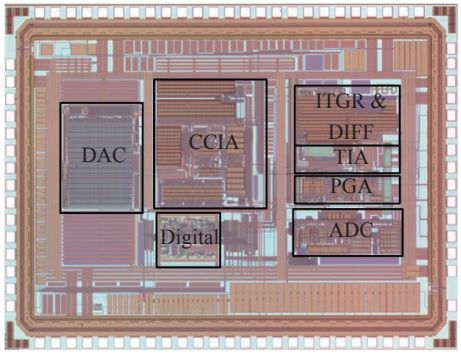

Figure 7 Die microphotograph of the fabricated analog front-end chip.

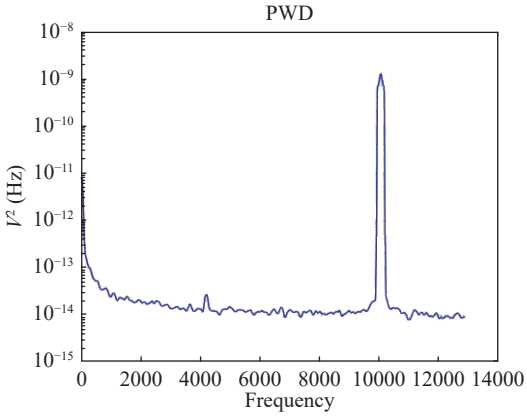

Figure 8 The spectrum map of the output voltage noise of I-D TIA channel.

this channel is 2.4 MΩ, thus the input referred current noise floor is 12.88 pA_{RMS} at 10 kHz.

The output noise of CCIA voltage spectrum measured by dynamic signal analyzer is shown in Figure 9. After integrating the noise power density, the output noise is 1.35 mV_{RMS} at 10 kHz bandwidth. The amplifier configures for a closed loop gain of 40. Accordingly, the input-referred noise is 33.7 μV_{RMS}.

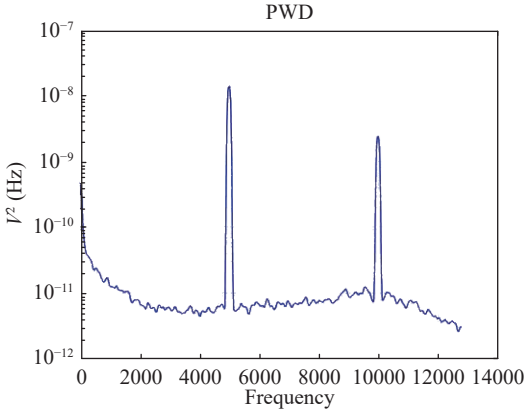

Figure 9 Measured input referred noise of the proposed CCIA.

Figure 10 plots the measured spectrum of the sigma-delta modulator output with a 1 kHz input sinewave at an OSR of 50, fourth order of noise shaping ability can be seen in the figure. In a 10 kHz BW, the proposed

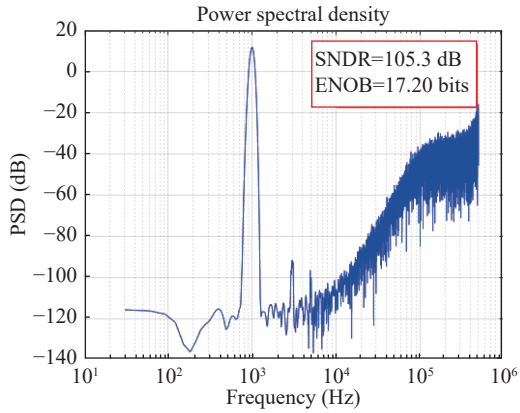

Figure 10 The spectrum map of the proposed DSM at 1kHz signal input.

DSM achieves a signal to noise and distortion ratio (SNDR) of 105.3 dB, corresponding to 17.2 bits effective number of bits (ENOB).

2. Current and voltage channel test result

A low noise current source is used to test the current channel. When the input current is less than 1 μA, it is measured by the I-D TIA channel. The measured output digital data versus input current is shown in Figure 11. For current above 1 μA, it is measured by the TIA channel. Figure 12 shows the measured result of 100 μA to 1 mA input signal. All figures show that the current test path of the AFE chip has high linearity at one range setting, and the smallest R^2 are 0.9999 and 1 for I-D TIA channel and TIA channel, respectively.

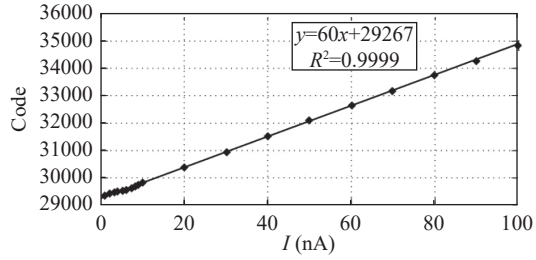

Figure 11 Measured output digital data versus input current (I-T TIA).

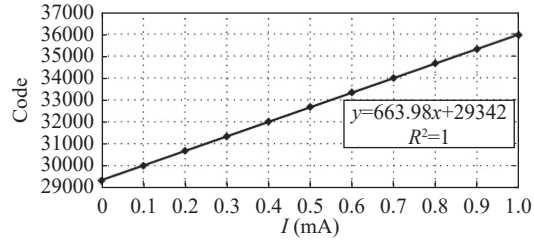

Figure 12 Measured output digital data versus input current (TIA).

The input signal of voltage testing is generated by a high-precision voltage source. The voltage signal is converted into a current signal by the on chip V2I module, before sending to the TIA. When voltage varies from 100 mV to 1 V, the measured result is shown in Figure 13,

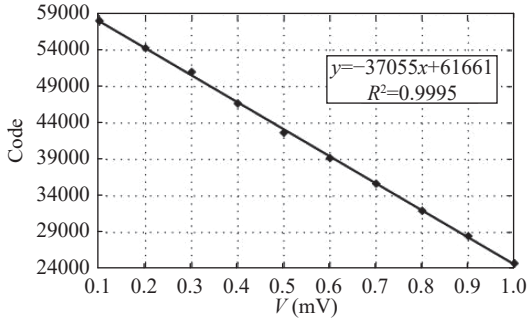

Figure 13 Measured output data versus single-ended input voltage.

the smallest R^2 is 0.9995. While the differential voltage signal is test by CCIA channel, the measured result with the voltage varying from 1 mV to 6 mV is shown in Figure 14, and the smallest R^2 is 0.9982.

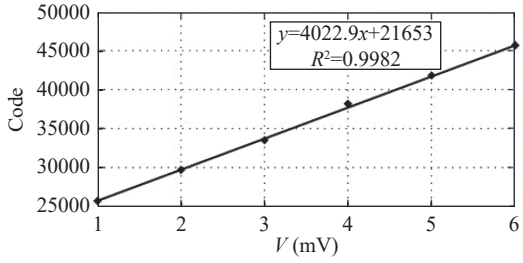

Figure 14 Measured output data versus input differential voltage.

The test results of the dynamic characteristics of the current path are shown in Figure 15. Under the condition of 100 nApp 259 Hz sinusoidal signal current input, the SNDR of the whole channel reaches 43.3 dB.

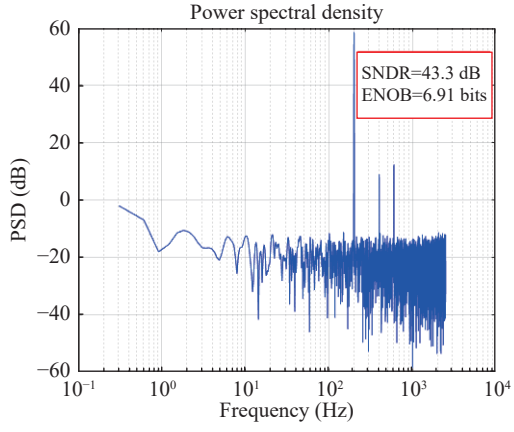

Figure 15 The spectrum map of current path under 100 nApp input.

3. Prototype electrochemical sensor platform

Figure 16 is the test platform for this system. The electrode materials are gold electrode, platinum electrode and AgCl electrode. Using KCN solution, the curve of current changing with scanning speed is shown in Figure 17(a), the linear relationship of the peak current with the scanning speed is shown in Figure 17(b), it can be seen that the linearity is 99.27%. Figure 18 reveals the scanning voltage program of Hg^{2+}, the I-V curves tested by chip and instrument are basically match.

The pH sensor test results with pH values of 1.13, 4, 6.86, 9.18, and 11.5 are shown in Figure 19, the maximum deviation between the measured value and the ac-

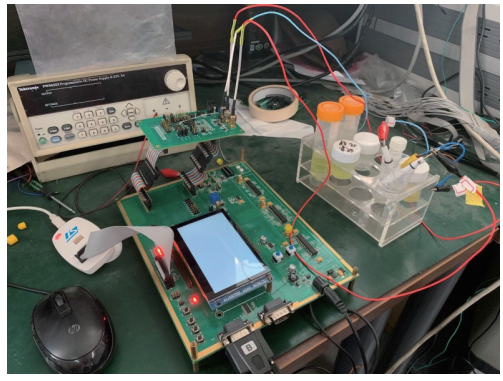

Figure 16 Test platform environment.

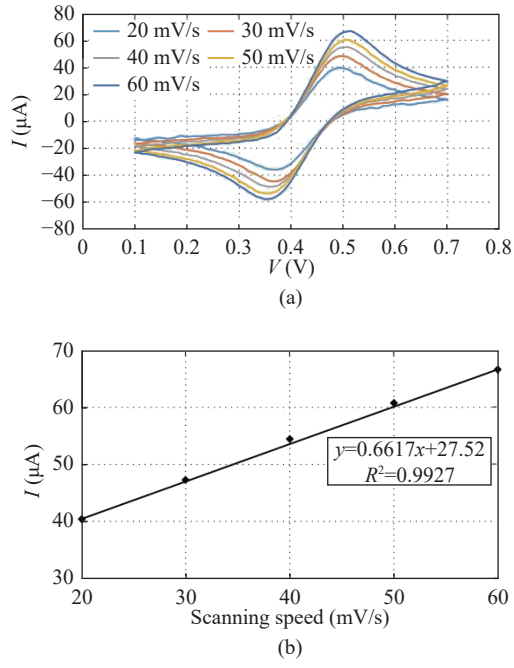

Figure 17 (a) Measured sweep *I-V* characteristic curve of KCN; (b) The peak current versus the scan speed.

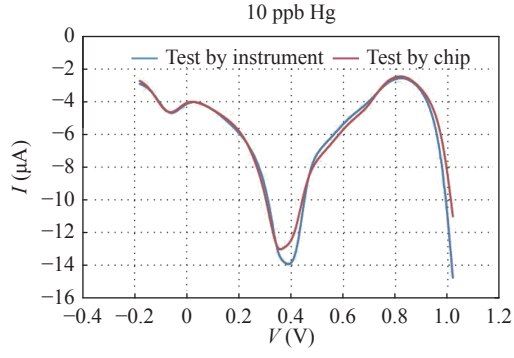

Figure 18 Measured sweep I-V characteristic curve of 10 ppb Hg^{2+}.

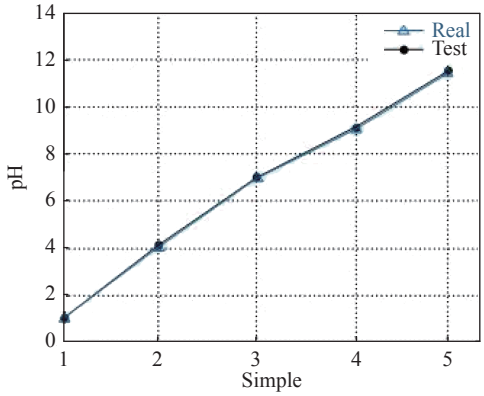

Figure 19 Measured of the output result of single-end voltage channel combining with pH sensor.

tual value is 0.1. Table 1 summarizes the characteristics of this AFE chip, and comparisons with prior results are made as well.

V. Conclusion

A multi-channel CMOS analog front-end interface IC has been presented. The chip consists of two highly sensitive current detection channels and two voltage detection channels, and it provides programmable voltage waveform needed by the sensor at the same time. The voltage detection dynamic range achieves 60 dB. The current detection dynamic range achieves 157.8 dB, which is larger than that of most state-of-art works. The input signals of sensors are converted into digital data with good linearity (the smallest R^2 of current channel is 0.9999, the smallest R^2 of voltage channel is 0.9982). The chip was fabricated in 0.18 μm CMOS process with supply voltage of 3.3 V. It achieves 12.88 pA_{RMS} and 33.7 μV_{RMS} at 10 kHz bandwidth. A prototype microsystem for a multifunctional sensor was constructed. Test results show that the circuit and the entire system function properly.

Table 1 Formal context

Parameters	This work	Ref. [6]	Ref. [7]	Ref. [8]	Ref. [9]
Technology (μm)	0.18	0.18	0.09	0.18	0.18
Supply (V)	3.3/1.8	1	2.5/1	1.8	2
Power	4.36 mW	1.55 μW	0.147 mW	5.22 mW	–
Current noise floor (Meas. with bandwidth)	12.9 pA (10 kHz)	–	75 fA (1 kHz)	204 fA (100 Hz)	100 fA (10 kHz)
Max. meas. current	1 mA	–	200 pA	11.6 μA	200 pA
Area (mm^2)	6.4	–	0.065	0.091	–
Current dynamic range (dB)	157.8	–	68.5	155.1	85
Voltage detection capability	Yes	Yes	No	No	No
Voltage dynamic range (dB)	89.4	73.48	–	–	–

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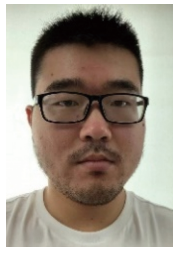

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