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Circuit Modeling and Performance Analysis of GNR@SWCNT Bundle Interconnects

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Abstract — In this paper, the single-walled carbon nanotube (SWCNT) with graphene nanoribbon (GNR) inside, namely GNR@SWCNT, is proposed as alternative conductor material for the interconnect applications. The equivalent circuit model is established, and the circuit parameters extracted analytically. By virtue of the equivalent circuit model, the signal transmission performance of GNR@SWCNT bundle interconnect is evaluated and compared with its Cu and SWCNT counterparts. The optimal repeater insertions in global- and intermediate-level GNR@SWCNT bundle interconnect are studied. Moreover, it is demonstrated that the GNR@SWCNT interconnects could provide superior performance, indicating that GNR@SWCNT structure would be beneficial for development of future carbon-based integrated circuits and systems.

Key words — GNR@SWCNT bundle, On-chip interconnect, Equivalent circuit mode, Time delay, Repeater insertion.

I. Introduction

In the past decades, the scaling minimum characteristic size of the transistors and interconnects has been an important driver of microchip performance improvement [1]. With the continuous development of integrated circuit technology, the distributed resistance and capacitance of interconnects are constantly increasing, whereas the resistance-capacitance (RC) product of the transistors has been reduced [2]. As the length exceeds a certain value, the interconnect delay becomes much larger than the gate delay, implying that the integrated circuit has entered "the interconnect era" [3], [4].

In order to improve the electrical properties and reliability of traditional metal interconnects, carbon nanotube (CNT) and graphene, which possess excellent properties including long mean free path (MFP), large relaxation time, high conductivity and high current-carrying capacity [3], have been proposed as attractive candidates for constructing on-chip interconnects [5]–[10]. The resistance-inductance-capacitance (RLC) circuit models of on-chip interconnects made of single-walled CNT (SWCNT) bundle and multi-walled CNT have been studied in-depth, indicating that the CNT interconnects have better performance than Cu wires [11]. Recently, it was experimentally demonstrated that graphene nanoribbon (GNR) can be grown inside the SWCNT [12], and its width was mainly determined by SWCNT diameter. This structure is named as GNR@SWCNT, and the optimal CNT diameter is about 1–2 nm. This is because that the SWCNT with diameter smaller than 1 nm do not have enough space for GNR growth, and it cannot effectively restrain the GNR growth if the diameter is larger than 2 nm [13]. Moreover, the GNR width must be at least 0.6 nm narrower than the CNT diameter [14], [15]. With the help of inside GNR, it can be anticipated that such structure of GNR@SWCNT can provide lower resistance than pure SWCNTs, and it is therefore suitable for interconnect applications.

This paper aims at investigating the ultimate performance of GNR@SWCNT bundle interconnect, and providing some useful guidelines for its development. The circuit model of GNR@SWCNT bundle interconnect is first developed, and the optimal repeater insertion is explored for intermediate- and global-level GNR@SWCNT bundle interconnects. The rest of this paper is organized as follows. Section II briefly introduces the circuit model of the GNR@SWCNT bundle

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interconnect. By virtue of the circuit model, the time delay of the GNR@SWCNT bundle interconnect is investigated and compared with the Cu and SWCNT counterparts. The optimal size and number of repeaters in global- and intermediate-level GNR@SWCNT bundle interconnects are extracted in Section III. Some conclusions are finally drawn in Section IV.

II. Circuit Modelling

As shown in Fig.1, the equivalent RLC circuit model is considered for evaluating CNT or GNR interconnects [16]. $R_{\rm d0}$ and $C_{\rm d0}$ are the driver resistance and capacitance, $C_{\rm l0}$ is the load capacitance, $R_{\rm c}$ is the contact resistance, and R, $L_{\rm k}$, and $C_{\rm q}$ are per-unit-length (p.u.l.) resistance, kinetic inductance, and quantum capacitance of the interconnect, respectively. $L_{\rm m}$ and $C_{\rm e}$ represent p.u.l. magnetic inductance and electrostatic capacitance of the interconnect, and they are determined by the geometry and surrounding dielectric material [17]. The interconnect parameters including width W, spacing S, height H, inter-layer dielectric (ILD) thickness T, and effective dielectric constant of the surrounding dielectric material ϵ_r are from ITRS projection and listed in Table 1 [18].

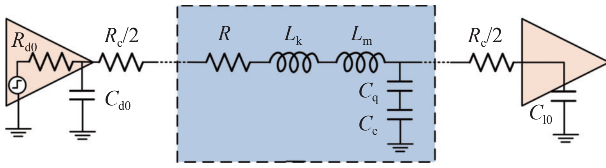

Fig. 1. Equivalent circuit model of carbon-based interconnects.

Table 1. Interconnect parameters adopted from ITRS [18]

	Technology node (nm)	14 nm	7 nm
Intermediate level	Interconnect width W	14 nm	7 nm
	Wire aspect ratio H/W	2.1	2.3
	ILD aspect ratio T/W	1.9	1.9
Global level	Interconnect width W	21 nm	11 nm
	Wire aspect ratio H/W	2.34	2.4
	ILD aspect ratio T/W	1.5	1.5
Minimum-sized gate	Driver resistance $R_{\rm d0}$ W	30.3 kΩ	69.7 kΩ
	Driver capacitance $C_{\rm d0}$	0.22 fF	0.13 fF
	Load capacitance $C_{\rm l0}$	0.15 fF	0.06 fF
Effective dielectric constant ϵ_r		2.08	1.65

1. Nanoscale Cu

With the continuous reduction of the interconnect dimension, the width is gradually close to the MFP of Cu, thereby leading to a sharp increase in the resistivity. The effective resistivity of Cu is given as [19]

$$\rho_{\rm Cu} = \rho_0 \left[\frac{\frac{1}{3}}{\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)} \right] + \frac{3C}{8}(1 - p_{\rm Cu})\frac{1 + {\rm AR}}{\rm AR}\frac{\lambda_{\rm Cu}}{W_{\rm Cu}} \tag{1}$$

where $C = 1.2$, $\alpha = (\lambda_{\rm Cu} R_g)/[d_g(1 - R_g)]$, $\rho_0 = 2.04$ μΩ·cm is the bulk resistivity, $\lambda_{\rm Cu} = 37.3$ nm is the MFP, $R_g = 0.22$ is specularity parameter, and AR is the aspect ratio. $d_{\rm g}$ is the average distance between grain boundaries and it is usually assumed as the interconnect width. As the barrier thickness $T_{\rm b}$ occupies a significant fraction of the metal area, the effective interconnect width and height are $W_{\rm Cu} = W - 2T_{\rm b}$ and $H_{\rm Cu} = H - 2T_{\rm b}$, respectively, and ${\rm AR} = H_{\rm Cu}/W_{\rm Cu}$. The per-unit-length resistance of Cu wire is calculated by $R_{\rm Cu} = \rho_{\rm Cu} l/(W_{\rm Cu} H_{\rm Cu})$, and $R_{\rm c} = 0$. According to [20], the capacitance of the GNR@SWCNT bundle is approximately same with the capacitance value for Cu wire with the same cross-dimensions. Therefore, $C_{\rm e}$ is extracted using ANSYS Maxwell, with the parameter settings listed in Table 1 [16], and $L_{\rm m} = (\mu_0 \epsilon_0)/C_{\rm e}$.

2. SWCNT

The conductance of an isolated SWCNT can be evaluated by utilizing the Landauer-Buttiker formula $G = (2e^2 N_{\rm ch})/h$, where e is electron charge and h is the Plank's constant. $N_{\rm ch}$ is the number of conducting channels, and it equals 2 for metallic SWCNTs. The quantum resistance is evenly distributed at both ends and it is calculated by $R_{\rm q} = h/(2e^2 N_{\rm ch}) = 12.9/N_{\rm ch}$ kΩ [21]. For SWCNTs longer than the MFP $\lambda_{\rm SWCNT}$, the p.u.l. scattering resistance is expressed as [22]

$$R = R_{\rm q}/\lambda_{\rm SWCNT} \tag{2}$$

where $\lambda_{\rm SWCNT} = 1000D$ and D is the diameter. Note that the model of SWCNT resistance has been validated experimentally in [23].

SWCNT bundle has same electrostateic capacitance with Cu wire, and the quantum capacitance $C_{\rm q}$ is usually ignored as it is much larger than $C_{\rm e}$. The kinetic inductance is given by [24]

$$L_{\rm k} = R_{\rm q}/((2v_{\rm F} N_{\rm ch})) \tag{3}$$

where $v_{\rm F} = 8\times10^5$ m/s is the Fermi velocity. The p.u.l. inductance of the SWCNT interconnect is $L = L_{\rm k} + L_{\rm m}$. The contact resistance of SWCNT interconnect is $R_{\rm c} = R_{\rm mc} + R_{\rm q}$, where $R_{\rm mc}$ denotes the imperfect contact resistance per tube [25]. In this study, $R_{\rm mc}$ is ignored as it highly depends on the fabrication process.

3. Monolayer GNR

The conductance of a monolayer GNR is mainly re-

lated to the width and Fermi level, and the number of conducting channels is calculated by [7]

$$N_{\mathrm{ch}}=\sum_{i=0}^{n_c}\left(1+\mathrm{e}^{\frac{E_i-E_{\mathrm{F}}}{k_{\mathrm{B}}T}}\right)^{-1}+\sum_{i=0}^{n_v}\left(1+\mathrm{e}^{\frac{E_i+E_{\mathrm{F}}}{k_{\mathrm{B}}T}}\right)^{-1} \quad (4)$$

where $E_i=(hv_{\mathrm{F}}|i+\beta|)/(2W)$ and $\beta=1/3$ for metallic GNR. The extraction method of N_{ch} has been validated through comparison with numerical method, i.e., non equilibrium Green function (NEGF) [8]. Similar with the SWCNT, for a GNR longer than its mean free path λ_{GNR}, the p.u.l. scattering resistance is given as $R=R_{\mathrm{q}}/\lambda_{\mathrm{GNR}}$, where λ_{GNR} is assumed as 1 μm [25]. The kinetic inductance p.u.l. can be obtained from $L_{\mathrm{k}}=8/N_{\mathrm{ch}}$ nH/μm [26].

4. GNR@SWCNT Bundle

As experimentally demonstrated in reference [12], GNR can be grown inside the SWCNT with appreciate filling and consecutive chemical reaction techniques (as shown in Fig.2). The equivalent circuit model of an isolated GNR@SWCNT interconnect is given in Fig.3. It is worth noting that the GNR@SWCNT is totally a new product, and more efforts are needed for exploring its design, modeling, fabrication, and integration. To investigate its ultimate performance, the GNR@SWCNT structure is viewed as a parallel series of SWCNT and GNR. The scattering resistance and inductance are therefore calculated as

$$R=\frac{h}{2e^2}\frac{1}{N_{\mathrm{ch,SWCNT}}\lambda_{\mathrm{SWCNT}}+N_{\mathrm{ch,GNR}}\lambda_{\mathrm{GNR}}} \quad (5)$$

$$L_{\mathrm{k}}=\frac{h}{4e^2v_{\mathrm{F}}}\frac{1}{N_{\mathrm{ch,SWCNT}}+N_{\mathrm{ch,GNR}}} \quad (6)$$

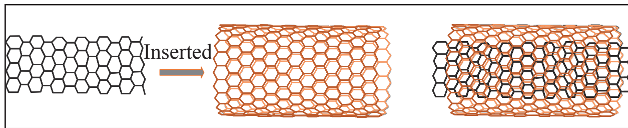

Fig. 2. Schematic of GNR@SWCNT structure.

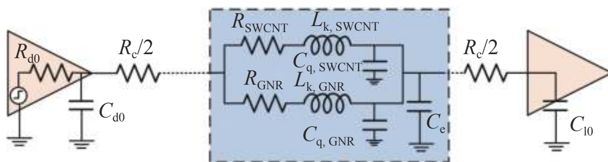

Fig. 3. Equivalent circuit model of an isolated GNR@SWCNT interconnect.

The quantum capacitance is a series combination of the quantum capacitances of SWCNT and GNR, and it is ignored as it is much larger than the electrostatic one. To reduce the resistance, a bundle of tubes is usually employed. To evaluate their ultimate potential for interconnect applications, the SWCNTs involved are assumed as metallic, and the spacing between adjacent tubes is van der Waal's gap $\delta=0.34$ nm. The number of tubes in the bundle is calculated by [18]

$$N=N_wN_h-\mathrm{Inter}\left[\frac{N_h}{2}\right] \quad (7)$$

where Inter[·] denotes that only the integer part is considered, $N_w=\mathrm{Inter}[(W-D)/(D+\delta)]+1$, and $N_h=\mathrm{Inter}[2/\sqrt{3}\cdot(H-D)/(D+\delta)]+1$.

Fig.4 shows the p.u.l. resistances of global-level Cu, SWCNT bundle and GNR@SWCNT bundle interconnects at the 14 nm and 7 nm nodes. In the figure, the width is gradually increased, with other parameters adopted from Table 1. It is evident that GNR@SWCNT bundle interconnect provides smaller resistance than its Cu and SWCNT counterparts due to additional conducting channels provided by the inside GNRs. Additionally, it is anticipated that the number of inside graphene layers would increase with the development of fabrication process, and the resistance can be further reduced with the increasing graphene layer number.

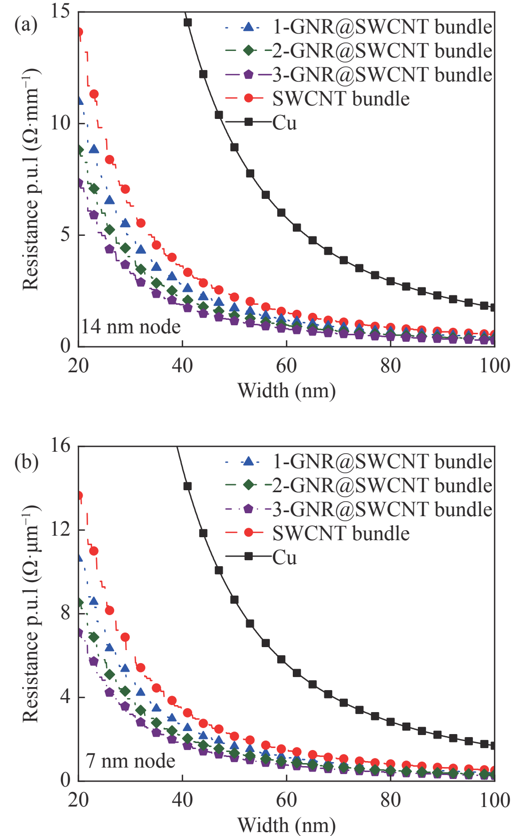

Fig. 4. Resistances p.u.l. of (a) 14 nm and (b) 7 nm node global-level interconnects.

By virtue of the RLC circuit model, the time delay of the GNR@SWCNT bundle interconnect is investigated. The time delay of driver-interconnect-load system is calculated by [27]

$$T_{\mathrm{s}} = (1.48\xi + \mathrm{e}^{-2.9\xi^{1.35}})\sqrt{L_{\mathrm{t}}(C_{\mathrm{t}} + C_{\mathrm{l0}})} \tag{8}$$

with

$$\xi = \frac{R_{\mathrm{t}}}{2}\sqrt{\frac{C_{\mathrm{t}}}{L_{\mathrm{t}}}}\frac{R_{\mathrm{T}} + C_{\mathrm{T}} + R_{\mathrm{T}}C_{\mathrm{T}}\left(1 + \dfrac{C_{\mathrm{d0}}}{C_{\mathrm{l0}}} + 0.5\right)}{\sqrt{1 + C_{\mathrm{T}}}} \tag{9}$$

where $R_{\mathrm{T}} = R_{\mathrm{d0}}/R_{\mathrm{t}}$, $R_{\mathrm{t}} = Rl + R_{\mathrm{c}}$, $C_{\mathrm{T}} = C_{\mathrm{l0}}/C_{\mathrm{t}}$, $L_{\mathrm{t}} = (L_{\mathrm{k}} + L_{\mathrm{m}})l$, and $C_{\mathrm{t}} = C_{\mathrm{e}}l$. Figs.5 and 6 show the time delays of the global- and intermediate-level Cu, SWCNT bundle, and GNR@SWCNT bundle interconnects at the 14 nm and 7 nm nodes. The sizes of driver/load are assumed to be 100 and 50 times the minimum size for global- and intermediate-level interconnects, respectively. It is evident that GNR@SWCNTs have superior performance in comparison with Cu and SWCNT counterparts as it has smallest resistance.

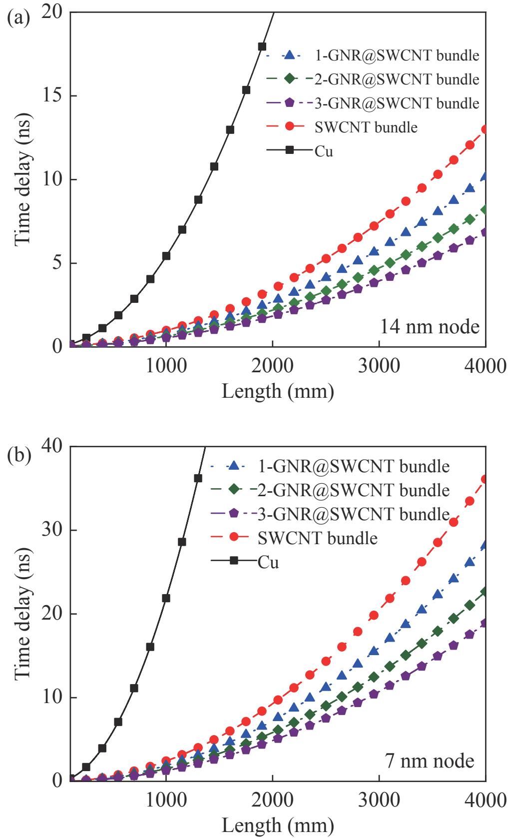

Fig. 5. Time delay of (a) 14 nm and (b) 7 nm node global-level interconnects.

III. Repeater Insertion

As the interconnect delay increases exponentially with the length, it is intuitive to insert repeaters in long interconnect to improve the performance, as shown in Fig.7. As the SWCNT bundle has many conducting channels, the contact resistance has little influence on

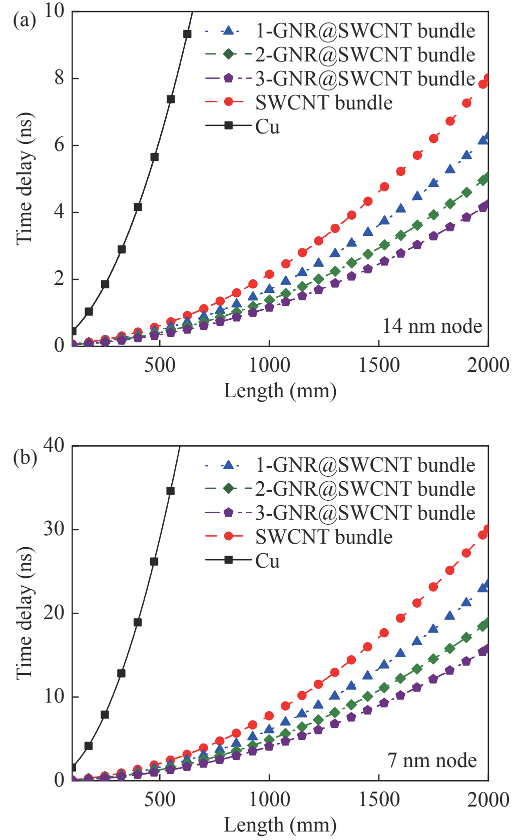

Fig. 6. Time delay of (a) 14 nm and (b) 7 nm node intermediate-level interconnects.

its repeater insertion [18]. Therefore, the optimal size and number of repeaters in GNR@SWCNT bundle interconnect can be calculated by [27]

$$h_{\mathrm{opt}} = \sqrt{\frac{R_{\mathrm{d0}}C_{\mathrm{t}}}{R_{\mathrm{t}}C_{\mathrm{l0}}}}\frac{1}{[1 + 0.18(T_{L/R})^3]^{0.26}} \tag{10}$$

$$k_{\mathrm{opt}} = \mathrm{Inter}\left[\sqrt{\frac{L_{\mathrm{t}}C_{\mathrm{t}}}{2(T_{L/R})^2}}\frac{1}{[1 + 0.21(T_{L/R})^3]^{0.28}}\right] \tag{11}$$

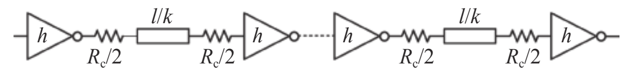

Fig. 7. Repeaters inserted in a long interconnect of length l to minimize delay.

where $T_{L/R} = \sqrt{L_{\mathrm{t}}R_{\mathrm{d0}}(C_{\mathrm{d0}} + C_{\mathrm{l0}})/R_{\mathrm{t}}}$, $R_{\mathrm{T}} = R_{\mathrm{d0}}/(hR_{\mathrm{t}})$, $R_{\mathrm{t}} = Rl/k + R_{\mathrm{c}}$, $C_{\mathrm{T}} = hC_{\mathrm{l0}}/C_{\mathrm{t}}$, and $C_{\mathrm{t}} = C_{\mathrm{e}}l/k$. The delay of each segment could be obtained by

$$T_{\mathrm{seg}} = (1.48\xi + \mathrm{e}^{-2.9\xi^{1.35}})\sqrt{\frac{Ll}{k}\left(\frac{C_{\mathrm{e}}l}{k} + hC_{\mathrm{l0}}\right)} \tag{12}$$

and total interconnect delay is

$$T_{\mathrm{t}} = (k+1)T_{\mathrm{seg}} \tag{13}$$

Fig.8 show the optimal number of repeaters $k_{\rm opt}$ in global-level Cu, SWCNT bundle, and GNR@SWCNT bundle interconnects at 14 nm and 7 nm technology nodes, respectively. As shown in Fig.8, $k_{\rm opt}$ increases linearly with the increasing length, and the requirement of repeaters for GNR@SWCNT is lesser than the Cu and SWCNT bundle counterparts. In particular, $k_{\rm opt}$ for GNR@SWCNT bundle interconnect is approximately half of that for Cu wires, which may save power consumption and area. As shown in Fig.9, $h_{\rm opt}$ is nearly unchanged with the increasing interconnect length. Moreover, the values of $h_{\rm opt}$ for GNR@SWCNT bundle interconnects are larger than those for Cu and SWCNT bundle interconnect counterparts, which may be attributed to their low resistances.

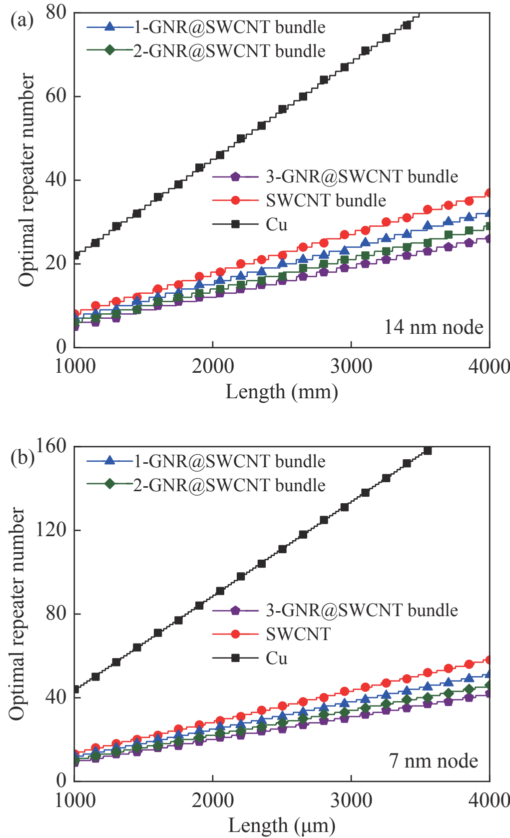

Fig. 8. Optimal number of repeaters in global-level interconnects at (a) 14 nm and (b) 7 nm technology nodes.

By substituting $k_{\rm opt}$ and $h_{\rm opt}$ into equation (13), total time delay of the interconnects can be obtained. The time delays of the global- and intermediate-level Cu, SWCNT bundle, and GNR@SWCNT bundle interconnects at 14 nm and 7 nm technology nodes are plotted in Figs.10 and 11. It is evident that the time delay can be reduced significantly with the insertion of repeaters, and it increases linearly as the length increases. Moreover, GNR@SWCNT is superior to its Cu and

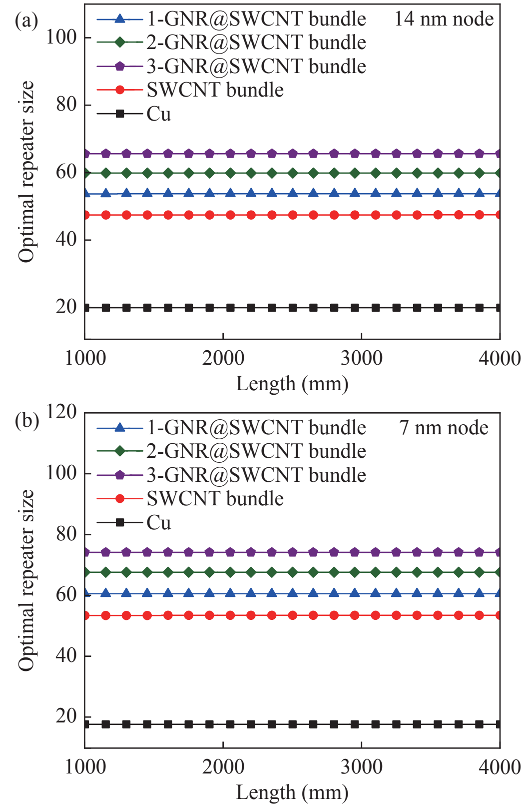

Fig. 9. Optimal size of repeaters in global interconnect level at (a) 14 nm and (b) 7 nm technology nodes.

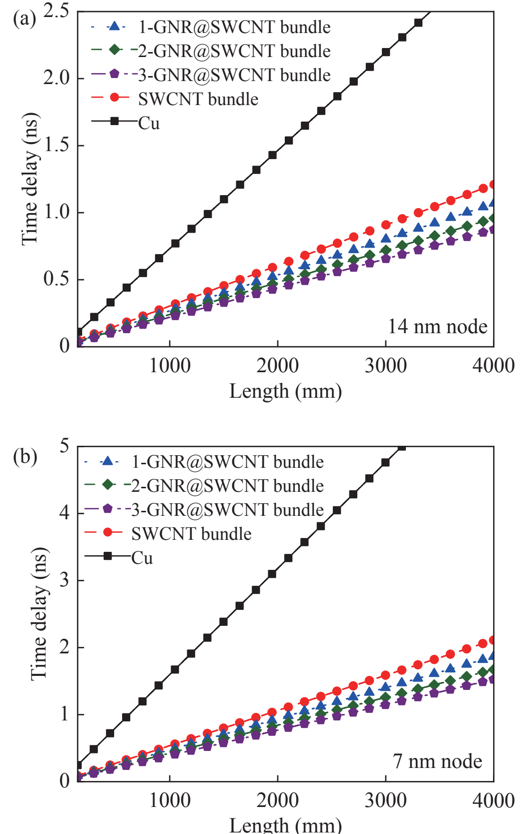

Fig. 10. Time delay of (a) 14 nm and (b) 7 nm node global level interconnects.

SWCNT counterparts, which proves the feasibility of the GNR@SWCNT structure for improving the electrical performance.

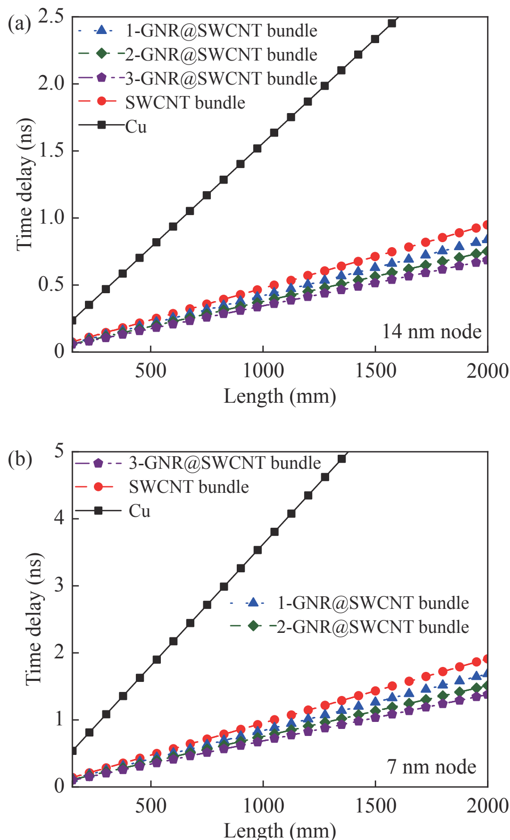

Fig. 11. Time delay of intermediate-level interconnects at (a) 14 nm and (b) 7 nm technology nodes.

IV. Conclusions

In order to improve the performance of on-chip interconnects, GNR@SWCNT was explored in this paper. The equivalent circuit model of GNR@SWCNT bundle interconnect was established, with the per-unit-length resistance and inductance calculated analytically. It was demonstrated that GNR@SWCNT bundle possesses smaller resistance than its Cu and SWCNT bundle due to additional conducting channels provided by the inside GNR. Further, the repeater insertion technique was explored for GNR@SWCNT bundle interconnects, and the time delay could be reduced with the insertion of repeaters. It was demonstrated that the implementation of GNR@SWCNT structure can significantly improve the electrical performance, indicating the high potential of GNR@SWCNT as on-chip interconnect in future carbon-based integrated circuits.

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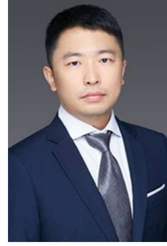

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