Analysis of Capacitance Characteristics of Light-Controlled Electrostatic Conversion Device

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Abstract — **In recent years, converting environmental energy into electrical energy to meet the needs of modern society for clean and sustainable energy has become a research hotspot. Electrostatic energy is a pollution-free environmental energy source. The use of electrostatic conversion devices to convert electrostatic energy into electrical energy has been proven to be a feasible solution to meet sustainable development. This paper proposes a light-controlled electrostatic conversion device (LCECD). When static electricity comes, an avalanche breakdown occurs inside the LCECD and a low resistance path is generated to clamp the voltage, thereby outputting a smooth square wave of voltage and current. Experiments have proved that LCECD can convert 30kV electrostatic pulses into usable electrical energy for the normal operation of the back-end light-emitting diode lights. In addition, the LCECD will change the parasitic capacitance after being exposed to light. For different wavelengths of light, the parasitic capacitance exhibited by the device will also be different. The smaller the parasitic capacitance of the LCECD, the higher the efficiency of its electrostatic conversion. This is of great significance to the design of electrostatic conversion devices in the future.**

Key words — **Environmental energy, Electrostatic energy, Electrostatic conversion, Parasitic capacitance.**

I. Introduction

In recent years, with the continuous development of various electronic devices, the global demand for power supply has also increased. Modern society requires clean energy to meet sustainable development. Therefore, converting various environmental mechanical energy into electrical energy is a feasible solution [1], [2]. Due to the diversity and extensiveness of mechanical energy in the environment, the collection of mechanical energy has received widespread attention and achieved good results. Various energy harvesting methods have been reported recently, such as solar energy [3]–[5], piezoelectric nanogenerators [6]–[8] and triboelectric nanogenerators [9]–[11]. Among these methods, the triboelectric nanogenerator has been proved to be a clean and sustainable development strategy. It has the characteristics of small size, high efficiency, and low cost. Lei Zhai *et al.* proposed an energy harvester coupled with a triboelectric mechanism and electrostatic mechanism [12]. By exposing the electrodes of the bracelet which is integrated onto the arm, the energy of the swinging arm and the energy generated by the separation and contact between the foot and the ground during movement can be obtained simultaneously. Ugur Erturun *et al.* proposed an energy harvester that combines a piezoelectric nanogenerator and an electret-based electrostatic generator [13], [14]. By changing the ratio between the monomer and the cross-linker of the polymer matrix, the structure can easily change the mechanical impedance of the device, making it suitable for the development of energy collection devices for various applications. Gang Cheng *et al.* proposed a triboelectric nanogenerator that can simultaneously obtain electrostatic energy and mechanical energy from running water [15]. Flowing water carries two kinds of energy. One is the mechanical energy of water movement. The second type is electrostatic energy. This electrostatic energy comes from the frictional charge generated by contact and electrification when water travels in the pipe or in the air.

The daily activities of human beings and natural phenomena in nature will also produce a lot of static electricity. When the human body is charged with a certain amount of static electricity due to friction and other reasons and then comes into contact with other objects to discharge, the human body is equivalent to a model with a resistance of 1.5 kΩ and a capacitance of 100 μF. This discharge mode is a human body model (HBM). These electrostatic voltages are usually between 3 kV and 30 kV. At the moment of electrostatic discharge, hundreds of millions of joules of energy can be released. Usually, people don't think that static electricity is useful, and even want to avoid it, because the instantaneous strong voltage can burn out electronic products. However, if static electricity can be used, it will ease the pressure on energy supply. At the same time, electrostatic energy, as an environmental energy source, also meets the requirements of clean energy and sustainable development.

In this paper, a light-controlled electrostatic conversion device (LCECD) has been presented. The device uses the positive feedback principle of two parasitic bipolar junction transistors (BJT) to form a low-resistance path when static electricity comes, which can clamp the voltage to below 10 V in tens of nanoseconds. The stable voltage and current output after the static electricity is clamped can be supplied to the back-end load to work normally, so as to achieve the purpose of using static electricity energy. Experimental results show that LCECD can convert 30 kV electrostatic pulses into usable electrical energy. In addition, LCECD can change its parasitic capacitance by applying different wavelengths of illumination. Experimental

results show that for LCECD, smaller parasitic capacitance can achieve higher electrostatic conversion efficiency. This provides a valuable reference for the design of subsequent electrostatic conversion devices.

II. Device Working Principle and Capacitance Characteristic Analysis

The three-dimensional structure diagram of LCECD is shown in Fig.1. The anode and cathode of the device are both connected by highly doped P+, N+ and polysilicon gates. One side of the polysilicon gate is N+, and the other side is shallow trench isolation (STI). The material for making STI is SiO_2. This can prevent the gate-source breakdown or source-drain breakdown of the device, and improve the stability of the device. The floating P+ is surrounded by STI and contained in P-Well. The N+ of the unconnected potential in the middle is also surrounded by STI. N-Well and P-Well are not directly connected, but separated by DN-Well. Here, the contact surface of P-Well and DN-Well can be equivalent to two PN junctions. J1 and J2 represent PN junctions formed on the side of P-Well and DN-Well/N-Well. J3 and J4 respectively represent the bottom PN junction. The N-Well and two P-Wells constitute a parasitic PNP BJT. N-Well, cathode P-Well and cathode N+ constitute a parasitic NPN1 BJT. N-Well, anode P-Well and anode N+ constitute a parasitic NPN2 BJT. The key dimensions of LCECD are shown in Table 1.

1. The working principle of LCECD

Light passes through the STI and is applied to the J1 junction and the J2 junction to achieve light control of the device. For the J2 junction, due to the excita-
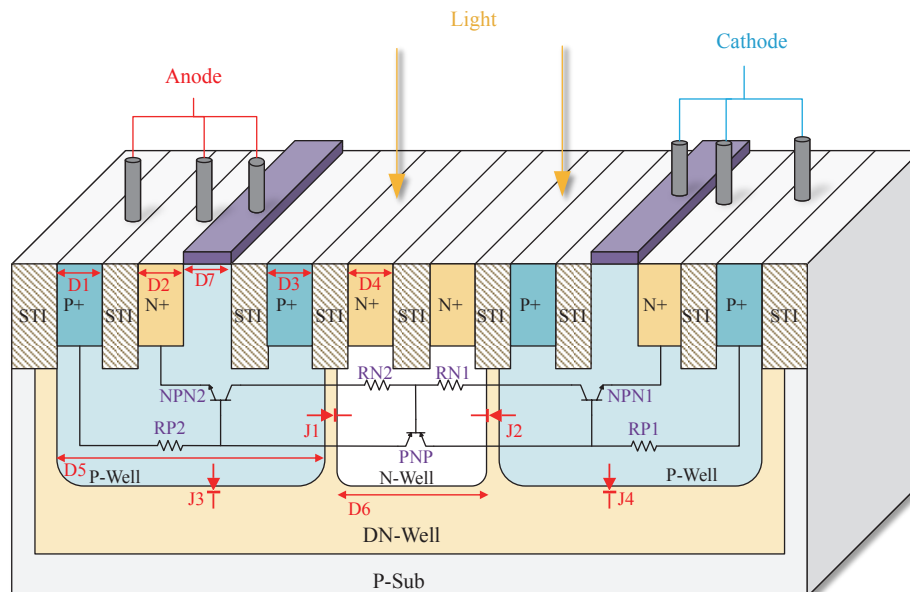

Fig. 1. Three-dimensional structure diagram and equivalent circuit of LCECD.

Table 1. Partial dimensions of LCECD

Area label	Width (μm)
D1	4.28
D2	4.28
D3	1
D4	1
D5	16.22
D6	3.2
D7	4

tion of photon energy, the N-well generates some minority carrier holes, and the P-well generates some minority carrier electrons. Under the action of the built-in electric field, the excited holes move to the P-well, and the electrons move to the N-well. This increases the potential of the P region and decreases the potential of the N region, and accumulates positive and negative charges on both sides of the PN junction to form a photovoltaic voltage. At the same time, the holes move to the P-Well, forming the base current of the NPN BJT, and the electrons move to the N-Well, forming the base current of the parasitic PNP BJT. When static electricity comes, a strong voltage will be applied to the anode of the device. And due to the transistor effect, the photocurrent will be amplified, resulting in avalanche breakdown of the reverse-biased J2 junction. A large number of avalanche carriers flow through the N-Well, causing a voltage drop on the N-Well and turning on the parasitic PNP BJT. At the same time, due to the amplification of the parasitic PNP BJT, the increasing current makes the voltage drop of the cathode P-Well increase continuously, which leads to the conduction of the parasitic NPN1 BJT. The two parasitic BJTs form a positive feedback loop, causing the device to form a PNPN low resistance path from anode to cathode. After the low-resistance path is formed, the device can clamp a voltage of tens of thousands of volts to about ten volts so that the back-end load can work normally.

Silvaco software is used to simulate the device in two dimensions to verify the working process of the LCECD. In this section, the DC simulation of the device is performed using Silvaco's Atlas. The initial voltage step is 0.05 V, and when the current reaches 1 nA, the voltage step becomes 1.5 V. When the current reaches 3 mA, the sweep ends. A Gaussian distribution light with a wavelength of 600 nm is added, and the light intensity is 10 W/cm^2. The illumination angle is set to 90 degrees, which means that the illumination is perpendicular to the surface from the top of the device. The applied illumination covers the entire J2 junction, as indicated by the yellow circle in Fig.2. Fig.2(a) shows the doping concentration distribution inside the device and the photon absorption rate. It can be seen
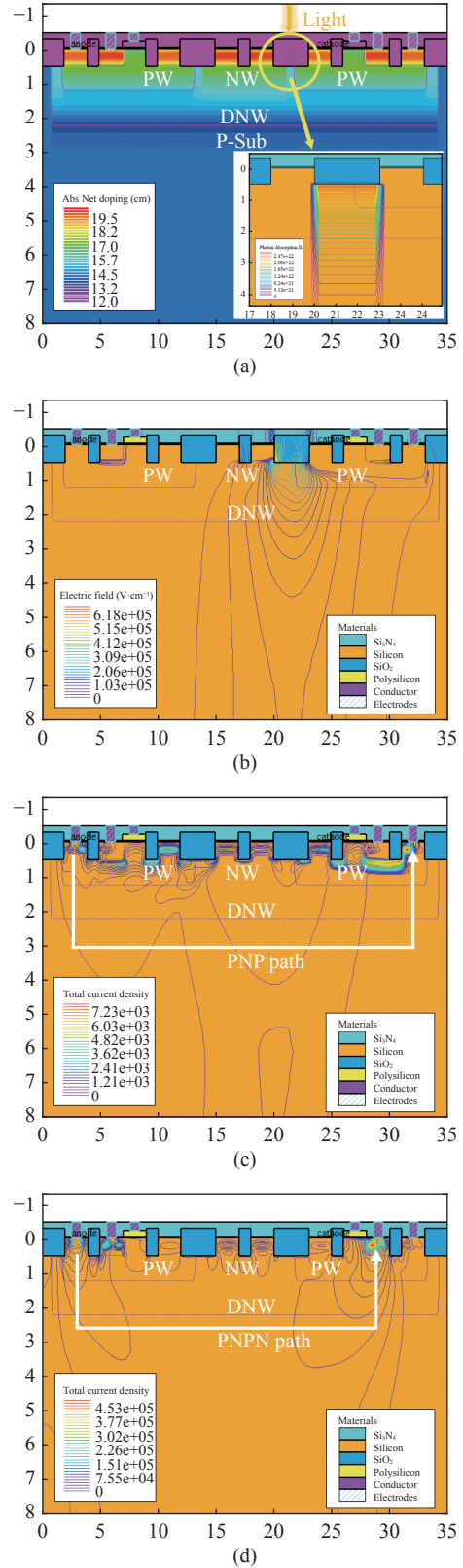

Fig. 2. Simulation results of LCECD. (a) Doping concentration distribution; (b) Electric field distribution at initial turn-on; (c) Current density at initial turn-on; (d) Current density at full turn-on.

from the figure that the photons are mainly absorbed by the reverse-biased PN junction J2 formed by N-Well

and P-Well. In the definition of the LCECD structure, the doping concentration of the N+ region is set to 9×10^{19} cm^{-3}, and the doping concentration of the P+ region is set to 5×10^{19} cm^{-3}. The doping concentration of P-Well and N-Well is set to 9×10^{16} cm^{-3}, and the doping concentration of DN-Well is set to 2×10^{15} cm^{-3}. The above regions are all Gaussian distributions. The P-Substrate is uniformly distributed at a concentration of 1×10^{14} cm^{-3} (because the foundry cannot provide the exact doping concentration, junction depth and other specific process parameters of the device. Therefore, using Atlas device-level simulations can only qualitatively verify the working principle of LCECD, but cannot quantitatively characterize its actual electrical performance). Fig.2 (b) shows the electric field distribution of LCECD when static electricity comes. It can be seen from the figure that the highest electric field distribution is the contact surface between N-Well and cathode P-Well. This is due to the avalanche breakdown occurring here and a large number of carriers are generated. Similarly, the current density distribution of the device can be seen from the simulation results, as shown in Fig.2(c). When the device is initially turned on, the current density distribution shows an obvious current path. The current path is made up of DN-Well and two P-Wells. This is a parasitic PNP BJT. At this time, there is no current density distribution under N+ of the cathode, indicating that the parasitic NPN transistor has not been turned on. Fig.2 (d) shows the current density distribution after the device is fully turned on. At this time, the device has formed a PNPN low-resistance path from the anode P-Well to the cathode N+, and the current density distribution below N+ is extremely high. These simulation results verify the working principle of LCECD.

2. Analysis of the parasitic capacitance characteristics of LCECD

PN junction capacitance includes diffusion capacitance and barrier capacitance. The main PN junction distribution of LCECD is shown as in Fig.1. C_{J1}, C_{J2}, C_{J3}, and C_{J4} represent the parasitic capacitance of the J1, J2, J3, and J4 junctions, respectively. The parasitic capacitance of LCECD can be represented as:

$$C_{\text{LCECD}} = \frac{(C_{J1} + C_{J3})(C_{J2} + C_{J4})}{C_{J1} + C_{J2} + C_{J3} + C_{J4}} \qquad (1)$$

When the J2 is irradiated by light, some electrons in the depletion layer absorb photon energy and then jump from the valence band to the conduction band, resulting in unbalanced carriers forming current in the J2. The electric field generated by the photon cancels the electric field a fraction of the depletion region of the J2. Therefore, the depletion region of J2 becomes thin-

ner and the barrier capacitance increases. Since the photon energy of different light wavelengths is different, the capacitance of LCECD varies with the wavelength reaction of the depletion region of J2. After the bias voltage is applied to the anode of the LCECD, the parasitic capacitance of the device is related to the accumulation of photons generated by the voltage change on the device. As the anode voltage increases, current injection recombines electrons and holes in J1 and J2. When the bias voltage is small, there are barrier capacitance and diffusion capacitance in PN junction. The diffusion capacitance is:

$$C_D = \left(Aq^2 pL/kT \right) \exp \left(qV_F/kT \right) \qquad (2)$$

Here, q is the electron charge and p is the minority carrier concentration. Therefore, when p increases, C_{J1} and C_{J3} also increase. For the J2 and J4 junctions, since the DN-Well/P-Well junction is in the reverse bias state, the diffusion capacitance can be ignored. Due to the existence of external voltage, the depletion region becomes wider and the barrier capacitance decreases. But, the carrier generated by J2 absorbing photon energy offsets a fraction of the depletion region, preventing the values of C_{J2} and C_{J4} from decreasing due to the applied electric field. As the current increases, the amount of carriers keeps increasing. In view of the capacitance is the number of carriers relative that to differential of voltage, the capacitance of the LCECD increases with the increase of voltage. When the voltage applied to LCECD go rises a certain value, the applied voltage broadens the depletion region, and the speed of carrier consumption keeps up with that produced by J2 under light. At this time, the capacitance value of LCECD reaches the maximum.

When the applied voltage keeps increasing, since J1 and J3 are forward biased, C_{J1} and C_{J3} are mainly determined by the size of the diffusion capacitance. J2 and J4 are in reverse biased state, and the depletion region widens as the bias voltage increases, which increases the carrier consumption. Under illumination, the correlation between the reversed-biased voltage and the barrier capacitance is as follows:

$$1/C_B^2 = \left(2/A^2 qN\epsilon\epsilon_0 \right) (V_R + V_D) \qquad (3)$$

Here, areas of J2 and J4 are A, and N denotes the doping concentration of DN-Well. V_R is an applied voltage, and contact potential difference expressed by V_D. Obviously, the capacitance values of C_{J2} and C_{J4} decrease non-linearly with the increase of V_R. Under high voltage, the reduced value of barrier capacitance is greater than the rising value of diffusion capacitance and the velocity of carriers consumed in the depletion

region is greater than that excited by photons. In this case, the capacitance of the LCECD shows a downward trend.

In summary, the $C(V)$ characteristics of LCECD can be summarized as follows: with the applied voltage continuously increasing, the capacitance of LCECD increases first, and then decreases after reaching the peak.

III. Experimental Result

In this work, the LCECD was manufactured to verify its electrostatic conversion capability and its $C(V)$ characteristics. The LCECD was manufactured by 180 nm BCD process without any process modification. Therefore, LCECD is compatible with standard CMOS processes. The layout of the LCECD is shown in Fig.3(a). The device structure layout is eight fingers with a finger length of 80 μm. Fig.3(b) and (c) are the microscope image and package diagram of the LCECD, respectively.
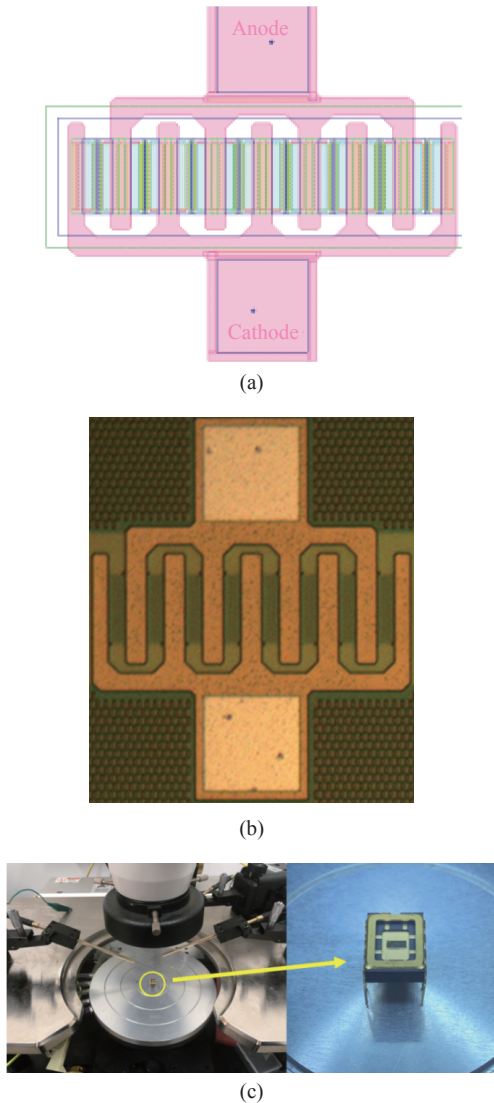
1. Electrostatic conversion experiment

In order to verify the voltage clamping capability of the LCECD, a transmission line pulse (TLP) test was performed on the device. A TLP measurement system with a rising edge of 10 ns and a pulse width of 100 ns is used to obtain the voltage and current curves of the device with respect to time. When the LCECD is subjected to an electrostatic pulse, the strong voltage causes an avalanche breakdown on the trigger surface of the device, and the device can form a low resistance path in a short time to clamp the voltage. Fig.4 shows the voltage trend of the LCECD measured under 25 V, 35 V, and 45 V square wave pulses. It can be seen from the test results that after receiving a square wave pulse higher than 25 V, the device can clamp the voltage to a lower value within 25 ns, and clamp the voltage to below 10 V within 50 ns. Obviously, the device has converted the electrostatic pulse into a smooth square wave pulse output after 50 ns, so it can provide a stable power supply for the back-end load.
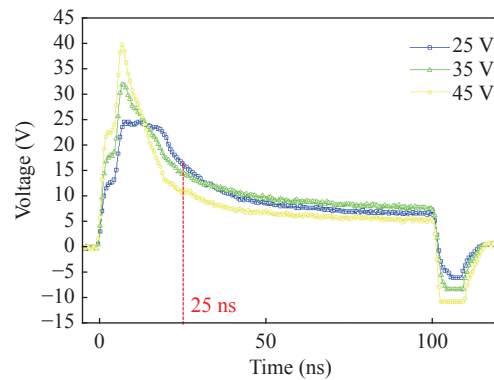

(a)

(b)

(c)

Fig. 3. The layout (a), the microscope image (b), and the package diagram (c) of LCECD.

Fig. 4. *V-T* curve across LCECD under TLP test.

Fig.5 shows the current change trend under the same pulse measured at both ends of the LCECD. Similarly, after the device receives an electrostatic pulse for 50 ns, it can stably output a steady current square wave. The stronger the applied voltage pulse, the higher the output current.
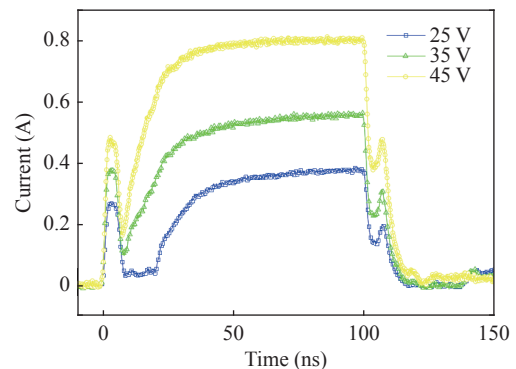

Fig. 5. *I-T* curve across LCECD under TLP test.

The experimental platform shown in Fig.6 is built to further verify the feasibility of the electrostatic energy conversion of LCECD. An electrostatic gun is used here to simulate a real electrostatic pulse. Two experiments were carried out, the electrostatic gun was set to 15 kV and 30 kV HBM static electricity respectively, and the discharge method was contact discharge. The electrostatic gun is in contact with the anode of the LCECD, and the cathode of the device is connected in series with one (or five) light-emitting diode (LED) lights, and then grounded. In two experiments, five contact discharges were performed on LCECD using an electrostatic gun respectively. The experimental results are shown in Fig.7 (a) and (b). The LED lights up at
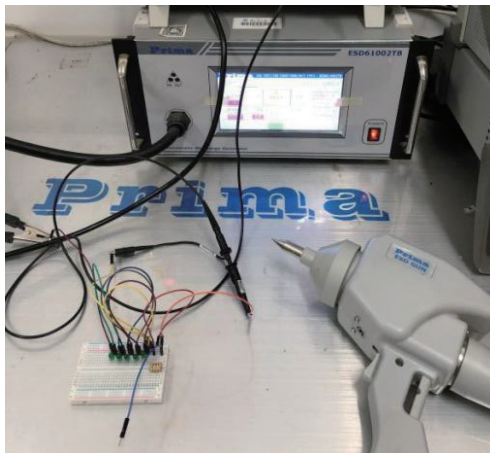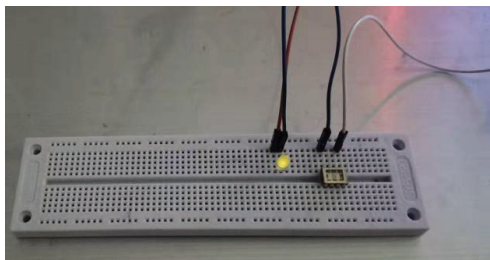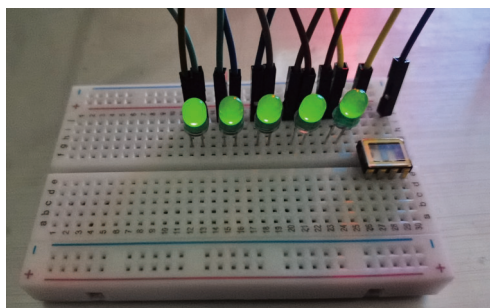

Fig. 6. Experimental platform for electrostatic conversion experiment.

(a)

(b)

Fig. 7. Electrostatic gun discharge lights up the LED light. (a) With a 15 kV HBM electrostatic; (b) With a 30 kV HBM electrostatic.

the moment of electrostatic discharge and can work normally. The experimental results of five contact discharges are the same. The repeatability of the experiment shows that the LCECD and the LED lamp are not burned out by 15 kV and 30 kV static electricity, and further shows that the LCECD can convert high-voltage static electricity into usable electrical energy output for the back-end load to work.

2. The relationship between the parasitic capacitance of LCECD and the electrostatic conversion efficiency

In order to study the influence of the parasitic capacitance of the LCECD on the electrostatic conversion efficiency, the light control characteristics of the device must first be verified. Here, the parasitic capacitance under different illuminations is tested. The bias voltage range set here is from -2.5 V to 2.5 V, and the test frequency is 1 MHz. In order to ensure the consistency of the light intensity, the light source is illuminated from the same position and the same angle, and the power of the light source is the same. The $C(V)$ test results of LCECD under different light are shown in Fig.8. The test result shows that when the bias voltage slowly increases from 0, the parasitic capacitance will increase first. After reaching the maximum value, the parasitic capacitance of LCECD shows a nonlinear downward trend. This verifies the parasitic capacitance characteristics of the LCECD in Section II. Furthermore, the capacitance of the LCECD changes with the change of light wavelength due to the different photon energies at different light wavelengths. The results of the test indicate that the capacitance of the LCECD is the largest under red light (wavelength 740 nm), followed by blue light (wavelength 450 nm), green light (wavelength 550 nm), and the smallest under orange light (wavelength 580 nm).
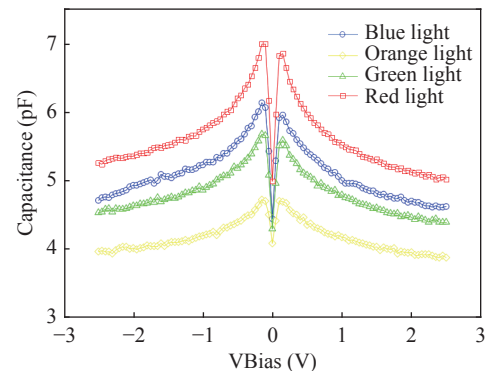

Fig. 8. The total capacitance of LCECD under different illumination.

For the electrostatic conversion characteristics of LCECD, as shown in Fig.4 and Fig.5 . For this TLP test, the entire electrostatic conversion process is 110

ns, of which a stable voltage and current can be output within 50–100 ns. The time of steady output of electric energy is determined by the time of clamping static electricity. The shorter the clamping time, the longer the device can output stable voltage and current. This clamping time reflects the response speed of the device to static electricity. The response speed is faster, the electrostatic conversion efficiency of LCECD is higher. In order to verify the relationship between the parasitic capacitance of the device and the electrostatic conversion efficiency, the device was connected in series with a 0.1 μF capacitor, and a 25 V voltage pulse was input to simulate the electrostatic pulse. Similarly, different wavelengths of light are applied to the device at the same position, and then measure the voltage waveforms of the capacitors connected in series. The test results in Fig.9 show that the charging time of the capacitor is different under different wavelengths of light. Among them, the charging speed of capacitor under orange light (wavelength 580 nm) is the fastest, followed by green light (wavelength 550 nm) and blue light (wavelength 450 nm), and the charging speed of capacitor under red light (wavelength 740 nm) is the slowest. The faster charging of the back-end capacitor means that the LCECD can respond faster. This corresponds to the parasitic capacitance of LCECD under different wavelengths of light，as shown in Fig.8 . The parasitic capacitance of LCECD is the smallest under orange light (wavelength 580 nm), and the charging speed of back-end capacitance is the fastest. The parasitic capacitance of the device under red light (wavelength 740 nm) is the largest, and the charging speed of the back-end capacitance is the slowest. In summary, when LCECD is under orange light (wavelength 580 nm), the parasitic capacitance is the smallest and the electrostatic conversion efficiency is the highest. When LCECD is under red light (wavelength 740 nm), the parasitic capacitance is the
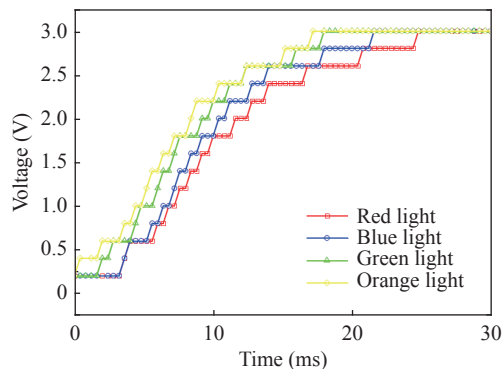
largest and the electrostatic conversion efficiency is the lowest.

IV. Conclusions

In this paper, an LCECD is designed and manufactured based on the 180 nm BCD process. In addition to converting electrostatic energy into electrical energy, the device can also change the parasitic capacitance of the device by changing the wavelength of incident light. Based on the TLP test system, the voltage clamping characteristics of the device were verified, and the feasibility of electrostatic conversion was verified by simulating static electricity with an electrostatic gun. Under illumination of different light wavelengths, the $C(V)$ characteristic of the device was measured, and then the charging waveform of the back-end capacitor was measured under different illumination wavelengths to study the influence of the LCECD capacitor on the electrostatic conversion efficiency. It is worth noting that the smaller the parasitic capacitance of the LCECD, the higher the efficiency of electrostatic conversion. This trend provides a valuable reference for the design of electrostatic conversion devices in the future.

Fig. 9. The waveform of charging the back-end capacitor after the LCECD converts static electricity under different illumination.

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