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Modeling and Measurement of 3D Solenoid Inductor Based on Through-Silicon Vias

YIN Xiangkun[1], WANG Fengjuan[2], ZHU Zhangming[1], Vasilis F. Pavlidis[3], LIU Xiaoxian[1], LU Qijun[1], LIU Yang[1], and YANG Yintang[1]

(1. *Shaanxi Key Lab. of Integrated Circuits and Systems, School of Microelectronics, Xidian University, Xi'an 710071, China*)

(2. *School of Automation and Information Engineering, Xi'an University of Technique, Xi'an 710048, China*)

(3. *Department of Computer Science, University of Manchester, Manchester M139PL, UK*)

Abstract — Through-silicon via (TSV) provides vertical interconnectivity among the stacked dies in three-dimensional integrated circuits (3D ICs) and is a promising option to minimize 3D solenoid inductors for on-chip radio-frequency applications. In this paper, a rigorous analytical inductance model of 3D solenoid inductor is proposed based on the concept of loop and partial inductance. And a series of 3D samples are fabricated on 12-in high-resistivity silicon wafer using low-cost standard CMOS-compatible process. The results of the proposed model match very well with those obtained by simulation and measurement. With this model, the inductance can be estimated accurately and efficiently over a wide range of inductor windings, TSV height, space, and pitch.

Key words — Analytical model, Solenoid inductor, Passive microwave devices, Three-dimensional integrated circuit, Through-silicon vias (TSVs), Finite element method (FEM).

I. Introduction

Three-dimensional integrated circuits (3D ICs) underpin low power and high-performance integrated systems by stacking multiple silicon layers [1]–[4]. As the critical component for 3D ICs, through-silicon vias (TSVs) provide short high aspect-ratio vertical interconnections among the stacked dies and have been greatly investigated aiming multiple applications [5]. One appealing application is the potential to produce an on-chip inductor, which is a key component in radio-frequency and microwave systems [6], [7].

Compared to conventional implementations of on-chip inductors, TSV-based solenoid inductors yield higher inductance density and can be realized with considerably less area [8]. Several investigations have been made on TSV-based solenoid inductors and the related fabrication processes are reported in [5]–[9]. Inductance models extracted by measured or simulated Y-parameters are proposed in [10]–[12]. However, these models are not rigorous and are not closely related to the physics describing the inductor. Grover formulas are convenient to estimate inductance [13], but the accuracy is limited due to the heterostructure of the TSV-based 3D solenoid inductor. Hence, a magnetostatic model used to rigorously evaluate the mutual inductance between coupled structures and parametrically analyze the solenoid inductors is required.

By approximating wire segments of the redistribution layer (RDL, metal layers deposited on top of the substrate, typically used to interconnect TSVs [1]) as cylinders, a simple model is proposed in [14]. However, this model is only suitable for the case that the RDL's width is equal to the TSV's radius. An inductance model based on trigonometric functions is proposed in [15], but this approximation underestimates the coupling between the top and bottom RDLs, thereby introduces a large error. Based on the finite element method (FEM), electromagnetic solvers such as the Ansys Q3D Extractor can obtain accurate results, but this and other similar extraction tools are intrinsically time-consuming and impractical for parametric analysis. Furthermore, the result is not intuitive and the analysis of the effect(s) of each geometric parameter on the overall be-

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havior of the inductor is not straightforward.

By computing the self- and multi- inductance formulas for four segments in each turn of 3D inductor separately, a rigorous inductance model of the solenoid inductor is developed analytically using the concept of loop and partial inductance. Compared with other methods, the proposed model is fast with computational times of about 30 ms, highly accurate with an error less than 3.7%, practical for capturing changes in the design parameters, and intuitive for parametric analysis in the design process of 3D systems.

The remainder of this paper is organized as follows. The partial and loop inductance are derived in Section II. The fabrication process flow of the solenoid inductor based on a standard CMOS process is demonstrated in Section III. The layouts, photographs, and cross sectional views of test samples are also included. Next, in Section IV, the proposed model is validated through measurements. In addition, the effect(s) of the design parameters on the inductance of TSV-based solenoid inductors are analyzed in depth. Finally, Section IV concludes this paper.

II. Analytic Model of Solenoid Inductor

In this section, a rigorous analytical inductance model of a solenoid inductor is proposed using the concept of loop and partial inductance.

The physical model of a 5-turn solenoid inductor is shown in Fig.1(a). N-loop TSV-based solenoid inductors consist of one TSV array with two rows and N columns, connected by top and bottom RDLs. The directions of the current and magnetic flux are also indicated in the Fig.1(a).

To derive a rigorous inductance expression, several steps are required as follows. Each loop can be divided into four segments: top RDL, two TSVs, and bottom RDL, as depicted in Fig.1 (b). The self-partial inductance of each segment and the mutual-partial inductance among segments are calculated by integration, respectively. The total loop inductance of an N-loop inductor is derived by adding all of the self- and mutual-partial inductances.

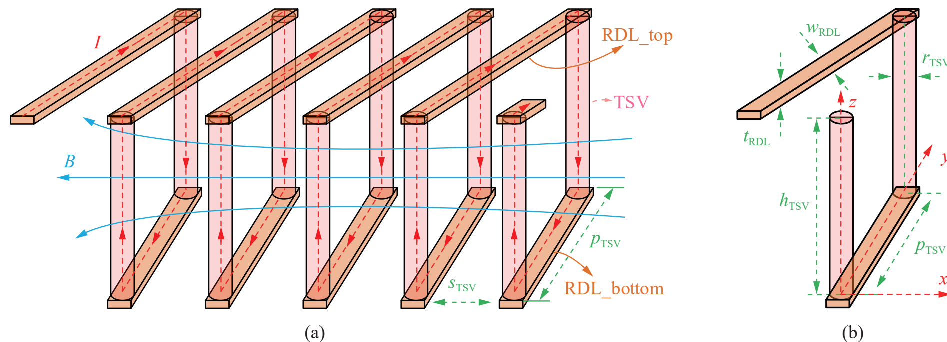

Fig. 1. Perspective view of a TSV-based solenoid inductor. (a) N-loop inductor ($N = 5$); (b) Single-loop inductor with coordinate axis and structural parameters.

1. Self-partial inductance of TSV

The coordinate system is set as shown in Fig.2. Due to the magnetostatic assumption, the current that flows in the TSV is assumed to be distributed uniformly over the wire cross section and oriented along the z-axis.

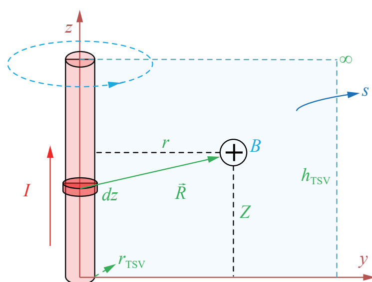

Fig. 2. Coordinate system for integrating the self-partial inductance of TSV.

According to the Biot-Savart law [16], this current segment produces a magnetic flux density B across the y-z plane, and the value of $B(r, Z)$ at the point (r, Z) can be described as (1).

$$\begin{aligned} B(r, Z) &= \frac{\mu_0 I r}{4\pi} \int_{z=0}^{h_{\mathrm{TSV}}} \frac{1}{\left[(Z-z)^2 + r^2\right]^{3/2}} dz \\ &= \frac{\mu_0 I}{4\pi r}\left[\frac{Z}{\sqrt{Z^2+r^2}} - \frac{Z-h_{\mathrm{TSV}}}{\sqrt{(Z-h_{\mathrm{TSV}})^2 + r^2}}\right] \end{aligned} \tag{1}$$

Hence the total magnetic flux through the surface s shown in Fig.2 can be derived as (2). The self-partial inductance of a single TSV can be obtained as (3). From (3), it can be seen that the self-partial inductance increases with the TSV height due to the larger integral region and decreases with the TSV radius due to the reduced magnetic flux density.

$$\psi_{\infty} = \int_{r=r_{\mathrm{TSV}}}^{\infty} \int_{Z=0}^{h_{\mathrm{TSV}}} B(r, Z) dZ dr = \frac{\mu_0 I}{4\pi} \int_{r=r_{\mathrm{TSV}}}^{\infty} \int_{Z=0}^{h_{\mathrm{TSV}}} \left[\frac{Z}{\sqrt{Z^2+r^2}} - \frac{Z-h_{\mathrm{TSV}}}{\sqrt{(Z-h_{\mathrm{TSV}})^2+r^2}} \right] dZ dr \tag{2}$$

$$Ls_{\mathrm{TSV}} = \frac{\psi_{\infty}}{I} = \frac{\mu_0 h_{\mathrm{TSV}}}{2\pi} \left[\ln\left(\frac{h_{\mathrm{TSV}}}{r_{\mathrm{TSV}}} + \sqrt{\left(\frac{h_{\mathrm{TSV}}}{r_{\mathrm{TSV}}}\right)^2+1} \right) - \sqrt{\left(\frac{r_{\mathrm{TSV}}}{h_{\mathrm{TSV}}}\right)^2+1} + \frac{r_{\mathrm{TSV}}}{h_{\mathrm{TSV}}} \right] \tag{3}$$

2. Mutual-partial inductances among TSVs

As shown in Fig.3(a), there are two kinds of mutual-partial inductances among TSVs: mutual-partial inductances among TSVs in the same row with the current flow in the same direction as depicted in Fig.3(b) and mutual-partial inductances among TSVs from different rows with the current flow in the opposite direction as depicted in Fig.3(c).

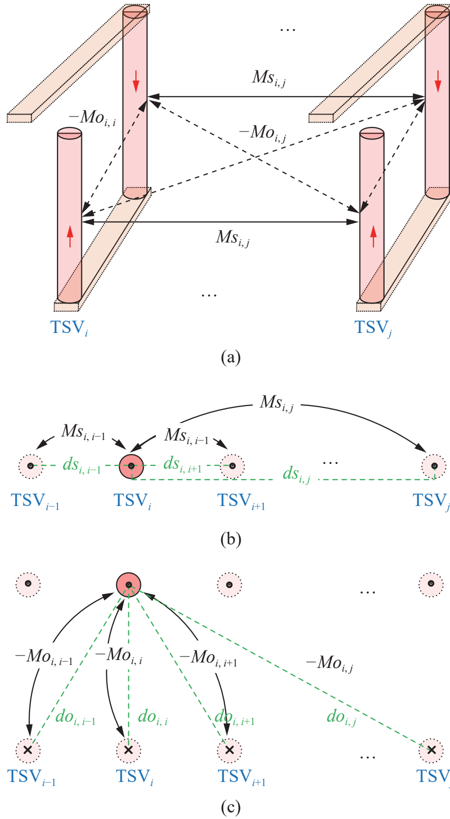

Fig. 3. Mutual-partial inductances among TSVs from (a) Both rows; (b) The same row; and (c) Different rows. The labels of points and crosses in the figures represent respectively the outward and inward current direction in the TSVs.

In both cases, the mutual-partial inductances $M_{\mathrm{TSV}}(d)$ can be derived by integration similar to (2)–(3), and are given by (4), where $d = ds_{i,j}$ or $d = do_{i,j}$ represents, respectively, the distance from the jth TSV to the ith TSV in the same row or different rows and is written as (5) and (6).

$$\begin{aligned} M_{\mathrm{TSV}}(d) &= \frac{\mu_0 h_{\mathrm{TSV}}}{2\pi} \left[\ln\left(\frac{h_{\mathrm{TSV}}}{r_{\mathrm{TSV}}+d} + \sqrt{\left(\frac{h_{\mathrm{TSV}}}{r_{\mathrm{TSV}}+d}\right)^2+1} \right) \right. \\ &\quad \left. - \sqrt{\left(\frac{r_{\mathrm{TSV}}+d}{h_{\mathrm{TSV}}}\right)^2+1} + \frac{r_{\mathrm{TSV}}+d}{h_{\mathrm{TSV}}} \right] \end{aligned} \tag{4}$$

$$ds_{i,j} = |i-j|\, s_{\mathrm{TSV}} \tag{5}$$

$$do_{i,j} = \sqrt{{p_{\mathrm{TSV}}}^2 + (i-j)^2 {s_{\mathrm{TSV}}}^2} \tag{6}$$

Hence, the mutual-partial inductances between the TSVs are $Ms_{i,j} = M_{\mathrm{TSV}}(ds_{i,j})$ if the TSVs belong to the same row and $Mo_{i,j} = M_{\mathrm{TSV}}(do_{i,j})$ if the TSVs belong to different rows, respectively.

Note that the mutual-partial inductances among TSVs from different rows are negative due to the opposite current directions. Particularly, a special case is encountered if $i = j$ in (5) where the ith and jth TSV represent the same TSV. In this case, the result obtained by substituting (5) into (4) is identical to that of (3). Both types of mutual-partial inductances decrease with the TSV distances as described in (4)–(6), which suggests that in order to increase the total inductance for the same chip area, a larger pitch of TSVs among different rows (labeled as p_{TSV} in Fig.1) and smaller space of TSVs of the same row (labeled as s_{TSV} in Fig.1) are preferred.

3. Self-partial inductances and mutual-partial inductances among RDLs

As shown in Fig.4(a), similar to the integration in Section II.2, there are three types of mutual-partial inductances among RDL wires: the mutual-partial inductances among bottom RDL segments ($Mb_{i,j}$), with the flow of currents in the same direction; the mutual-partial inductances among top RDL segments ($Mt_{i,j}$), with the flow of currents in the same direction; and the mutual-partial inductances among segments from both the top and bottom RDLs ($-Mc_{i,j}$), with the flow of currents in the opposite directions.

Similar to the integration in Section II.2, the mutual-partial inductances between centers of parallel RDL segments can be given as (7), where l_{RDL} notates the length of the RDL wire and d denotes the distance between two RDL wire segments.

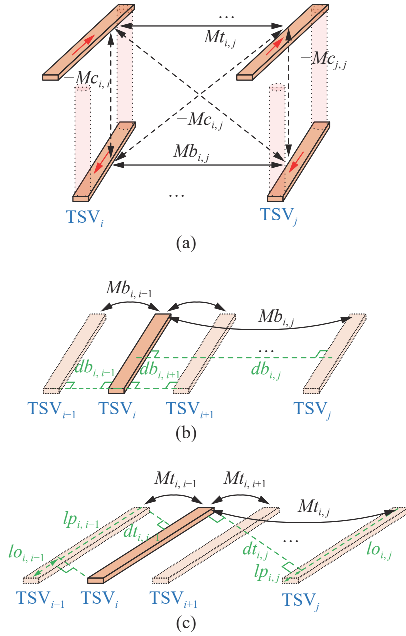

Fig. 4. Mutual-partial inductances among (a) All the RDLs, (b) Bottom RDLs, and (c) Top RDLs.

For the case of bottom RDL wires as shown in Fig.4(b), by substituting (8) into (7), the mutual-partial inductance can be obtained as $Mb_{i,j} = M_{\rm RDL}(p_{\rm TSV}, db_{i,j})$, where the distance between bottom RDL wire segments $db_{i,j}$ is described as (8).

$$M_{\rm RDL}(l_{\rm RDL}, d) = \frac{\mu_0}{2\pi}\left[l_{\rm RDL}\ln\left(\frac{l_{\rm RDL}}{d}+\sqrt{\left(\frac{l_{\rm RDL}}{d}\right)^2+1}\right) - \sqrt{l_{\rm RDL}{}^2+d^2}+d\right] \tag{7}$$

$$db_{i,j} = \begin{cases} |i-j|\, s_{\rm TSV}, & i\neq j \\ 0.5w_{\rm RDL}, & i=j \end{cases} \tag{8}$$

The mutual-partial inductances between top and bottom RDLs can also be approximately evaluated by substituting (9) into (7), leading to $Mc_{i,j} = M_{\rm RDL}(p_{\rm TSV}, dc_{i,j})$, with the sign being negative due to the opposite current directions. Here, the distance is written as (9).

$$dc_{i,j} = \sqrt{[(|i-j|+0.5)\, s_{\rm TSV}]^2 + h_{\rm TSV}{}^2} \tag{9}$$

For the case of top RDL wire segments as shown in Fig.4(c), the calculation is more complicated and their endpoints are offset by length $lo_{i,j}$, parallel length $lp_{i,j}$, and perpendicular distance $dt_{i,j}$ can be decreased as (10), (11), and (12).

$$lo_{i,j} = \min\left[\frac{|i-j|\, s_{\rm TSV}{}^2}{\sqrt{s_{\rm TSV}{}^2+p_{\rm TSV}{}^2}}, \sqrt{s_{\rm TSV}{}^2+p_{\rm TSV}{}^2}\right] \tag{10}$$

$$lp_{i,j} = \sqrt{s_{\rm TSV}{}^2+p_{\rm TSV}{}^2} - lo_{i,j} \tag{11}$$

$$dt_{i,j} = \begin{cases} \dfrac{|i-j|\, s_{\rm TSV} p_{\rm TSV}}{\sqrt{s_{\rm TSV}{}^2+p_{\rm TSV}{}^2}}, & i\neq j \\ 0.5w_{\rm RDL}, & i=j \end{cases} \tag{12}$$

According to the theory of partial inductance with offset [16], the mutual-partial inductances (between segments in the top RDLs) from the jth RDL to the ith RDL are determined by substituting (10)–(12) into (7), which can be written as (13).

$$Mt_{i,j} = \frac{1}{2}\left[M_{\rm RDL}\left(lp_{i,j}+2lo, dt_{i,j}\right)+M_{\rm RDL}\left(lp_{i,j}, dt_{i,j}\right)\right] - M_{\rm RDL}\left(lo_{i,j}, dt_{i,j}\right) \tag{13}$$

Note that, when $i=j$, the self-partial inductances of bottom and top RDL segments $Lb_{\rm RDL} = M_{\rm RDL}(p_{\rm TSV}, db_{i,j})$ and $Lt_{\rm RDL} = M_{\rm RDL}(lp_{i,j}, db_{i,j})$ are determined through (7)−(12).

Due to the similar distance and length, the mutual-partial inductances of wire segments located both either at the top and bottom RDL are approximately equal and contribute considerably to the total inductance of the solenoid inductor. In contrast, the inductance between wire segments located, respectively, either at the top and bottom RDL or, vice versa, $Mc_{i,j}$ is negative and has a weak contribution to the total inductance due to the long distance between the top and bottom RDLs, as described by (9).

The current flow in TSVs is orthogonal to that in the RDLs and yields identically zero scalar product. Consequently, the mutual-partial inductances between TSVs and RDLs are zero according to the Neumann formula [17].

4. Total loop inductance of *N*-loop inductor

According to the theory of loop inductance, the inductance is produced by the magnetic flux, and the total inductance of inductor loop is the sum of external inductance and internal inductance. In the TSV-based 3D inductor, the external inductance due to the magnetic flux external to the wires has been derived as the sum of these self- and mutual-partial inductances.

And the internal inductance can be evaluated as $L_{Int} = \mu_0 l/(8\pi)$. μ_0 is the permeability of the surrounding medium, and l is the length of TSV and RDL, respectively. Usually, this is inconsequential compared to the external inductance. Specially, the dimension of the wire is several tens of microns in the TSV-based 3D inductor, the DC internal inductance is less than 10^{-4} nH, which is negligible compared with the external inductances.

The total loop inductance of an N-loop inductor is written as (14), which is the sum of these self- and mu-

tual-partial inductances derived through (3), (4), (7), and (13), and all the internal inductances of TSVs and RDLs.

$$\begin{aligned} &L_{\text{TOTAL}} \\ &= 2\left(N\cdot Ls_{\text{TSV}}+\sum_{i=1}^{N}\sum_{j=1,j\neq i}^{N}Ms_{i,j}-\sum_{i=1}^{N}\sum_{j=1}^{N}Mo_{i,j}\right) \\ &\quad +N\left(Lb_{\text{RDL}}+Lt_{\text{RDL}}\right)+2\sum_{i=1}^{N}\sum_{j=1,j\neq i}^{N}\left(Mb_{i,j}+Mt_{i,j}\right) \\ &\quad -2\sum_{i=1}^{N}\sum_{j=1}^{N}Mc_{i,j}+N\left(2L_{\text{Int,TSV}}+L_{\text{Int},t\text{RDL}}+L_{\text{Int},b\text{RDL}}\right) \end{aligned} \tag{14}$$

III. Fabrication Process of the Solenoid Inductor

The fabrication process flow of the solenoid inductor within a low-cost standard CMOS process is shown Fig.5. The photographs of the inductor layers corresponding to the process steps are depicted in Fig.6. High resistivity silicon with dielectric constant of 11.9 and resistivity 1 kΩ·cm is employed as the substrate material to reduce the high-frequency magnetic loss induced by eddy currents and polarization in the substrate [18]–[23].

The process steps are as follows:

Step 1: As shown in Fig.5 (a), the fabrication begins with a deep reactive ion etching (DRIE) process to make fine silicon vias with depth of 100 μm, and the corresponding photograph is depicted in Fig.6(a).

Step 2: SiO_2 liner is formed by chemical vapor deposition (CVD) process to isolate the TSV metal from the substrate, as depicted in Fig.5(b).

Step 3: The via is filled by copper plug fabricated by depositing an iPVD copper seed first and subsequently electroplating a copper plug as illustrated in Fig.5(c).

Step 4: After these process steps, the backside metal wiring levels are developed utilizing standard copper damascene process to pattern the RDL_{bot} which interconnects the TSVs, as the process step depicted in Fig.5(d) and the corresponding photograph shown in Fig.6(b). Note that the RDL_{bot} is formed by five separated metal lines and each of these layers interconnects the bottom ends of two TSVs.

Step 5: After surface passivation, the wafer is flipped and bonded to a carrier die or wafer using thermal compression bonding. The backside of the silicon substrate is then thinned to 100 μm thickness, so as to expose the TSVs, per the process step shown in Fig.5(e).

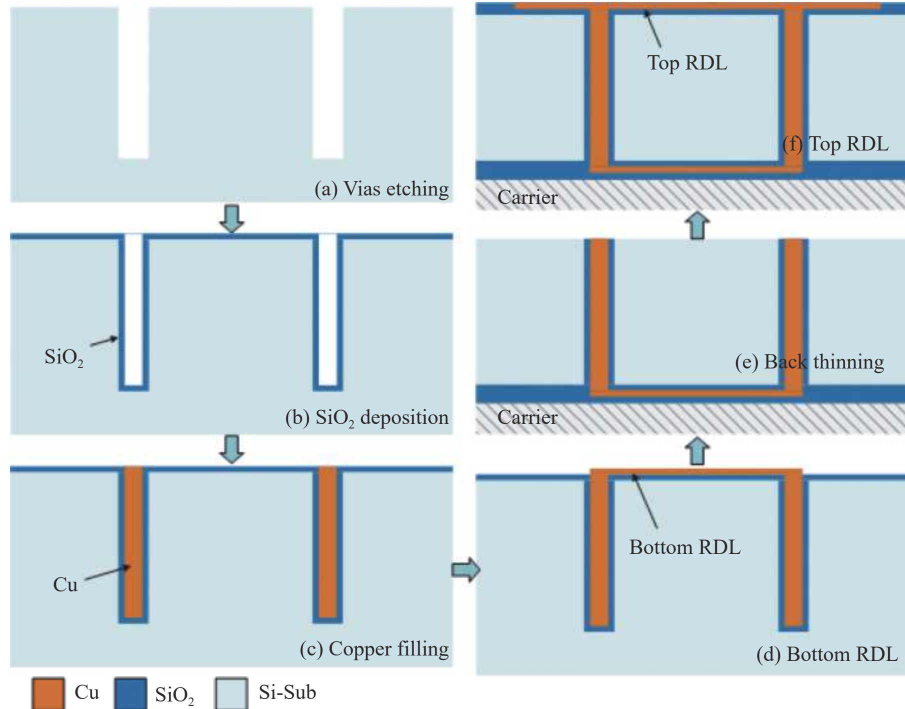

Fig. 5. Fabrication process flow for solenoid inductor. (a) Vias etching (by deep reactive ion etching process); (b) Vias filling with SiO_2 liner (by chemical vapor deposition process); (c) Vias filling with metal plug (by depositing an iPVD copper seed first and then electroplating a copper plug); (d) Pattern the bottom RDL (RDL_{bot}) which interconnects the TSVs (by standard copper damascene process); (e) Wafer flipping and back thinning; (f) Pattern the top RDL (RDL_{top}) which interconnects the TSVs and input/output ports (by standard copper damascene process).

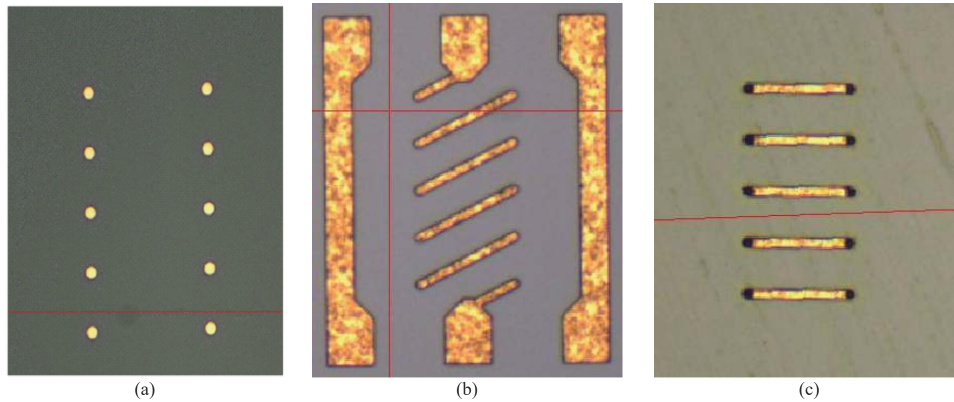

Fig. 6. Photographs of inductor layers. (a) TSVs; (b) RDL_{top}; (c) RDL_{bot}.

Step 6: This step includes several tasks similar to the backside metal wiring processes. A planarization oxide is deposited followed by a damascene process to pattern RDL_{bot}, as the process step depicted in Fig.5(f) and the corresponding photograph is shown in Fig.6(c). Similar to RDL_{bot}, RDL_{top} is formed by six separate metal lines, which act as the input/output ports and interconnect the top terminals of TSVs.

Following the above procedure, a series of test samples of TSV-based solenoid inductors with different design parameters are fabricated.

In order to validate the rigor of the inductance model and analyze the influence of each geometric parameter on the design process of 3D inductors, various geometric parameter combinations are considered. The number of inductor turns is varied from 1 to 10. Scanning electron microphotograph (SEM) photographs of the cross-section of a 5-turn inductor is shown in Fig.7(a) as a sample of the diverse manufactured prototype inductors.

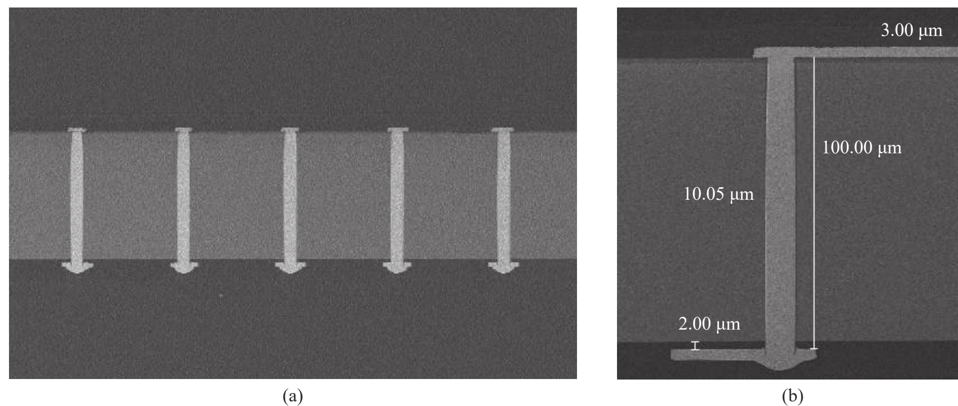

Fig. 7. SEM photos of a solenoid inductor. (a) Cross view; (b) Parameters.

Considering the present 3D TSV technology, the design parameters adopted in this work are defined as follows. As depicted in Fig.7(b), the height and radius of the TSVs are set to 100 μm and 5 μm, respectively. The thickness and width of the RDLs is 3 μm and 10 μm, respectively.

IV. Measurement and Validation

In this section, the proposed model is validated through measurements. Additionally, the effect of design parameters on the inductance of TSV-based solenoid inductors is analyzed and the accuracy of the proposed analytic model is validated.

1. Measurement

To verify the derived model, each sample of the fabricated inductors is packaged in a test structure as the layer depicted in Fig.6 (b). The input and output ports of the test structure are each formed by 3 pads with ground-signal-ground (GSG) mode. Hypotenuse is designed at the interfaces between the sample core and test pad to reduce the reflection loss. The S-parameters of the fabricated solenoid inductors with different design parameters are measured using an Agilent N5244A vector network analyzer (VNA) and probes Model 50A DS style with 250 μm GSG pitch calibrated on a reference kit.

2. Open-short de-embedding method

The transition and test pads in the signal path affect the measured results of S-parameters. In order to remove this effect and accurately capture the characteristics of the solenoid inductor, the parasitic elements induced by the test structure are evaluated and removed from the measured results using an open-short de-embedding method [20], [21], [24].

The net Y-parameters of the solenoid inductor are derived as (15).

$$Y_{\text{net}} = \left((Y_{\text{DUT}} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1}\right)^{-1} \quad (15)$$

where Y_{DUT}, Y_{open} and Y_{short} denote the Y-parameter matrices and correspond to the DUT, open and shorted structures, respectively. Based on the de-embedding calibration using the open/short structures, the impacts of parasitic and coupling effects from the adjacent components, bonding wire and package are canceled from the measurement results.

3. Model validation and discussion

Based on the de-embedded Y-parameters derived from (15), the inductance of the solenoid inductor can be determined by (16).

$$L = \text{Im}\,(1/Y_{11})/2\pi f \quad (16)$$

As shown in Fig.8, the inductances derived from measured S-parameters varies with the frequency, and the self-resonant frequencies (SRFs) of the inductors are larger than 10 GHz. In the case that the frequency is much less than SRF, the inductances calculated from the measured S-parameters are changed slightly with signal frequency. In order to verify the derived model, the measurement inductance results at 1 GHz (less than SRF/10) are selected as the reference, the maximum of the deviations is less than 1%.

The quality factor can be expressed by (17). As shown in Fig.8(b), the maximums of Q for the six cases are respectively 17.6, 19.9, 21.9, 24.8, 26.7, and 26.8.

$$Q = \text{Im}\,(1/Y_{11})\,/\text{Re}\,(1/Y_{11}) \quad (17)$$

The total loop inductance results with different TSV space, pitch, and number of turns obtained from the model and measurements are plotted in Fig.9. The comparison reveals good match between the results of the proposed model and the measurement over several design parameters. As demonstrated in the comparison, all the inductance values determined by the proposed model agree very well with the measured results and the error ranges from −2.89% to 3.43%, verifying the accuracy of the proposed model.

The slight differences between the measured and calculated results are due to the non-ideal factors in practical measurements. The analytical model in this paper assumes an ideal physical structure for the inductor. However, there are some non-ideal factors in practical measurements. Examples of these non-idealities include the non-uniform thickness of RDLs, the non-uniform doping concentration of the silicon substrate, the roughness of the TSV surface, and the mismatch of the TSV radius and pitch [22]. In addition, the parasitic parameters of instruments, probes, and pads can also affect the measured inductance. However, the error between the measured and calculated results is less than 3.7% across a variety of combinations of geometric parameters.

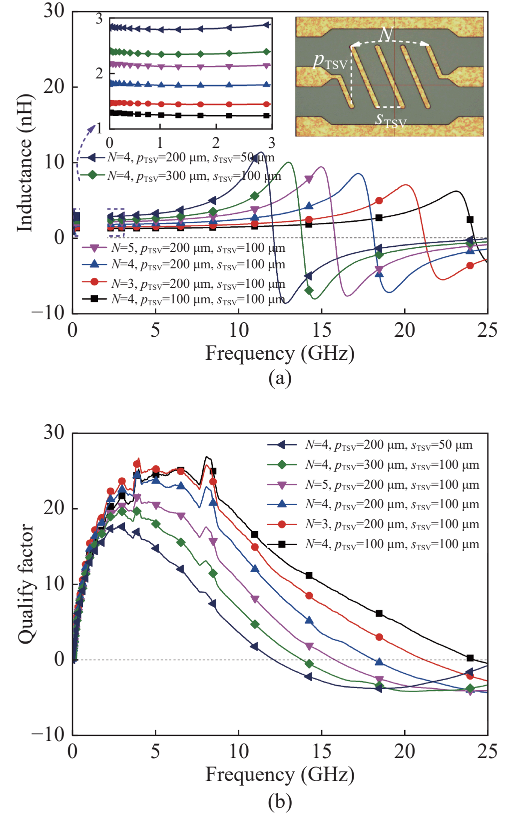

Fig. 8. The extracted parameters derived from measured S-parameters. (a) Inductances; (b) Qualify factors.

The total loop inductance of the solenoid inductor increases slightly with the TSV space as shown in Fig.9(a). In the case of large s_{TSV}, the total loop inductance approximately follows a linear relationship with the number of turns. Alternatively, the total loop inductance exhibits super-linear variation with the number of turns in the case of spacing smaller than 300 μm. The reason is that larger TSV space decreases the mutual-partial inductance among TSVs within the same row, but increases the wire segments in the same RDL layer. The current flows along the same direction for these TSVs and RDL wire segments according to (4)−(9). In extreme conditions where the space is large enough lead-

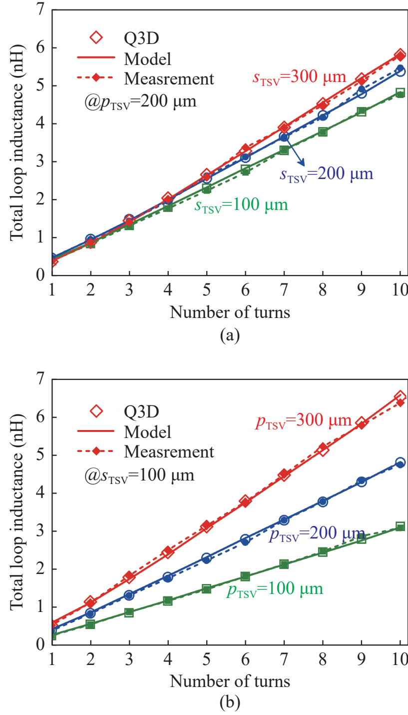

Fig. 9. Comparison of total loop inductance between analytical model and measurements with (a) TSV space ($s_{\rm TSV}$) and inductor turns ($@h_{\rm TSV}=100$, $p_{\rm TSV}=200$ µm); (b) TSV pitch ($p_{\rm TSV}$) and inductor turns ($@h_{\rm TSV}=100$ µm, $s_{\rm TSV}=100$ µm).

ing to negligible mutual-partial inductances, the total loop inductance approximately equals the summation of all the self-partial inductances.

As shown in Fig.9(b), the inductance increases significantly with$p_{\rm TSV}$. The reason is that the negative mutual-partial inductances between TSVs from different rows decrease with $p_{\rm TSV}$. For these TSVs, the current flows in the opposite direction, according to (4) and (6). The length of the RDL wire segments increases with $p_{\rm TSV}$, thus the mutual-partial inductance of the RDL segments and the total loop inductance increase according to (7)−(14).

Also, the observations and results relating to Fig.9 also offer insight in the design process of TSV-based inductors. To obtain a larger inductance density, the designer should increase the distance of currents along the same direction, and decrease the distance of currents along the different directions. That is to say, the design solution with large TSV pitch and small TSV space will obtain an optimal inductance in the same chip area. For fast estimation, to design a 3D inductor with 2 nH inductance, the footprint is 0.0125 mm^2, and the size could be further reduced with a larger TSV height.

With the explicit formulae as listed in (3), (4), (7), (9), (13), and (14), this model can determine inductance fast and effectively by just substituting the design parameters into the formulae. Furthermore, the inductance model is intuitive to explore the influence of each geometric parameter on the behavior of the 3D inductor.

4. Comparison with related work

A first-order model for TSV-based inductors has been proposed in [14]. In this model, the RDL wire segments are approximated as cylinders with radius equal to half of the RDL width. These approximations, however, lead to three sources of error. The first error is the calculation of the RDL length without distinguishing the offset and parallel length, as described by (10) and (11), which underestimates the mutual inductance of the top RDL wire segments ($Mt_{i,j}$). The second error is that the approximation of RDL wire segments as cylinders enlarges the conductor surface and decreases the distance between the conductors, which underestimates the mutual inductance of the bottom RDL wire segments ($Mb_{i,j}$). The third error is that the cylinder approximation decreases the distance between the top and bottom RDLs, thereby overestimating the mutual inductance between the metal layers ($Mc_{i,j}$). Note that all the three errors collectively underestimate of the total inductance of the TSV-based 3D inductor.

Another inductance model based on trigonometric functions is proposed in [15]. In this model, the mutual inductance between the metal layers is calculated with Grover formulas. However, the distance between two RDLs in different rows is overestimated. As the magnitude of the mutual inductance is in principle, inversely, proportional to the distance between the coupled RDLs, this model underestimates the effect of negative coupling and overestimates the total loop inductance.

In order to demonstrate this point further, the results of RDL inductance with varying RDL width are compared by the different methods as depicted in Fig.10. In this figure, the results from the proposed model, the Q3D extractor, and the referred papers are labeled as "Model," "Q3D," "[14]," and "[15]," respectively. In both cases of the RDL width, the proposed inductance model agrees very well with the results by the Q3D extractor. On the contrary, the error of the referred works changes with the RDL width, which affects the accuracy of the evaluated inductance.

The error in the total loop inductance derived from different models where the number of turn ranges from 1 to 10 is shown in Fig.11 and is determined by

$$\text{Error}=\frac{L_{\rm Modeled}-L_{\rm Measured}}{L_{\rm Measured}}\times 100\% \tag{18}$$

Note that all the errors change with the number of turns. Model in [14] exhibits the largest fluctuation from 9.1% to −4.2%. Model in [15] demonstrates a vari-

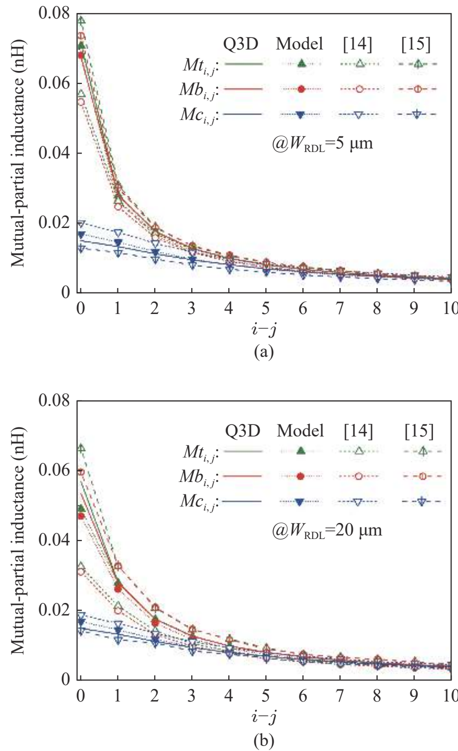

Fig. 10. Modeled results of RDL inductance with varying RDL segment width. i and j represent the RDL positions, $i-j=0$ denotes the self-inductance of a single RDL (@$h_{\mathrm{TSV}}=100$ μm, $p_{\mathrm{TSV}}=200$ μm, $s_{\mathrm{TSV}}=100$ μm).

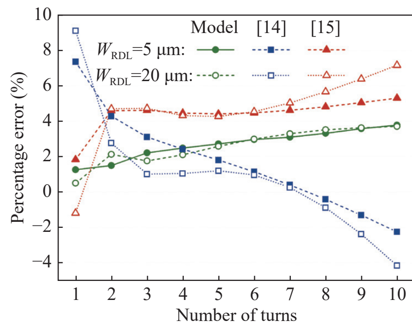

Fig. 11. Comparison of errors of total loop inductance derived from different models with turn number (@$h_{\mathrm{TSV}}=100$ μm, $p_{\mathrm{TSV}}=200$ μm, $s_{\mathrm{TSV}}=100$ μm).

ation from 1.7% to 7.6%. Alternatively, the proposed model in this work exhibits the lowest fluctuation, ranging from 0.5% to 3.7%, and the highest accuracy. Furthermore, due to the approximation used in [14] and [15], the RDL width affects the error of both models, but does not affect the accuracy of the proposed model. These results demonstrate the superiority and versatility of the proposed model across several structural and design parameters compared to the state-of-the-art works.

V. Conclusions

Based on the concept of loop and partial inductances, a rigorous analytical inductance model for TSV-based solenoid inductors is proposed. A series of test samples of TSV-based solenoid inductors with different design parameters are fabricated within a standard CMOS process and measured to validate the accuracy of the model. Measurement results for these diverse test cases verify the accuracy of the proposed model. The model offers a more accurate estimation of the inductance for different number of turns, TSV height, TSV space, and pitch over the prior art.

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YIN Xiangkun was born in Hunan Province, China. He received the Ph.D. degree from Xidian University in 2017. He is currently an Associate Research Fellow with the School of Microelectronics, Xidian University. His current research interests include 3D ICs based on the TSVs and high-performance RF/Microwave circuits.
(Email: yinxkcn@163.com)

WANG Fengjuan (corresponding author) received the Ph.D. degree from Xidian University in 2014. She is currently a Professor with the School of Automation and Information Engineering, Xi'an University of Technology. Her research interests include TSV-based integrated passive device and 3D ICs. (Email: wfjxiao4@163.com)

ZHU Zhangming received the Ph.D. degree from Xidian University in 2004. He is currently a Professor with the School of Microelectronics, Xidian University. His current research interests include low power mixed-signal integrated circuits, high speed ADC/DAC, green-power power ICs, and 3D ICs based on the TSVs. (Email: zmyh@263.net)

Vasilis F. Pavlidis received the Ph.D. degree from University of Rochester in 2008. He is now an Assistant Professor with the School of Computer Science, University of Manchester. His current research interests include interconnect modeling and design, 3D integration, networks-on-chip.
(Email: pavlidis@cs.man.ac.uk)

LIU Xiaoxian received the Ph.D degree in 2015. She is currently an Associate Professor with the School of Microelectronics, Xidian University. Her current research interests focus on the microwave integration for high-speed 3D ICs based on the TSV technology.
(Email: liudou132@163.com)

LU Qijun received the Ph.D degree in microelectronics from Xidian University in 2015. He is currently an Associate Professor with the School of Microelectronics, Xidian University. His current research interests include high performance 3D ICs based on the TSVs.
(Email: luqijun2000@126.com)

LIU Yang received the Ph.D degree from Xidian University in 2017. She is currently an Associate Professor with the school of Microelectronics, Xidian University. Her current research interests include design, modeling, and simulation of through-silicon via-based 3D ICs. (Email: lliu_yang@163.com)

YANG Yintang received the Ph.D. degree from Xidian University. He is currently the vice president of Xidian University, and a Professor with the School of Microelectronics at Xidian University. His current research interests include high-speed data converters, 3D ICs, network-on-chip, and new semiconductor devices. (Email: ytyang@xidian.edu.cn)