

NGD Analysis of Defected Ground and SIW-Matched Structure

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Abstract — A bandpass negative group delay (NGD) passive circuit based on defect ground structure (DGS) and substrate integrated waveguide (SIW)-matched is developed in the paper. The NGD DGS topology is originally built with notched cells associated with self-matched substrate waveguide elements. The DGS design method is introduced as a function of the geometrical notched and SIW via elements. Then, parametric analyses based on full wave 3-D electromagnetic *S*-parameter simulations were considered to investigate the influence of DGS physical size effects. The design method feasibility study is validated with fully distributed microstrip circuit prototype. Significant bandpass NGD function performances were validated with 3-D simulations and measurements with -1.69 ns negative group delay value around 2 GHz center frequency over 33.7 MHz NGD bandwidth. Insertion loss is 4.37 dB, and reflection loss reaches 41.5 dB.

Key words — Defected ground structure (DGS), Microwave circuit design method, Bandpass negative group delay (BP NGD) function, Experimentation, Microstrip circuit, Substrate integrated waveguide (SIW).

I. Introduction

Following the traditional method to increase the electronic and electrical system performance consists in the integration density increase and size shrinking. However, the electronic system confinement is naturally penalized by the electromagnetic compatibility (EMC) and interference (EMI) undesirable effects [1]–[4]. Against the undesirable printed circuit board (PCB) EMI and EMC problems, different geometrical solutions were deployed. Research work on EMC and EMI design is permanently ongoing against this technical

electronic and electrical system design challenge. Based on the EMI field-circuit simulation, an optimization design of vehicle navigation system was introduced [1].

To predict these EMC and EMI effects, PCB level computation tools were investigated [2]. Computerized [3] and full-wave [4] simulations in EMC PCB level were proposed. The costs of the EMC and EMI issues constitute a major breakthrough for the PCB manufacturers. Therefore, the electronic PCB designers are continuously looking for the best technical solution without increasing the cost. And also, to alleviate the PCB EMIs, the proposal solution must guarantee that the design level of complexity does not increasing.

Among these solutions, our attention is bibliographically attracted to the deontological electronic ones consisting in modifying the paths of return current propagating through the ground plane. Such solutions were currently assigned as the defected ground structure (DGS) EMI reduction solutions [5]–[8]. This relevant and costless EMI solution candidate is generally applied to microstrip circuit designs. The DGS design solution is particularly efficient to suppress PCB level EM crosstalk [5]–[8]. An innovative DGS approach using irregularly-spaced vias connecting the PCB traces over a slotted ground plane is proposed in [5]. The effectiveness of the DGS solution was verified to reduce radio frequencies and broadband EMIs from active PCBs [6], [7]. The effectiveness of crosstalk suppression was validated from mode mismatch between spoof SPP microstrip transmission line (TL) [8]. In a high-speed (HS) PCBs, the effectiveness of DGS solution was demonstrated to mitigate simultaneous switch-

ing noise (SSN) and EMI reduction in [9].

Moreover, in addition to the EMI effect cancellation, the enormous sleeping potential of DGS need to be explored by the EMC, signal integrity (SI), RF and microwave design researchers. Under such a circumstance, we can point out that the DGS enables also to enhance the signal integrity (SI) performances [10], [11] and suppression of microwave device harmonics [12]. In more general review, the DGS constitutes one of promising design solution and miniaturization minimizing the EMIs of various microwave passive circuits [12]–[22]. Because of these technical benefits, the DGSs have been extensively exploited to design microwave circuits. For example, the DGS circuits have an outstanding potential of integrability in different microwave devices as power dividers/combiners [12], filters [13]–[16], EMI filtering [17], EMC/EMI power electronics [18], [19], and antennas [20]. The extension of certain electronic function can also be exploited with the control of DGS parameters. By designing DGS resonator, a tunable band stop circuit was implemented by using reconfigurable dumbbell-shaped coplanar waveguide [21].

In addition to these classical microwave function designs, the DGS was also exploited to design the unfamiliar bandpass negative group delay function. It was found that the defected microstrip structures enable to design dual-band NGD circuits (NGDCs) operating between 3.46–3.58 GHz and 5.10–5.20 GHz [22]. Furthermore, compact NGD microstrip passive circuits with DGSs were designed [23]–[25]. However, the bandpass (BP) NGD performances of existing DGS microwave circuits are susceptible to be improved by playing on their geometry. For this reason, a novel design of DGS via elements is proposed in this paper by means of notched elements combined with substrate integrated waveguide.

Before the paper outline, it is worth briefly introducing the state-of-the-art on the BP NGD microstrip circuits. For its intriguing counterintuitive phenomenon, the NGD existence was one of controversial topics for many microwave design researchers. The BP NGD function was understood in early 2000 s with split ring resonator (SRR) based negative refractive index (NRI) metamaterial structure [26], [27]. However, the NGD passive circuits were initially present more than 20 dB losses with important physical sizes [26], [27]. Therefore, few research teams around the world were curiously attracted to the low cost and compact NGD circuit design in order to overcome this technical bottleneck. One of the helpful basic NGD theory enabling to understand in easier way the design method was introduced by considering the Kramer-Koenig analogy between the linear

circuit transfer function magnitude and group delay (GD). Subsequently, the concept of bandpass negative group delay function was defined and verified with all microwave NGD circuits. An interesting microwave engineering was revealed on the fact that the BP NGD function can be designed with unlimited diverse topologies. The study, design and test of diverse NGD microwave topologies are still an open research area for future engineers for the three following decades. For example, the BP NGD function was verified with absorptive bandstop filter [28], microwave signal interference technique [29], microwave transversal filter approach [30] and TL based microstrip circuits [31]–[34]. Innumerable topologies of microstrip NGD circuits (NGDCs) [22]–[35] were deployed in order to reduce to reach competitive compactness's.

Behind this progressive NGD design investigation, further research works were required about the design of NGD microwave circuits by illustrating the adequate characterization techniques required by microwave standards. The novelty of the present paper compared to the NGD research work available in the literature [22]–[35] is the design consideration of substrate waveguide via and the circuit compactness. The substrate waveguide was exploited to design classical microwave function as filters [36], [37], and a review considering wireless applications from DGS was given in [38]. Based on the authors' knowledge the present paper is the first-time research on the design of compact NGD circuit.

The paper consists of four main sections. Section II describes the key fundamental definition and design methodology to familiarize to the BP NGD passive circuit design. Section III is focused on the design application of DGS-SIW circuit. The feasibility of the NGD design is investigated with parametric analyses with regard to the DGS notched element physical sizes. Section IV will validate the DGS NGD topology with experimentation of microstrip prototype. Then, Section V ends the paper with a conclusion.

II. Theoretical Specifications of BP NGD Performance

This present section defines BP NGD function key specifications. The qualification of NGD performance will be defined from two-port circuit S -parameters. Then, the design methodology for NGD passive distributed circuit will be elaborated.

1. Theoretical recall on GD parameter

The two-port system of Fig.1 represents a circuit black box. The present case of study associates the two-port symmetric microwave passive circuits.

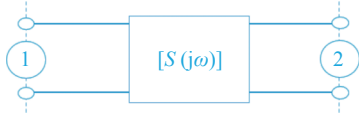


Fig. 1. Two-port black box system.

They can be theoretical modeled by an equivalent 2-D S -matrix written as

$$[S(j\omega)] = \begin{bmatrix} S_{11}(j\omega) & S_{21}(j\omega) \\ S_{21}(j\omega) & S_{11}(j\omega) \end{bmatrix} \quad (1)$$

where $j\omega$ is the complex angular frequency variable.

The transmission coefficient phase is given by

$$\varphi(\omega) = \arg [S_{21}(j\omega)] \quad (2)$$

The specific parameter of the present study is expressed by the GD mathematically defined by

$$GD(\omega) = \frac{-\partial\varphi(\omega)}{\partial\omega} \quad (3)$$

For the case of BP NGD function, the equation:

$$GD(\omega) = 0 \quad (4)$$

should present two roots, ω_1 and ω_2 , (we take $\omega_1 < \omega_2$), which are named NGD cut-off frequencies.

2. Ideal specifications of BP NGD response

By analogy with all microwave function, the NGD one should be targeted to operate at specific NGD center frequency, ω_0 as introduced in Fig.2.

In the NGD bandwidth, $\omega_1 < \omega < \omega_2$, given the desired values of positive reals, $A < 1$ and $B < 1$, the essential parameters of BP NGD function are as follows:

- The reflection coefficient, $S_{11} = A$, as seen in Fig.2(a);
- The transmission coefficient, $S_{21} = B$, as illustrated in Fig.2(b);
- And as depicted in Fig.2 (c), the NGD value, $GD(\omega) = GD_0 < 0$;

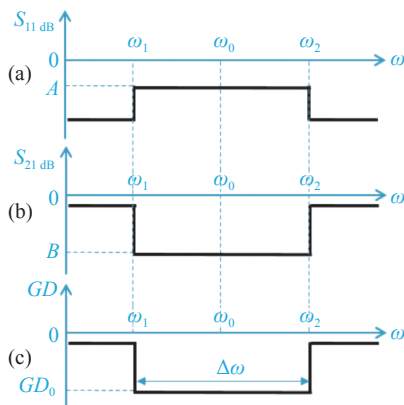


Fig. 2. Typical behaviors of BP NGD S -parameters. (a) Reflection; (b) Transmission coefficients; and (c) GD.

- Over the NGD bandwidth:

$$\Delta\omega = \omega_2 - \omega_1 \quad (5)$$

3. Design methodology of BP NGD circuit

The BP NGD circuit design method is actually similar to classical RF and microwave circuits (filters, phase shifters, power dividers,...). The design can be organized in different successive phases. The principal design phases can be described as follows:

- Phase 1: As mentioned in the previous section, the design process must start with the required BP NGD specifications.
- Phase 2: Define the desired minimum and maximum ranges of physical parameters.
- Phase 3: After the 3-D circuit design of the negative group delay topological structure, the physical sizes of the structure (widths, lengths, interspaces,...) should be optimized.
- Phase 4: The final design of BP NGD circuit should be carried out after manufacturing.
- Phase 5: Conduct the NGD behavior frequency domain validation tests of the prototype.

III. DGS Circuit Designing and Parametric Analyses with Respect to the Notched Element Physical Sizes

This section is focused on the design description of notched element based DGS BP NGD circuit. The NGD circuit based on DGS acts as a two-port passive circuit. Parametric analyses of GD and S -parameters will be discussed. All the computational results presented in this paper were obtained from 3-D electromagnetic full wave simulations. The present simulated results were run in the commercial tool environment of the microwave simulator HFSS® from ANSYS® Electromagnetics Suite 19.0.0 which operates with Solver Finite Element Method. The employed PC is equipped with a single-core processor Intel® Core™ Intel(R) Core(TM) i5-8400 CPU @2.80 GHz 2.81 GHz and 16 GB physical RAM with 64-bits Windows 7.

1. Design of notched element based DGS circuit

Following the design flow elaborated in Fig.2, the present subsection investigates the geometrical implementation of our DGS NGD proof-of-concept (POC) circuit. The group delay specifications targeted for the present circuit design are addressed in Table 1. The POC DGS is mainly designed in microstrip topology by using a direct TL. Fig.3 introduce the planar design of microstrip circuit geometrically designed with width, W , and length, L . The circuit is essentially composed of distributed elements without lumped element. As seen in top view of Fig.3(a), the microstrip circuit is consti-

tuted by the direct TL presenting physical width, w_{port} . The direct TL was designed with characteristic impedance equal to the terminal load reference impedance, $R_0=50 \Omega$.

As initial value, by denoting the substrate effective permittivity, ϵ_{reff} , and vacuum speed of light, c , the TL length was calculated via the formula:

$$L = \frac{c}{2f_0\sqrt{\epsilon_{reff}}} \quad (6)$$

As illustrated in Fig.3 (b), the DGS is constituted by bilateral side of interconnected holed and notched elements. The notched elements present physical lengths, l_k , and widths, w_k , with $k = 1, \dots, 5$. The notched element parameters were chosen in order to generate the bandpass negative group delay specifications targeted in Table 1. As displayed in Fig.3 (b), in each side of the circuit, the notched element is surrounded in U-shape by aligned via hole with physical diameter, D_{via} , and interspaced, S_{via} . The POC NGD circuit was expected to operate under low-attenuation better than 4 dB and well access matching under return loss better than 10 dB.

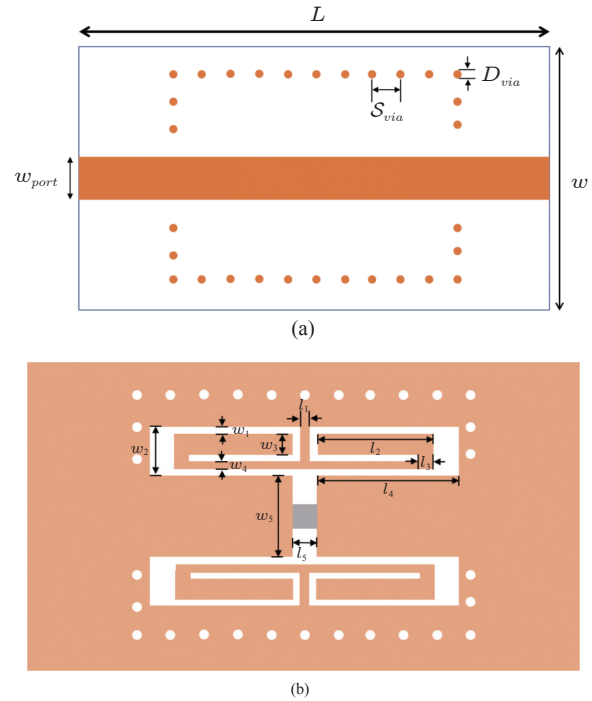


Fig. 3. DGS planar design. (a) Top view of the overall circuit; (b) Backside view of notched element.

Table 1. Targeted BP NGD specifications

Parameter	DG_0	f_0	Δf	S_{11}	S_{21}
Value	-2 ns	2 GHz	40 MHz	-10 dB	-4 dB

2. DGS SIW circuit prototyping

The DGS circuit prototype was implemented on double side Copper metallized FR4-based substrate. The length and width physical sizes, l_k , and w_k , of the notched elements were optimized with HFSS® simulations in order to achieve the targeted BP NGD response specified previously in Table 1. Fig.4 (a) and Fig.4(b) display the HFSS® 3-D design view and photograph of top and back sides of the fabricated prototype with size, 19 mm × 34 mm. The final values of the POC circuit physical parameters are addressed in Table 2. For the better understanding the influence of each physical dimension on the BP NGD function, the detailed parametric analyses will be explored in the next paragraph.

3. Parametric analyses with respect to the DGS physical sizes

The present parametric investigation is based on the S-parameter computation of the DGS structure introduced previously. The computations were carried out in the HFSS® environment with the frequency bandwidth from 1.8 GHz to 2.2 GHz with 300 frequency samples. During the simulations, the considered notched element physical parameters were swept linearly.

1) Parametric analysis versus l_1

The first parametric analysis was performed by

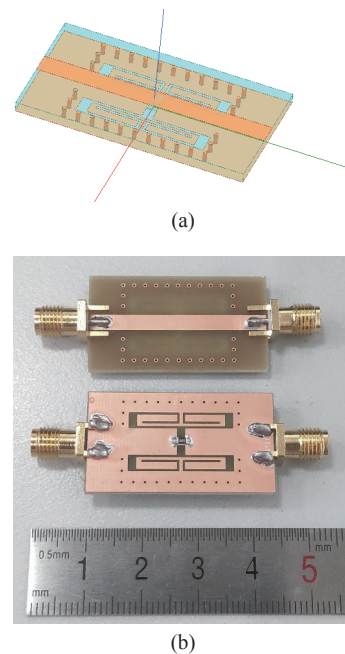


Fig. 4. (a) 3-D HFSS® design; (b) Photograph of the fabricated DGS circuit prototype.

Table 2. DGS circuit parameters and specifications

Components	Description	Parameter	Value
Dielectric substrate	Material	FR4	–
	Relative permittivity	ϵ_r	4.2
	Loss tangent	$\tan(\delta)$	0.02
	Thickness	h	1.5 mm
Metallization	Material	Copper (Cu)	–
	Thickness	t	35 μm
	Conductivity	σ	58 MS/m
DGS NGD circuit	Total length	L	34 mm
	Total width	W	19 mm
	Resistance	R	36 Ω
	Via diameter	D_{via}	0.6 mm
	Via interspace	S_{via}	1.5 mm
	Width	W_{port}	3.1 mm
		w_1	0.4 mm
		w_2	3 mm
		w_3	1.3 mm
		w_4	0.5 mm
	Length	w_5	5 mm
		l_1	0.6 mm
		l_2	7.3 mm
		l_3	0.92 mm
l_4		8.75 mm	
l_5	1.5 mm		

varying l_1 from 0.4 mm to 1 mm and fixing all the other parameters in Table 2. After simulations, we obtain the results mapped in Fig.5. In these results, Fig.5(a) illustrates that the BP NGD behavior is conserved despite the swept of l_1 .

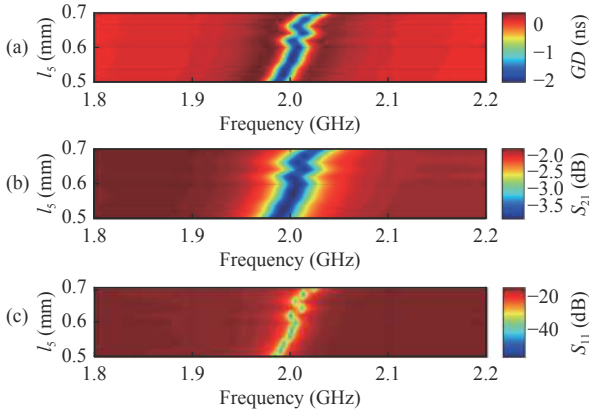


Fig. 5. Parametric simulated results versus l_1 . (a) GD ; (b) S_{21} ; (c) S_{11} .

As witnessed by Table 3, in the considered parametric range, the variation of l_1 , influences remarkably the NGD center frequency, f_0 , which increases from 1.969 GHz to 2.064 GHz. Moreover, the GD optimal value, $GD(f_0)$ present absolute value decreasing from about 2.22 ns down to 1.74 ns. As shown in Fig.5(b), the transmission coefficient (S_{21}) is increasing from -4.09 dB to -3.78 dB over reflection coefficient (S_{11}) of Fig.5(c)

Table 3. NGD specifications versus l_1

l_1 (mm)	Z (Ω)	f_0 (GHz)	$GD(f_0)$ (ns)	$S_{21}(f_0)$ (dB)	$S_{11}(f_0)$ (dB)
0.4	50.2	1.969	-2.22	-4.09	-44.4
0.6	49.9	2.007	-2.19	-4.07	-46.0
0.8	49.8	2.028	-1.94	-3.86	-34.7
1.0	49.7	2.064	-1.74	-3.78	-35.2

widely better than -10 dB.

2) Parametric analysis versus w_5

This second parametric analysis aims to investigate the influence of w_5 . This parameter was varied from 1.9 to 2.2 mm by fixing all the other ones as shown in Table 2. Fig.6 summarize the mappings of the group delay, transmission and reflection coefficients. Table 4 shows the NGD performances at different values of w_5 . Fig.6(a) illustrates the conservation of the DGS circuit BP NGD responses despite the variation of w_5 . In this case, the NGD center frequency is slightly shifted with 3 MHz variation. The absolute value of $GD(f_0)$ is decreasing also from 2.53 ns to 1.65 ns. The transmission coefficient mapped in Fig.6(b) is increasing from -4.38 dB to -3.59 dB.

3) Parametric analysis versus R

This third parametric analysis aims to investigate the influence of R . This later one was varied from 36 to 43 Ω by fixing all the other ones as shown in Table 2. Fig.7 plot the group delay responses of the DGS NGD circuit for the different values of R . Table 5 indicates

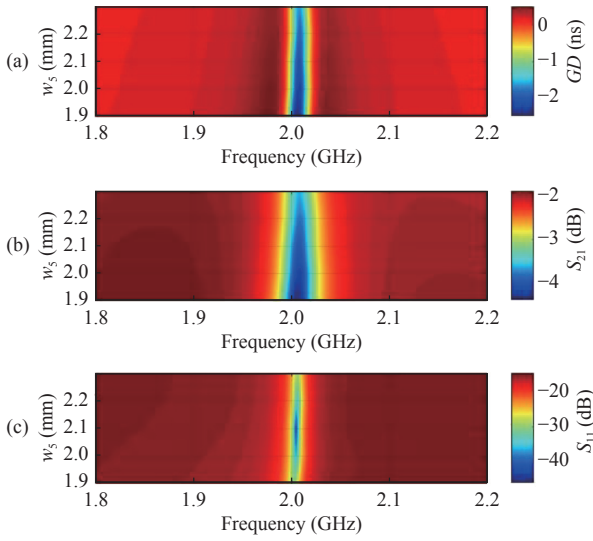


Fig. 6. Parametric simulated results versus w_5 . (a) GD ; (b) S_{21} ; (c) S_{11} .

Table 4. NGD specifications versus w_5

w_5 (mm)	Z (Ω)	f_0 (GHz)	$GD(f_0)$ (ns)	$S_{21}(f_0)$ (dB)	$S_{11}(f_0)$ (dB)
4.8	49.9	2.006	-2.53	-4.38	-30.2
4.9	49.8	2.007	-2.32	-4.18	-36.3
5.0	49.9	2.007	-2.19	-4.07	-46.0
5.1	50.1	2.009	-1.87	-3.78	-34.4
5.2	49.8	2.009	-1.65	-3.59	-28.6

the frequency domain specifications around the NGD center frequency, f_0 . This later one variation can be considered as negligible under the variation of R . It can be understood from Fig.7(a) that the resistor value influences the access matching. However, the transmission coefficient around the NGD center frequency presents less than 0.3 dB variation. More importantly, as explained by Fig.7(c), the GD responses can be literally assumed as insensitive to the R variation.

4) S -parameter analysis versus vias

This last parametric analysis aims to investigate the influence of vias. Fig.8 plot the difference of the BP NGD response with/without the vias. Table 6 indicates the frequency domain specifications around the NGD center frequency, f_0 . It can be understood from Fig.8(a) that the reflection coefficient and the transmission coefficient of the circuit with vias is better than the circuit without vias.

IV. Simulated and Experimental Validation Results

The bandpass negative group delay aspect of the DGS circuit prototype was investigated by comparisons of the full wave simulation and measurement. The detailed experimental results will be discussed in the next subsection.

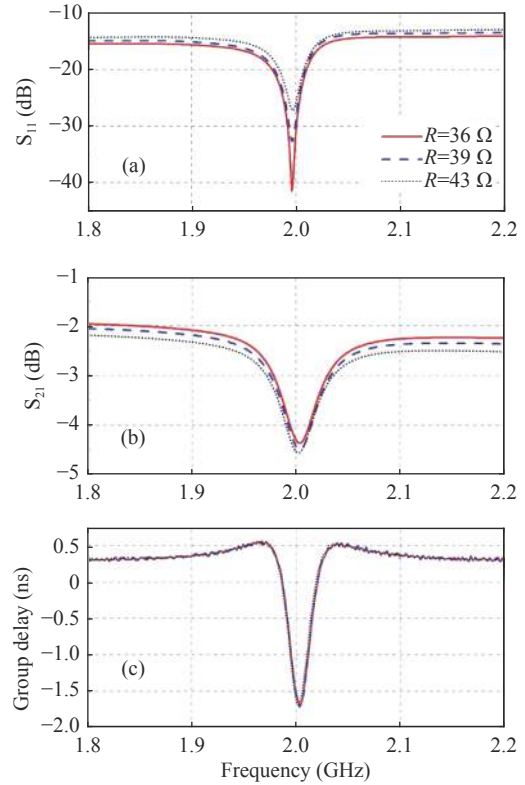


Fig. 7. Parametric simulated results versus R . (a) S_{11} ; (b) S_{21} ; (c) GD .

Table 5. NGD specifications versus resistance R

R (Ω)	f_0 (GHz)	$GD(f_0)$ (ns)	$S_{21}(f_0)$ (dB)	$S_{11}(f_0)$ (dB)
36	2.003	-1.69	-4.37	-41.5
39	2.003	-1.70	-4.49	-32.6
43	2.002	-1.67	-4.57	-27.2

1. Test and measurement of DGS NGD circuit prototype

Similar to classical microwave devices, the validation study was carried out via S -parameter measurement from 1.8 GHz to 2.2 GHz.

The experimental setup configuration with vector network analyzer (VNA) is shown in Fig.9. The VNA is from Rohde & Schwarz® referenced ZNB 20 and specified by frequency band 100 kHz to 20 GHz. Fig.10 show the comparisons between the simulated and measured results. The HFSS® computation speed was less than five minutes. As analyzed above, these well-correlated results verify the negative group delay function of the notched element based DGS circuit.

As plotted in Fig.10(c), the center frequency (f_0) of the fabricated circuit is about 2 GHz. The tested circuit presents the NGD optimal simulated and measurement values, $GD(f_0)$, approximately -2.19 ns against -1.69 ns. The NGD bandwidth is approximately 33.7 MHz. As shown in Fig.10 (b) and in Fig.10 (a), the transmission coefficient is about -4.37 dB while the re-

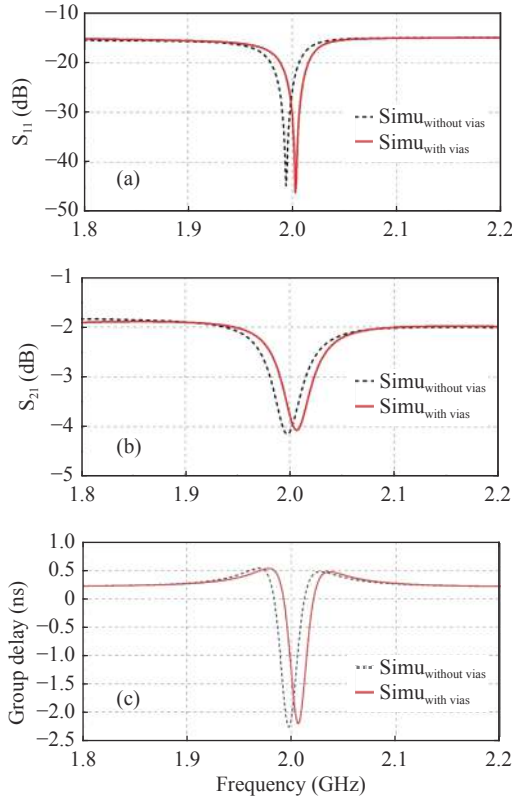


Fig. 8. Parametric simulated results versus vias. (a) S_{11} ; (b) S_{21} ; (c) GD .

Table 6. NGD specifications versus vias

	f_0 (GHz)	$GD(f_0)$ (ns)	$S_{21}(f_0)$ (dB)	$S_{11}(f_0)$ (dB)
With vias	2.007	-2.19	-4.07	-46.0
Without vias	1.997	-2.25	-4.14	-44.6

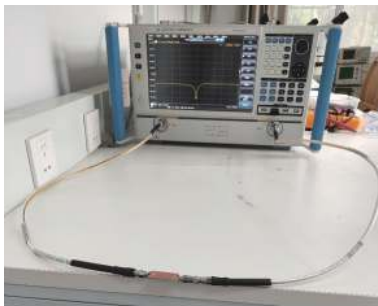


Fig. 9. Photograph of the DGS NGD circuit frequency domain experimental setup.

reflection coefficient is up to -41.5 dB around the NGD center frequency.

There is little difference between the simulation and the experimental results. Table 7 summarizes the

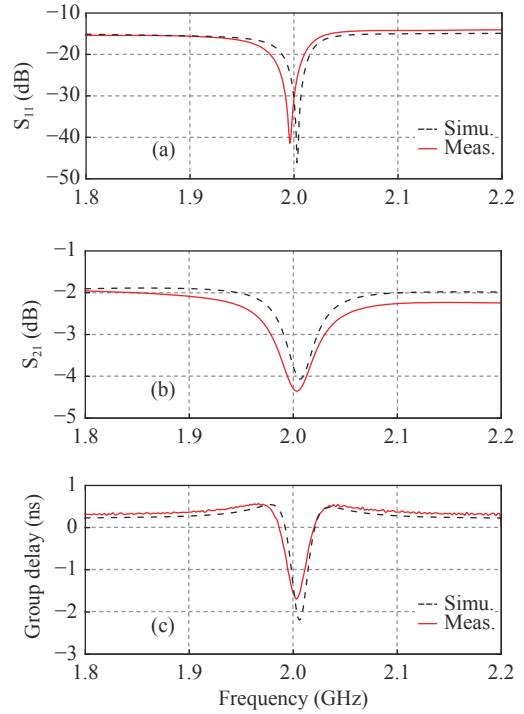


Fig. 10. Simulated and measured (a) Reflection and (b) Transmission coefficients, (c) GD of the fabricated circuit.

comparison of NGD performances from two aspects of simulation results and measurement results.

The following subsection will discuss the BP NGD performance comparisons between the developed DGS NGD result and the existing ones in the literature.

2. Discussion on active prototype NGD performances compared with the literature

Table 8 summarizes the comparison of NGD performance parameters with the literature NGD circuit [22]–[23], [30]–[32]. Compared to the DGS NGD circuit introduced in [19]–[23], [30]–[32], the DGS NGD circuit presented in this paper show the advantage in better transmission coefficient and reflection coefficient and relative compact size. As the DGS NGD circuit is simple and robust to parameters' variations, it is easy to design and fabricate. The main circuit is designed at the back side of the PCB and the top size is only a TL, easily implementable in microwave circuit to equalize the delay.

V. Conclusions

An innovative design method of BP NGD circuit based on DGS and SIW-matched structure implemen-

Table 7. Simulated and experimented NGD performances

Validation method	f_0 (GHz)	GD_n (ns)	BW (MHz)	S_{21} (dB)	S_{11} (dB)
Simulation	2.007	-2.19	28.7	-4.07	-46.0
Measurement	2.003	-1.69	33.7	-4.37	-41.5

Table 8. NGD performance comparison

Ref.	f_0 (GHz)	GD_n (ns)	BW (MHz)	S_{21} (dB)	S_{11} (dB)	Size (λ_g^2)
[19]	3.56	-4.24	62	-26.6	(*)	0.26×0.17
[20]	3.5	-3.8	100	-37.1	(*)	0.89×0.27
[27]	1	-1.5	370	-33	-28	0.78×0.06
[28]	1.79	-7.7	35	-8.6	-20	0.3×0.18
[29]	1.57	-8.75	60	-20.5	-32	0.39×0.19
Proposed one	2	-1.69	33.7	-4.37	-41	0.43×0.24

Note: (*) means no data in the origin references, simulation results indicate it is not better than -10 dB.

ted directly transmission TL associated with specific design of notched ground plane. The essential specifications of BP NGD functions are pedagogically defined. The design process of the DGS topological structure is elaborated with the graphical design flow.

The feasibility study of the DGS BP NGD circuit is performed with the design description followed by parametric analyses in function of the key geometrical parameters of the notched elements. The fabricated circuit after optimization is described. The test results confirm an outstanding correlation between the BP NGD responses from simulation and measurement.

In the future, the DGS NGD topology is expected as a potential solution for EMC compliant microwave 5G-circuits against the size and NGD performances.

References

- [1] H. Yang, X. Xiao, and H. Song, "Field-circuit simulation of electromagnetic interference and optimisation design in vehicle navigation system," *IET Science, Measurement & Technology*, vol.14, no.5, pp.552-556, 2020.
- [2] B. Archambeault, C. Brench, and S. Connor, "Review of printed-circuit-board level EMI/EMC issues and tools," *IEEE Trans. Electromag. Comp.*, vol.52, no.2, pp.455-461, 2010.
- [3] X. Z. Wu, C. Zhang, S. F. Yang, and L. Q. Zhao, "Computerized simulation of board-level EMC in high-speed PCB," *Advanced Materials Research*, vol.989-994, pp.1977-1980, 2014.
- [4] V. Jandhyala, D. Gope, S. Chakraborty, R. Murugan, and S. Mukherjee, "Toward building full-system EMI verification and early design flows through full-wave electromagnetic simulation," *Int. J. RF and Microwave Computer-Aided Engineering*, vol.22, no.1, pp.104-115, 2012.
- [5] U. Choi, Y.-J. Kim, and Y.-S. Kim, "Crosstalk reduction in printed circuit boards using irregularly-spaced vias in a guard trace over a slotted ground plane," in *Proc. of 2009 European Conference on Circuit Theory and Design*, Antalya, Turkey, pp.794-797, 2009.
- [6] A. Henridass, M. Sindhadevi, N. Karthik, *et al.*, "Defective ground plane structure for broadband crosstalk reduction in PCBs," in *Proc. of 2012 Int. Conf. on Computing, Communication and Applications*, Dindigul, India, pp.1-5, 2012.
- [7] M. Sindhadevi, K. Malathi, A. Henridass, and A. K. Shrivastav, "Crosstalk reduction using defective ground plane structures in RF printed circuit boards," *Arabian Journal for Science and Engineering*, vol.39, pp.1107-1116, 2014.
- [8] X. Gao, H. C. Zhang, P. H. He, *et al.*, "Crosstalk suppression based on mode mismatch between spoof SPP transmission line and microstrip," *IEEE Trans. Components Packaging and Manufacturing Technology*, vol.9, no.11, pp.2267-2275, 2019.
- [9] M. M. Bait-Suwailam, and O. M. Ramahi, "Ultrawideband mitigation of simultaneous switching noise and EMI reduction in high-speed PCBs using complementary split-ring resonators," *IEEE Trans. Electromag. Comp.*, vol.54, no.2, pp.389-396, 2012.
- [10] S.-G. Kim, H. Kim, H.-D. Kang, and J.-G. Yook, "Signal integrity enhanced EBG structure with a ground reinforced trace," *IEEE Trans. Components Packaging and Manufacturing Technology*, vol.33, no.4, pp.284-288, 2010.
- [11] M. Sindhadevi, K. Malathi, A. Henridass, and A. K. Shrivastav, "Signal integrity performance analysis of mutual coupling reduction techniques using DGS in high speed printed circuit boards," *Wireless Pers. Commun.*, vol.94, pp.3233-3249, 2017.
- [12] W. Duk-Jae and L. Taek-Kyung, "Suppression of harmonics in Wilkinson power divider using dual-band rejection by asymmetric DGS," *IEEE Transactions on Microwave Theory and Techniques*, vol.53, no.6, pp.2139-2144, 2005.
- [13] C. S. Kim, J. S. Park, D. Ahn, and J. B. Lim, "A novel 1-D periodic defected ground structure for planar circuits," *IEEE Microw. Guided Wave Lett.*, vol.10, no.4, pp.131-133, 2000.
- [14] P. Jun-Seok, Y. Jun-Sik, and A. Dal, "A design of the novel coupled-line bandpass filter using defected ground structure with wide stopband performance," *IEEE Transactions on Microwave Theory and Techniques*, vol.50, no.9, pp.2037-2043, 2002.
- [15] L. Jong-Sik, K. Chul-Soo, D. Ahn, *et al.*, "Design of low-pass filters using defected ground structure," *IEEE Transactions on Microwave Theory and Techniques*, vol.53, no.8, pp.2539-2545, 2005.
- [16] L. Zhou, Y. Ma, J. Shi, J. Chen, and W. Che, "Differential dual-band bandpass filter with tunable lower band using embedded DGS Unit for common-mode suppression," *IEEE Transactions on Microwave Theory and Techniques*, vol.64, no.12, pp.4183-4191, 2016.
- [17] D.-B. Lin and Y.-H. Lee, "A wideband common-mode suppression filter using enhanced coupled defected ground structure," in *Proc. of 2016 IEEE Int. Symp. on Electromag. Comp. (EMC)*, Ottawa, ON, Canada, pp.791-796, 2016.
- [18] L. Chan, J. Li, H. Pan, and X. Qin Yi, "An efficient-im-

- proved power amplifier using split-ring resonator defected ground structure,” in *Proc. of 2010 Asia-Pacific Int. Symp. on Electromag.*, Beijing, China, pp.1421–1423, 2010.
- [19] H.-N. Lin, W.-D. Tseng, C.-H. Wu, *et al.*, “Root cause analysis and defect ground effect of EMI problem for power electronics,” in *Proc. of 2019 Joint Int. Symp. on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC)*, Sapporo, Japan, pp.440–443, 2019.
- [20] C. Kumar, M. I. Pasha, and D. Guha, “Microstrip patch with nonproximal symmetric defected ground structure (DGS) for improved cross-polarization properties over principal radiation planes,” *IEEE Antennas and Wireless Propagation Letters*, vol.14, pp.1412–1414, 2015.
- [21] A. M. E. Safwat, F. Podevin, P. Ferrari, and A. Viltot, “Tunable bandstop defected ground structure resonator using reconfigurable dumbbell-shaped coplanar waveguide,” *IEEE Transactions on Microwave Theory and Techniques*, vol.54, no.9, pp.3559–3564, 2006.
- [22] G. Chaudhary, Y. Jeong, and J. Lim, “Miniaturized dual-band negative group delay circuit using dual-plane defected structures,” *IEEE Microwave and Wireless Components Letters*, vol.24, no.8, pp.521–523, 2014.
- [23] G. Chaudhary, J. Jeong, P. Kim, Y. Jeong, and J. Lim, “Compact negative group delay circuit using defected ground structure,” in *Proc. of 2013 Asia-Pacific Microwave Conference Proceedings (APMC)*, Seoul, Korea (South), pp.22–24, 2013.
- [24] R. Xian-Ke Gao, S.-P. Gao, H. M. Lee, and E.-X. Liu, “Metamaterial-based common-mode noise filter with NGD effect for multilayer PCB,” in *Negative Group Delay Devices: From Concepts to Applications*, IET Materials, Circuit and Devices Series 43, Publisher Michael Faraday House, Hertfordshire, UK, pp.309–342, 2018.
- [25] B. Ravelo, *Negative Group Delay Devices: From Concept to Applications*, IET Materials, Circuit and Devices Series 43, Publisher Michael Faraday House, UK, 2018.
- [26] O. F. Siddiqui, M. Mojahedi, and G. V. Eleftheriades, “Periodically loaded transmission line with effective negative refractive index and negative group velocity,” *IEEE Trans. Antennas Propagat.*, vol.51, no.10, pp.2619–2625, 2003.
- [27] G. V. Eleftheriades, O. Siddiqui, and A. K. Iyer, “Transmission line for negative refractive index media and associated implementations without excess resonators,” *IEEE Microw. Wireless Compon. Lett.*, vol.13, no.2, pp.51–53, 2003.
- [28] L. -F. Qiu, L. -S. Wu, W. -Y. Yin, and J. -F. Mao, “Absorptive bandstop filter with prescribed negative group delay and bandwidth,” *IEEE Microw. Wireless Compon. Lett.*, vol.27, no.7, pp.639–641, 2017.
- [29] Z. Wang, Y. Cao, T. Shao, S. Fang, and Y. Liu, “A negative group delay microwave circuit based on signal interference techniques,” *IEEE Microw. Wireless Compon. Lett.*, vol.28, no.4, pp.290–292, 2018.
- [30] C.-T.-M. Wu and T. Itoh, “Maximally flat negative group-delay circuit: A microwave transversal filter approach,” *IEEE Trans. Microw. Theory Techn.*, vol.62, no.6, pp.1330–1342, 2014.
- [31] G. Liu and J. Xu, “Compact transmission-type negative group delay circuit with low attenuation,” *Electron. Lett.*, vol.53, no.7, pp.476–478, 2017.
- [32] T. Shao, Z. Wang, S. Fang, *et al.*, “A compact transmission line self-matched negative group delay microwave circuit,” *IEEE Access*, vol.5, pp.22836–22843, 2017.
- [33] T. Shao, S. Fang, Z. Wang, and H. Liu, “A compact dual-band negative group delay microwave circuit,” *Radio Engineering*, vol.27, no.4, pp.1070–1076, 2018.
- [34] X. Zhou, B. Li, N. Li, *et al.*, “Analytical design of dual-band negative group delay circuit with multi-coupled lines,” *IEEE Access*, Vol.8, No.1, pp.72749–72756, 2020.
- [35] B. Ravelo, “On the low-pass, high-pass, bandpass and stop-band NGD RF passive circuits,” *URSI Radio Science Bulletin*, vol.2017, no.363, pp.10–27, 2017.
- [36] M. Esmaili and J. Bornemann, “Novel tunable bandstop resonators in SIW technology and their application to a dual-bandstop filter with one tunable stopband,” *IEEE Microw. Wireless Compon. Lett.*, vol.27, no.1, pp.40–42, 2017.
- [37] A. P. Saghati, A. P. Saghati, and K. Entesari, “Ultra-miniature SIW cavity resonators and filters,” *IEEE Trans. Microw. Theory Techn.*, vol.63, no.12, pp.4329–4340, 2015.
- [38] M. Kumar Khandelwal, B. Kumar Kanaujia, and S. Kumar, “Defected ground structure: Fundamentals, analysis, and applications in modern wireless trends,” *Int. J. of Ant. And Prop.*, vol.2017, pp.1–22, 2017.



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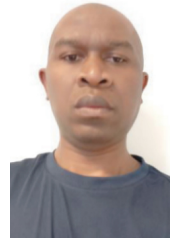


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