A 1.6-mW Cryogenic SiGe LNA IC for Quantum Readout Applications Achieving 2.6-K Average Noise Temperature From 3 to 6 GHz

Zhenjie Zou, *Graduate Student Member, IEEE*, Sanjay Raman, *Fellow, IEEE*, and Joseph C. Bardin, *Fellow, IEEE*

***Abstract*— Readout of superconducting quantum processors of sufficient scale to enable useful fault-tolerant quantum computing will require large arrays of high-performance cryogenic low-noise amplifiers. While it is desirable to employ silicon-based integrated-circuit amplifiers for this application, to date, the noise performance of such devices has been significantly worse than that of amplifiers implemented in III–V technologies. Here, we present the design and characterization of a high-gain cryogenic SiGe LNA IC achieving an average noise temperature of 2.6 K over the 3–6-GHz frequency band while dissipating just 1.6 mW. To the best of our knowledge, this amplifier achieves the best performance of any silicon-based LNA (discrete or integrated circuit) operating in this frequency range.**

***Index Terms*— Cryogenic LNA, noise modeling, quantum computing, SiGe HBT.**

I. Introduction

STATE-OF-THE-ART superconducting quantum processors are measured using a technique known as dispersive readout, in which the quantum state of a qubit is encoded in the phase of a ∼5-GHz readout resonator's reflection coefficient [1]. However, dispersive readout is complicated by the fact that the system being measured is so nonlinear that the measurement must be performed while populating the readout resonator with no more than ∼10 microwave photons, each of energy $E_{\text{photon}} = hf$, where h is the Planck constant and f is the readout frequency. Since quantum mechanics dictate that the probe signal be accompanied by a spectral density corresponding to a 1/2 photon of quantum noise and that any phase-preserving amplification chain must add at least another 1/2 photon of input-referred noise, achieving the signal-to-noise ratio needed for high-fidelity dispersive readout requires implementation of a near-quantum-limited amplification chain (i.e., one approaching noise temperature $T_e = 0.12$ K at 5 GHz).

Parametric amplifiers thermalized to ∼10 mK and employing superconducting nonlinear reactances provide a means to achieve near-quantum-limited amplification and find wide use in the readout of superconducting quantum processors [2]. However, linearity and bandwidth considerations typically limit the gain achievable by these devices to below 20 dB. Thus, amplification of the very weak probe signal (roughly −125 dBm) to levels appropriate for digitization while preserving near-quantum-limited noise performance requires the parametric amplifier be followed by a state-of-the-art semiconductor amplification chain. The first stage of this chain is usually thermalized at about 4 K, allowing the use of a superconducting input cable, and should provide as low noise as possible while achieving sufficient gain to overcome the impact of noise contributed by subsequent amplification at room temperature. Today, these amplifiers are usually implemented using InP HEMT technology; discrete InP HEMT amplifiers achieving $T_e < 2$ K from 4 to 8 GHz while dissipating less than 8 mW are commercially available [3].

For today's $\mathcal{O}(100)$ qubit quantum computers, only 10–20 readout chains are required for complete readout of the processor. However, future fault-tolerant quantum computers are expected to require $\mathcal{O}(100\,000)$ readout chains [4], motivating the development of silicon-based cryogenic LNAs, which can be mass manufactured and benefit from ON-chip digital CMOS. In particular, SiGe HBT-based cryogenic LNAs appear to be a promising candidate for this application, due to their low-power operation [5] and excellent noise properties. Recent progress in cryogenic SiGe LNAs includes a 1-mW 4–8-GHz discrete transistor amplifier achieving an average $T_e = 3.2$ K [6] and a 2.9-mW 3–6-GHz frequency and bandwidth reconfigurable LNA IC achieving an average $T_e = 4.3$ K [7]. However, to the best of our knowledge, no SiGe IC demonstrating $T_e < 4$ K in this frequency range has been reported to date.

Here, we present the design and measurement of a high-gain 3–6-GHz cryogenic SiGe LNA achieving an average $T_e = 2.6$ K while dissipating just 1.6 mW. The amplifier uses Global Foundries SG4501 technology [8], which combines ∼500-GHz $f_{\max}$ SiGe HBTs with 45-nm PDSOI CMOS.

II. HBT Characterization and Model Extraction

To enable amplifier design, we first extracted cryogenic small-signal noise models using transistor and de-embedding structures provided to us by the foundry. Using a Lakeshore

Manuscript received 28 February 2024; revised 21 April 2024; accepted 23 April 2024. Date of publication 8 May 2024; date of current version 7 June 2024. This work was supported by the Defense Advanced Research Projects Agency (DARPA) through Office of Naval Research (ONR) under Grant N00014-20-1-4003. *(Corresponding author: Zhenjie Zou.)*

Zhenjie Zou and Sanjay Raman are with the Department of Electrical and Computer Engineering, University of Massachusetts Amherst, Amherst, MA 01003 USA (e-mail: zzou@umass.edu; sraman@umass.edu).

Joseph C. Bardin is with the Department of Electrical and Computer Engineering, University of Massachusetts Amherst, Amherst, MA 01003 USA, and also with Google Inc., Goleta, CA 93117 USA (e-mail: jbardin@engin.umass.edu).

This article was presented at the IEEE MTT-S International Microwave Symposium (IMS 2024), Washington, DC, USA, June 16–21, 2024.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWT.2024.3395114.

Digital Object Identifier 10.1109/LMWT.2024.3395114

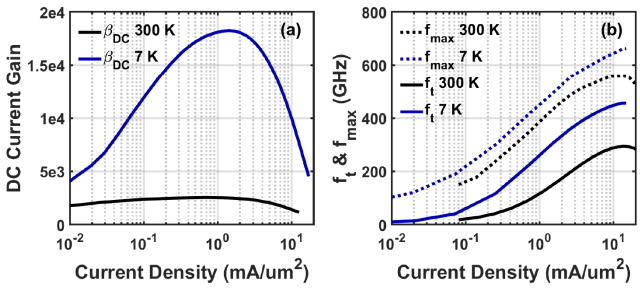

Fig. 1. (a) β_{DC} and (b) f_t/f_{max} at room temperature and 7 K.

TABLE I

SMALL-SIGNAL MODEL PARAMETER AT 7 K (THE MODEL WAS ACQUIRED AT $V_{CE} = 0.5$ V)

J_C	R_B	R_E	R_C	C_{CB}	C_{CS}	C_{BE}	g_m	τ	β_{DC}	r_{be}	$T_{MIN\ @\ 5\ GHz}$
mA/μm^2	$\Omega \cdot \mu$m^2			fF/μm^2			mS/μm^2	ps	–	$\Omega \cdot \mu$m^2	K
0.625	3.1	1.4	5.6	18	4.7	39.7	69	0.7	1.76e4	1.9e5	1.1
0.5	3.8	1.4	5.6	18	4.7	38	57	0.8	1.72e4	2.2e5	1.2
0.25	6.8	1.4	5.6	18	4.7	35.1	29	1.4	1.54e4	3.0e5	1.5

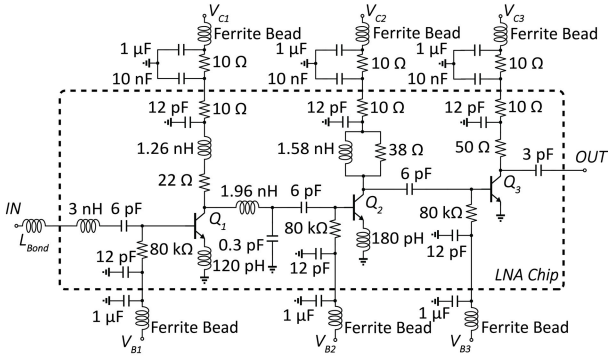

Fig. 2. LNA schematic with OFF-chip bypass network. Transistor dimensions—Q_1 : 4 × 0.1 × 10 μm, Q_2 : 2 × 0.1 × 10 μm, and Q_3 : 2 × 0.1 × 10 μm. Bias currents for each stage are 2.5, 1, and 0.5 mA, respectively.

CRX-4K probe station, we measured the (1 × 0.1 × 10 μm) NPN transistor for a wide range of current densities at both 300 and 7 K. Then, following PAD/OPEN/SHORT de-embedding [9], we extracted small-signal noise models for each bias point using the model topology and extraction procedure described in [10]. Example terminal characteristics for the HBTs appear in Fig. 1. With cryogenic cooling, we observed increases in a peak β_{DC}, f_t, and f_{max} of 7.2×, 1.6×, and 1.2×, respectively. Moreover, at a current density 0.5 mA/μm^2—close to the optimum for a typical cryogenic SiGe LNA—we observed the peak values of β_{DC}, f_t, and f_{max} of 17 000, 190 GHz, and 375 GHz, respectively. Extracted model parameters for three different current densities appear in Table I. The computed minimum achievable noise temperature is as low as 1.1 K at 5 GHz.

III. AMPLIFIER DESIGN

A schematic of the amplifier appears in Fig. 2. It is a three-stage design optimized to achieve $S_{21} > 35$ dB and $T_e < 3$ K from 3 to 6 GHz. The input stage is sized for $R_{OPT} \sim 50\ \Omega$ when biased at $J_C = 0.625$ mA/μm^2. A source inductor is used for simultaneous noise and impedance match. A series inductance of 3 nH is used for input matching. The second and third stages were used to flatten the gain profile and provide output matching. Filtering is incorporated into each of the bias lines to ensure stability despite the high ON-chip gain

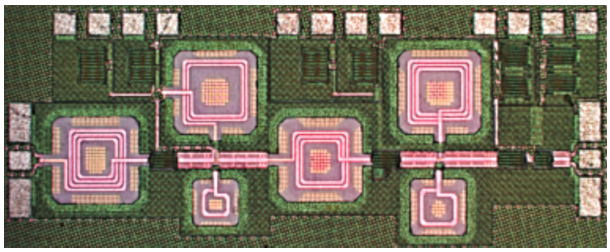

Fig. 3. Chip micrograph. The chip dimensions are 0.68 × 1.7 mm.

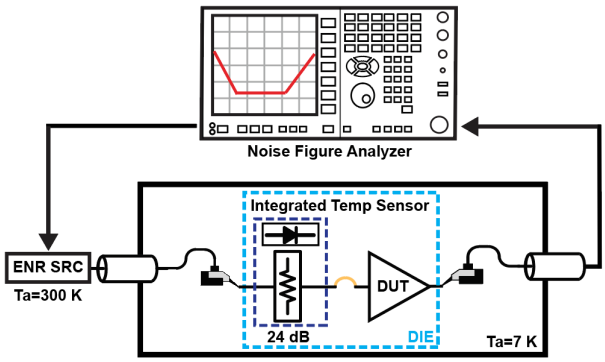

Fig. 4. System diagram of cold on-wafer attenuator measurement setup. The attenuator and LNA are on the same die and connected by bonding wire to minimize the uncertainty during the noise measurement.

of the amplifier. In addition, resistive loading was incorporated in the input and output stages to improve the gain and output match, respectively. All inductors used in the design were optimized for cryogenic operation through electromagnetic simulations, using a metal stack with 5× the conductivity and 1000× the substrate resistivity than that of the room temperature PDK values [11]. The design is optimized to draw 4 mA from 0.4 V, corresponding to a power consumption of 1.6 mW.

IV. RESULTS

A die micrograph of the fabricated IC appears in Fig. 3. To study the limits of the amplifier performance, the IC was characterized entirely on wafer. Both scattering parameter and noise measurements were carried out, with the cold attenuator method [12], [13] applied for the on-wafer noise measurements.

A block diagram of the measurement setup used to characterize the noise of the amplifier appears in Fig. 4. A 24-dB attenuator with a local temperature sensor was cointegrated on die next to the LNA, permitting interconnection between the attenuator and the LNA via short wirebonds. We chose to use an attenuator value of 24 dB rather than the more commonly used 20 dB to reduce uncertainties related to the noise source ENR and the noise contributions of the poorly thermalized lossy coaxial transmission line connecting between the input wafer probe and the room temperature feedthrough of the cryogenic probe station. The ON-chip temperature sensor is required to determine the physical temperature of the 24-dB attenuator.

Photographs of the test setup as configured during noise measurements appear in Fig. 5. The die was mounted to the probe station chuck using silver epoxy, and, to enable adequate bypassing of both the amplifier biases and the temperature sensor readout lines (configured for Kelvin sensing), all dc biases were supplied via cryogenic wires, which, as shown in Fig. 5, were wrapped around OFHC bobbins and encapsulated

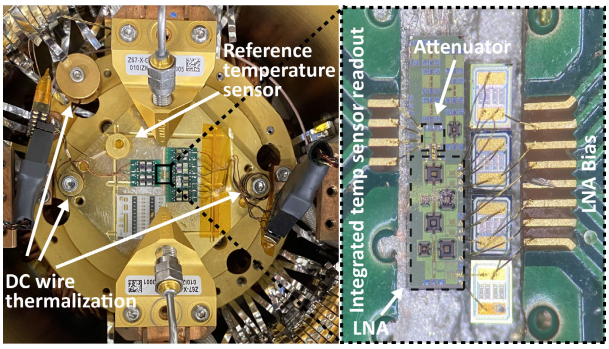

Fig. 5. Photograph showing the measurement setup on a chuck inside the cryogenic probe station. An on-wafer diode temperature sensor is incorporated next to the attenuator.

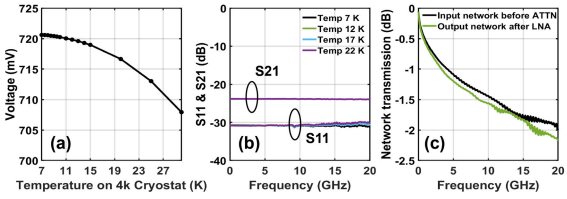

Fig. 6. (a) Characterization of on-wafer temperature sensor. (b) S-parameter measurement of on-wafer attenuator at 7, 12, 17, and 22 K, respectively. (c) Network transmission before attenuator (black) and after LNA (green).

in Stycast epoxy. A reference temperature sensor, affixed to the chuck surface using GE varnish, was used to calibrate the ON-chip temperature sensor (which is a Schottky diode biased at a constant 10-μA current). To remove ancillary sources of dc heating of the ON-chip temperature sensor, the RF probes were lifted, and the LNA bias wires were open circuited for this calibration. As any error in this calibration due to excess ON-chip thermal loading would result in an artificial increase in the measured LNA noise temperature, this was a critical step in minimizing our measurement error. The temperature sensor calibration curve appears in Fig. 6(a).

With the temperature sensor calibrated, we next measured the amplifier and attenuator scattering parameters independently (before bonding the two together). The scattering parameters of the amplifier measured at 7 K appear alongside simulation in Figs. 7 and 8. The LNA achieved a peak gain of 39.2 dB at 4.7 GHz and average input and output return losses of 11 and 12 dB from 3 to 6 GHz, respectively. The measured amplifier characteristics show excellent agreement with simulation. The attenuator characteristics, measured from 7 to 22 K, appear in Fig. 6(b). The attenuator achieved excellent gain flatness and return loss from 0.01 to 20 GHz.

Next, we prepared to perform the on-wafer noise measurement by wire bonding the LNA to the attenuator (as shown in Fig. 5). Before measuring the amplifier, we first determined the losses of the input and output networks (connecting between the RF vacuum feedthrough and the probe tips) using a technique similar to a one-port VNA calibration. The measured transmission of the input and output networks appears in Fig. 6(c). Each of these networks includes a 1.85-mm vacuum feedthrough, a 1.85-mm stainless-steel coaxial cable, and an RF wafer probe.

Finally, we performed on-wafer measurement of the LNA noise temperature at physical temperatures ranging from 7 to 22 K. For these measurements, the amplifier was biased at the nominal 1.6-mW bias. Results appear in Fig. 8 alongside simulations. Excellent agreement was observed between measurement and simulation. Moreover, at a physical temperature of 7 K, the average noise measured from 3 to 6 GHz was

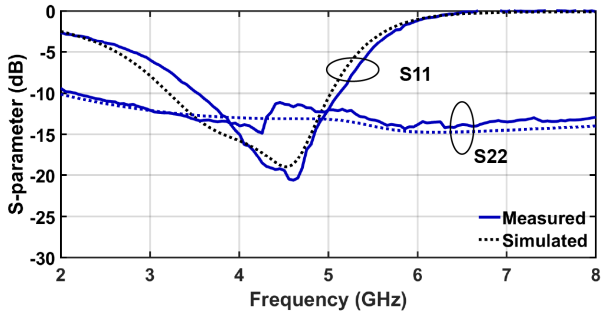

Fig. 7. On-wafer S-parameter measurement of the LNA at 7 K.

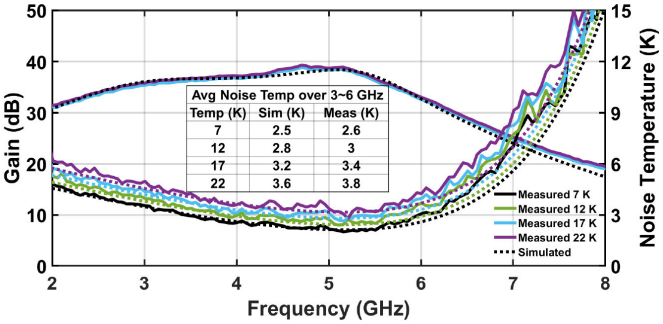

Fig. 8. Noise temperature and gain measurement with cold attenuator method at 7, 12, 17, and 22 K, respectively. The corresponding average noise temperatures over 3–6 GHz are 2.6, 3, 3.4, and 3.8 K, respectively.

TABLE II

COMPARISON TABLE WITH STATE-OF-THE-ART CRYOGENIC HEMT AND SiGe LNAs. FOM = $G_{\mathrm{dB}} \times (f_h/f_l) \times (hf_0/kT_e) \times (1/P_{\mathrm{DC}})$

Ref.	Technology	Form Factor	Frequency (GHz)	Gain (dB)	Noise (K)	P_{DC} (mW)	FOM ($\mathrm{mW^{-1}ph^{-1}}$)
[3]	InP-HEMT	Discrete	4-8	44	1.5	7.8	2.17
[6]	SiGe-HBT	Discrete	4-8	28	3.2	1	5.04
[7]	SiGe-HBT	Integrated	3-6	36	4.3	1.8	2.01
[14]	SiGe-HBT	Integrated	4-8	26	8	0.6	3.12
This	SiGe-HBT	Integrated	3-6	37	2.6	1.6	3.84

2.6 K. When the amplifier was warmed, we observed an approximately linear increase in a T_e of 0.08 K/K. This implies that the noise performance may improve if the amplifier was thermalized to 4 K rather than the 7 K employed here (which was set by the capabilities of our probe station).

The amplifier is compared with other state-of-the-art cryogenic LNAs in Table II. Considering a figure of merit that combines average gain, power dissipation, added noise photons, and relative bandwidth, this design offers the best trade-off among relative bandwidth, noise, and power consumption among prior integrated-circuit SiGe HBT LNAs.

V. CONCLUSION

Here, for the first time, we have shown that it is possible to realize an integrated-circuit LNA achieving noise performance below 3 K up to 6 GHz using a silicon technology. This is an important advance for the field of quantum computing, where large arrays of high-performance cryogenic LNAs will be required for future qubit readout systems. Future work should focus on further improving the noise performance of SiGe LNAs, while at the same time reducing power consumption.

ACKNOWLEDGMENT

The authors would like to thank GlobalFoundries for the chip fabrication. The opinions, interpretations, and/or findings expressed herein are those of the authors and are not necessarily indicative of the official views or policies of the Department of Defense or the U.S. Government.

REFERENCES

[1] J. C. Bardin, D. Sank, O. Naaman, and E. Jeffrey, "Quantum computing: An introduction for microwave engineers," *IEEE Microw. Mag.*, vol. 21, no. 8, pp. 24–44, Aug. 2020.

[2] J. Aumentado, "Superconducting parametric amplifiers: The state of the art in Josephson parametric amplifiers," *IEEE Microw. Mag.*, vol. 21, no. 8, pp. 45–59, Aug. 2020.

[3] *LNF-LNC4_8SF Datasheet*. Accessed: Feb. 27, 2023. [Online]. Available: https://lownoisefactory.com/wp-content/uploads/2023/03/lnf-lnc4_8sf.pdf

[4] J. C. Bardin, D. H. Slichter, and D. J. Reilly, "Microwaves in quantum computing," *IEEE J. Microw.*, vol. 1, no. 1, pp. 403–427, Jan. 2021.

[5] S. Montazeri, W.-T. Wong, A. H. Coskun, and J. C. Bardin, "Ultra-low-power cryogenic SiGe low-noise amplifiers: Theory and demonstration," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 178–187, Jan. 2016.

[6] W.-T. Wong, M. Hosseini, H. Rücker, and J. C. Bardin, "A 1 mW cryogenic LNA exploiting optimized SiGe HBTs to achieve an average noise temperature of 3.2 K from 4–8 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 181–184.

[7] Z. Zou, M. Hosseini, R. Kwende, S. Raman, and J. C. Bardin, "A frequency and bandwidth reconfigurable 3–6 GHz cryogenic SiGe BiCMOS LNA with a power consumption of $= 2.9$ mW," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 653–656.

[8] J. Pekarik et al., "SiGe HBTs with f_t/f_{max} ∼375/510 GHz integrated in 45 nm PDSOI CMOS," in *IEDM Tech. Dig.*, Dec. 2021, pp. 1–4.

[9] R. Torres-Torres, R. Murphy-Arteaga, and J. A. Reynoso-Hernandez, "Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1335–1342, Jul. 2005.

[10] J. C. Bardin, "Silicon-germanium heterojunction bipolar transistors for extremely low-noise applications," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, USA, 2009.

[11] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 448–456, 2020.

[12] G. Tomassetti, S. Weinreb, and K. Wellington, "Low-noise 10.7 GHz cooled GaAs FET amplifier," *Electron. Lett.*, vol. 17, nos. 25–26, pp. 949–950, 1981.

[13] F. Heinz, F. Thome, A. Leuther, and O. Ambacher, "A cryogenic on-chip noise measurement procedure with ±1.4-K measurement uncertainty," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 233–236.

[14] S. Montazeri and J. C. Bardin, "A sub-milliwatt 4–8 GHz SiGe cryogenic low noise amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 160–163.