A 4-to-6-GHz Cryogenic CMOS LNA With 4.4-K Average Noise Temperature in 22-nm FDSOI

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***Abstract*— Integrated readout systems are desired to enable future large-scale superconducting quantum computers. These systems require high-performance cryogenic low-noise amplifiers, and implementing these in CMOS is desirable from an integration point of view. However, realizing the necessary noise and power performance required for this application while using CMOS is an open challenge. Here, we present the design of a cryogenic low-noise amplifier (LNA) in 22-nm fully depleted silicon on insulator (FDSOI) technology. Operating between 4 and 6 GHz and consuming 15.8 mW, it achieved a peak gain of 38 dB, a minimum noise of 3.5 K at 5.2 GHz, and an average noise of 4.4 K. Through back-gate control and bias optimization, it can be operated at a lower supply voltage while dissipating <4.5 mW at the expense of 0.7-K higher noise. Considering a figure of merit (FOM), which takes into account the number of added noise photons, gain, bandwidth, and power consumption, the LNA, biased at low power, demonstrates an FOM of >3× higher than other state-of-the-art cryogenic CMOS (cryo-CMOS) LNAs. To the best of our knowledge, this is the first report of a cryo-CMOS LNA operating above 4 GHz that exhibits a noise temperature below 4 K.**

***Index Terms*— Cryogenic CMOS (cryo-CMOS), cryogenic device modeling, fully depleted silicon on insulator (FDSOI) CMOS, low-noise amplifier (LNA), low power, quantum computing.**

I. Introduction

QUANTUM computers promise to enable the solution of certain classes of problems that are not solvable using other known computational paradigms. However, implementation of a fault-tolerant quantum computer enabling such computations is currently believed to require at least one million physical qubits [1]; such a system is several orders of magnitude larger than what has already been demonstrated. Superconducting qubits are among the most promising of available technologies [2], but their readout requires near-quantum-limited amplification chains comprised of quantum-limited superconducting parametric amplifiers at 10 mK, providing ∼15–20-dB gain, followed by state-of-the-art 4–8-GHz semiconductor low-noise amplifiers (LNAs) at 3 K [3]. These semiconductor LNAs must provide enough gain to overcome the impact of subsequent room temperature LNA noise while providing sufficiently low noise temperature T_e to limit the impact on input-referred system noise temperature to about 20%, or $hf/5k$. While the feasibility of using cryogenic CMOS (cryo-CMOS) control systems to enable more extensible superconducting quantum computers is currently being aggressively researched (see [4], [5], [6], and [7]), the LNAs required at 3 K are currently implemented using InP HEMT technology [8], and, to date, cryo-CMOS LNAs with the high gain (≥35 dB), low power (≤1 mW) and low noise (≤4 K) required for this application have not been realized. Here, we present a cryo-CMOS LNA with performance approaching that required for large-scale superconducting quantum computers.

Several cryo-CMOS amplifiers targeting the ∼4–8 GHz frequency range have recently been reported (see [9], [10], [11], [12], and [13]). Of these results, the amplifiers whose power consumption was close to that required for superconducting quantum computing had noise temperatures (T_e) an order of magnitude too high for this application. For instance, the high-gain amplifier reported in [11] dissipated just 4.2 mW but had an average $T_e = 39$ K from 6 to 8 GHz. On the other hand, amplifiers whose T_e was closer to that required for this application dissipated over an order of magnitude too much power. To this point, the cryo-CMOS LNA with the lowest reported T_e to date (4.5–21 K over 4.2–9.2 GHz) dissipated 21 mW [12].

Here, we present the design and characterization of a 4–6-GHz cryo-CMOS LNA, implemented in the Global Foundries 22FDX technology (GF22FDX) and achieved a peak gain of 38 dB and minimum $T_e < 4$ K. Flipped-well NMOS devices were employed, and, through use of the back-gate, we were able to reduce the power consumption of the cryo-CMOS LNA to less than 5 mW while achieving an average noise temperature of 5.1 K from 4 to 6 GHz.

II. Cryogenic Transistor Model Extraction

The DC and RF characteristics of a GF22FDX NMOS transistor were measured at a physical temperature of 8 K using a Lakeshore CRX-4K cryogenic probe station. Scattering parameter measurements were obtained over a wide range of biases, with a pad-open-short de-embedding technique used to shift the reference plane to the transistor terminals. Small-

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TABLE I
SMALL-SIGNAL MODEL PARAMETERS, EXTRACTED AT 8 K

J_D	R_G	R_S	R_D	r_{gs}	C_{GS}	C_{GD}	C_{DS}	g_m	g_{ds}	τ	F	f_t	f_{max}
mA/mm	$\Omega \cdot \mu$m				fF/μm			mS/μm		fs		GHz	
37.5	480	98	95	66	0.45	0.23	0.24	0.92	0.08	100	0.7	221	277

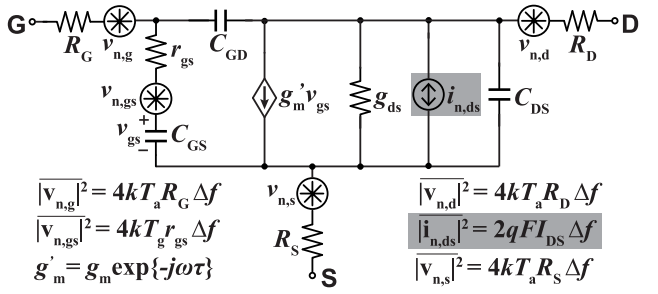

Fig. 1. MOSFET cryogenic small-signal noise model.

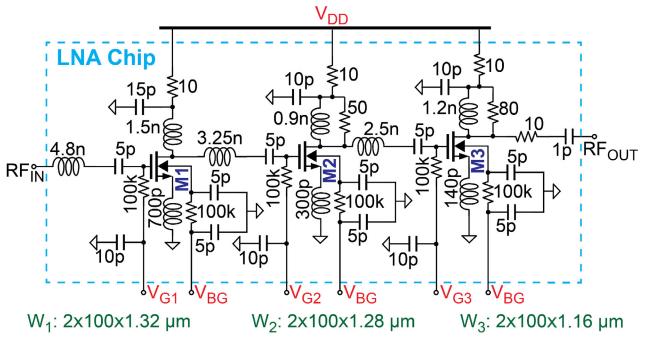

Fig. 2. Schematic of the 4–6-GHz cryogenic low noise amplifier. All FETs are of minimum length.

signal models were extracted from these de-embedded data using the method described in [14].

Completion of the small-signal noise model shown in Fig. 1 requires determination of the spectral density of the channel current noise. This model is a variant of the Pospieszalski model [15], which is widely used to describe the small-signal and noise performance of FETs at cryogenic temperatures. As explained in [16] and [17], MOSFET channel noise can be described as suppressed shot noise: $\overline{|i_{n,d}|^2} = 2qFI_{DS}$, where q is the elementary charge, I_{DS} is the dc drain current, and $F \leq 1$ is the Fano factor, which accounts for shot noise suppression. Determination of the unknown value of F requires a noise measurement, which can be performed in a 50-Ω environment [18]. In [13], we showed that F appears to be temperature-independent. Thus, we have extracted F for cryogenic modeling purposes using room temperature measurements. The extracted parameter values are shown in Table I for the bias point used for amplifier design.

III. AMPLIFIER DESIGN

The schematic of the LNA is shown in Fig. 2. It is a three-stage common source amplifier and is optimized to achieve high gain (>35 dB) and low noise at a center frequency of 5 GHz, aligning with the needs of superconducting qubit readout. We selected a bias point of 37.5 mA/mm for M_1 and M_2, trading off transistor T_{MIN} with power consumption. At this bias, $T_{MIN} \sim 1.5$ K at 5 GHz. The first-stage FET is sized for noise parameter $R_{OPT} \sim 50$ Ω. M_3 is biased at

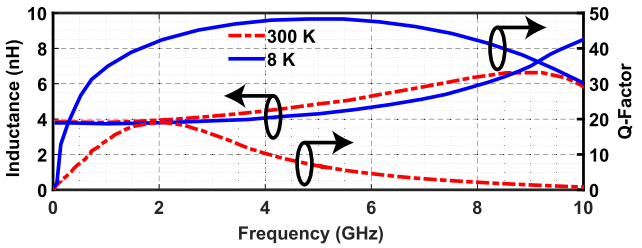

Fig. 3. EM simulation of the gate inductor and corresponding quality factor at 300 and 8 K.

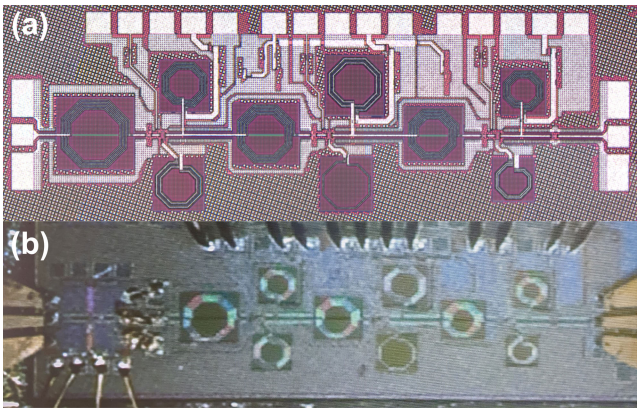

Fig. 4. Fabricated LNA chip. (a) Micrograph (dimensions: 0.63 × 1.95 mm) and (b) wire-bonded to input attenuator with probes landed. An on-chip temperature sensor within 10 μm of the attenuator is used for calibration. Its four leads are well thermalized to minimize heating.

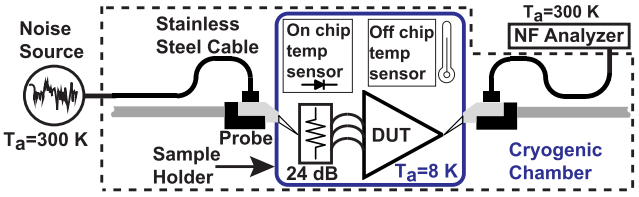

Fig. 5. Cryogenic on-wafer noise measurement block diagram.

a lower current density of 29 mA/mm to minimize power consumption. The output network was designed to provide matching to 50 Ω.

At cryogenic temperatures, the quality factor associated with the optimum noise match, $Q_{OPT} = X_{OPT}/R_{OPT}$, increases from its room temperature value of ∼1.3 to ∼7. As such, minimizing input-matching network losses is critical. Here, we use inductive degeneration of M_1 to achieve simultaneous noise/input match and an inductor in series with the gate of M_1 to provide reactive matching. The gate inductor was optimized via electromagnetic simulations, using a metal stack with 5× the conductivity and 1000× the substrate resistivity than that of room temperature values. The RC supply filtering reduces parasitic feedback, improving stability. The simulation results, shown in Fig. 3, predict a significant rise in quality factor with cryogenic cooling. A common back-gate control allows tuning of the transistor threshold voltages (V_T).

IV. AMPLIFIER CHARACTERIZATION

The LNA was fabricated in GF22FDX, and a die micrograph appears in Fig. 4(a). The LNA's S-parameters were first measured on-wafer at a physical temperature of 8 K. Next, the amplifier was wire-bonded to an on-chip 24-dB

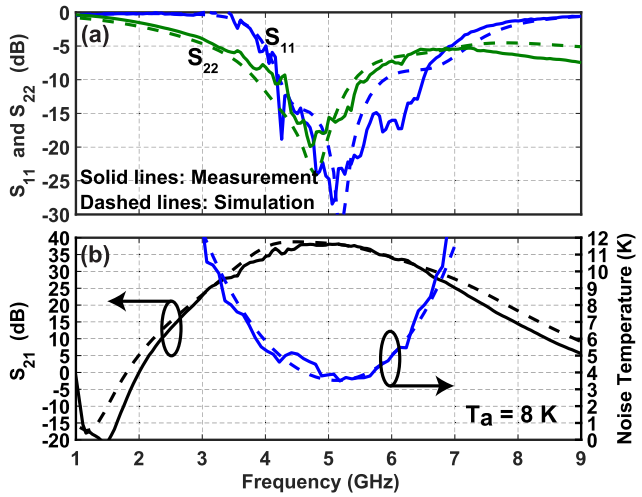

Fig. 6. On-wafer measurements at 8 K. (a) Input and output reflection coefficient. (b) Gain and noise temperature. The LNA is biased at $V_{DD} = 0.6$ V and $I_{DD} = 26.3$ mA.

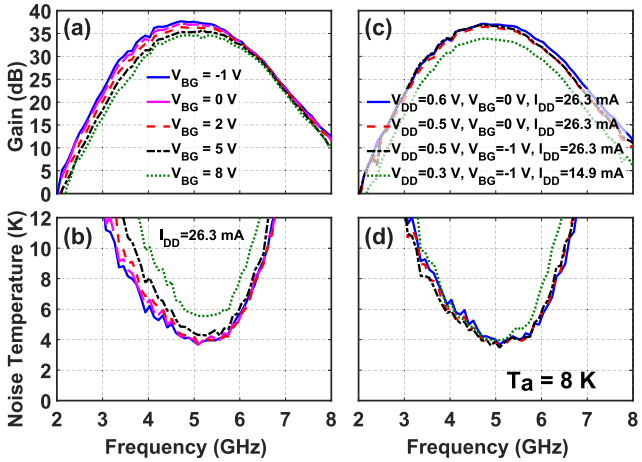

Fig. 7. Effect of back-gate bias and V_{DD} on LNA performance. (a) Gain and (b) noise temperature at constant $V_{DD} = 0.6$ V and $I_{DD} = 26.3$ mA for different values of V_{BG}. (c) Gain and (d) noise temperature as a function of V_{DD} and V_{BG}. For the low current bias of (c) and (d), $I_{D1} = 5.5$ mA, $I_{D2} = 5.3$ mA, and $I_{D3} = 4.1$ mA.

attenuator for on-wafer cryogenic noise measurement using the cold attenuator method [19]. The test setup for this measurement appears in Fig. 5, while a photograph of the chip configuration, including wirebonds and probes, appears in Fig. 4(b). Through use of a 24-dB attenuator (as opposed to the more standard 20-dB value used for coaxial measurements) and careful calibration of losses and the attenuator's physical temperature, we estimate that the measurement uncertainty is limited to ± 1.1 K ($\pm 2\sigma$).

Measurement results and corresponding simulations for the LNA at its nominal bias ($V_{DD} = 0.6$ V, $I_{D1} = 9.9$ mA, $I_{D2} = 9.6$ mA, and $I_{D3} = 6.8$ mA) appear in Fig. 6. It achieved a peak gain of 38 dB at 5 GHz and an input return loss of >10 dB from 4.2 to 6.5 GHz. The LNA achieved a noise temperature of 3.5 K at 5.2 GHz while consuming 15.8 mW from a 0.6-V supply. The average T_e measured at a physical temperature of 8 K from 4 to 6 GHz is 4.4 K. The excellent agreement between measured and simulated T_e supports our assumption that F does not change with cooling. At this bias point, the input $P_{1\,dB}$ was greater than -40 dBm, greatly exceeding the requirements for qubit readout. We note that,

TABLE II

COMPARISON TABLE WITH STATE-OF-THE-ART CRYO-CMOS LNAS. FOM $= G_{dB} \times (f_h/f_l) \times (hf_0/kT_e) \times (1/P_{DC})$

Ref.	Tech. node	Frequency (GHz)	Gain (dB)	$T_{Physical}$ (K)	Average T_e (K)	P_{DC} (mW)	FOM (dB/mW/ph)
[9]	40 nm	4.6 - 8.2	42	4.2	28	39	0.02
[10]	14 nm	5.9 - 8.4	13.4	4.1	39	2.57	0.065
[11]	28 nm	6 - 8	50*	4.2	39	4.2	0.137
[12]	22 nm	4.2 - 9.2	33	16	11.4	21	0.097
[13]	65 nm	3.6 - 5.3	35	16	11.4	10.6	0.091
This	**22 nm**	**4 - 6**	**37**	**8**	**4.4**	**15.8**	**0.192**
This^	**22 nm**	**4 - 6**	**33**	**8**	**5.1**	**4.5**	**0.517**

^ Low power bias * Minimum gain

when biased for similar g_m, the amplifier achieved $T_e \sim 170$ K at room temperature.

To study the effect of back-gate bias (V_T control), the LNA was measured at its nominal V_{DD} and I_{DD}, while V_{BG} was varied from -1 to 8 V. More positive V_{BG} corresponds to a decrease in V_T. As shown in Fig. 7(a) and (b), the gain and noise performance are best at $V_{BG} = -1$ V, which corresponds to the highest value of V_T. While biasing V_{BG} to reduce V_T could allow a lower value of V_{DD}, this result indicates that the corresponding reduction in power consumption will come at the cost of lower gain and higher noise.

We evaluated this trade-off between dc power and RF performance, first reducing V_{DD} to 0.5 V and then adjusting V_{BG} to optimize performance. Finally, the currents were reduced by $\sim$40%, and V_{DD} was dropped to 0.3 V. The measurement results at each step of the optimization appear in Fig. 7(c) and (d). At the lowest power bias, the LNA achieved a peak gain of 34 dB with 5.1-K average T_e while consuming 4.5 mW, which is 3.5$\times$ lower than that at the nominal bias point.

V. CONCLUSION

The LNA is compared with other cryo-CMOS LNAs in Table II. We introduce a figure of merit (FOM), similar to that used in [13], which quantifies the trade-off among relative bandwidth, gain, noise and power consumption. To the best of authors' knowledge, this LNA has the best FOM of cryo-CMOS LNAs reported in the literature to date. The measured FOM for the LNA surpasses the previous state-of-the-art by up to a factor of 3. At its nominal bias, it achieves the lowest reported noise for a cryo-CMOS amplifier in this frequency range, and its bias can be reduced to 4.5 mW with only a minor degradation to the performance. While this work marks important progress toward meeting the requirements of large-scale superconducting qubit readout systems, future work should focus on further reducing the noise and power consumption of cryo-CMOS LNAs.

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