A 240-GHz 4-TX 4-RX 2-D-MIMO FMCW Radar Transceiver in 130-nm SiGe BiCMOS

Christoph Mangiavillano, Alexander Kaineder, Thomas Wagner, *Member, IEEE*, and Andreas Stelzer, *Member, IEEE*

***Abstract*— A 240-GHz 4-transmitter (TX) 4-receiver (RX) 2-D multiple-input–multiple-output (MIMO) frequency-modulated continuous-wave (FMCW) radar transceiver was designed in a 130-nm SiGe bipolar CMOS (BiCMOS) technology with f_T/f_{max} of 250/370 GHz using patch antennas on a single 4.032 × 4.032 mm^2 chip. The differential RF inputs, located at the emitters of the direct conversion mixer quad transistors of each RX channel are dc-coupled and current-matched to the differential on-chip patch antenna. At 240 GHz, measurements reveal an RX conversion gain of 24.8 dB, a single-sideband noise figure of 14.9 dB, and an output power of −2 dBm.**

***Index Terms*— Frequency-modulated continuous-wave (FMCW) radar, industrial, scientific and medical (ISM) band, *J*-band, mixer, multiple-input–multiple-output (MIMO), multiplier, on-chip antenna, SiGe bipolar CMOS (BiCMOS).**

I. Introduction

RADAR imaging applications benefit from the economies of scale offered by CMOS and SiGe bipolar CMOS (BiCMOS) technologies, supported by an approximate tripling in the number of yearly silicon-integrated radar publications on IEEE Xplore in the past 15 years [1]. Multiple-input–multiple-output (MIMO) frequency-modulated continuous-wave (FMCW) radars in silicon technologies are demonstrated up to the *D*-band, for example, as multichip assemblies [2], [3], [4], [5], [6], [7]. In the 244–246-GHz industrial, medical, and scientific band, multichip solutions will struggle to achieve an unambiguous half-space, as $\lambda/2 = 612\ \mu$m, smaller than typical single-channel *J*-band FMCW radar transceiver chip dimensions [8], [9], [10], [11], [12], [13]. For a 2-D-MIMO application, signal-to-noise ratio (SNR) improvements using external lenses [8], [9] are not feasible. Furthermore, improving gain of the on-chip antenna using large arrays [13] or selective localized backside etching [12] will increase array element spacing to values larger than $\lambda/2$. Thus, in a single-chip 240-GHz 2-D-MIMO transceiver, the overall SNR is to be maximized by optimizing the transmitted power (P_T) and noise figure (F_N), primarily, while at the same time maintaining a low dc power (P_{dc}) consumption for multichannel operation.

In this work, we introduce a 240-GHz 4-transmitter (TX) 4-receiver (RX) 2-D-MIMO FMCW radar transceiver with on-chip antennas, designed in a 130-nm SiGe BiCMOS technology with an f_T/f_{max} of 250/370 GHz. Compared to the previous 1-TX 1-RX 240-GHz transceiver [13], several improvements have been introduced to achieve 4-RX and 4-TX channels in a similar power and area budget. The final frequency-doubler stage, previously implemented using a quadrature push–push topology, is now replaced with a bootstrapped Gilbert-cell circuit [14] for the reduced area. The RX now uses a direct conversion mixer with current matching and dc-coupling to the on-chip antennas at the RF input, rather than a subharmonic mixer [15], resulting in an improvement of the single-sideband noise figure (NF_{SSB}) from 20 to around 14.9 dB, using the same technology.

II. Transceiver Design

The block diagram of the 240-GHz 2-D-MIMO transceiver is shown in Fig. 1(a), together with the resulting virtual 2 × 8 array. An external local oscillator (LO) signal is fed into the transceiver chip at 20 GHz. A ×12 frequency multiplier chain, detailed in Fig. 2, consisting of a single-transistor active balun, a cascoded differential pair tripler, and two cascaded bootstrapped frequency doublers [14], is utilized to achieve a 240-GHz signal. A series of differential 60-GHz branchline couplers with a modeled attenuation of 4.5 dB, including power division, split the LO signal into the RX and TX channels. To achieve sufficient driving amplitudes after the LO-distribution, 60-GHz amplifiers, as shown in Fig. 3(a), are implemented before and after the couplers. On the RX side, a direct conversion mixer is utilized, depicted in Fig. 3(b). The topology is similar to [16] and [17], although, in this work, the operation at 240 GHz is demonstrated using a technology with f_T of 250 GHz, rather than f_T of more than 300 GHz. Additionally, the radio-frequency (RF) input at the emitters of Q_{1-4} is current-matched and dc-connected to the on-chip RX antenna, without the need for additional matching circuitry. The dc-coupled 500-Ω resistor is placed at the $\mathbf{E}_0$ of the antenna and is thus isolated from the RF. A resistor-defined current is mirrored by a one-to-one current mirror in Fig. 3(b) and a one-to-four current mirror in Figs. 2 and 3(a), with differential circuits using two mirrors for improved symmetry. The bias voltages of the input transistors are generated using the current mirror transistor, while the cascode bias

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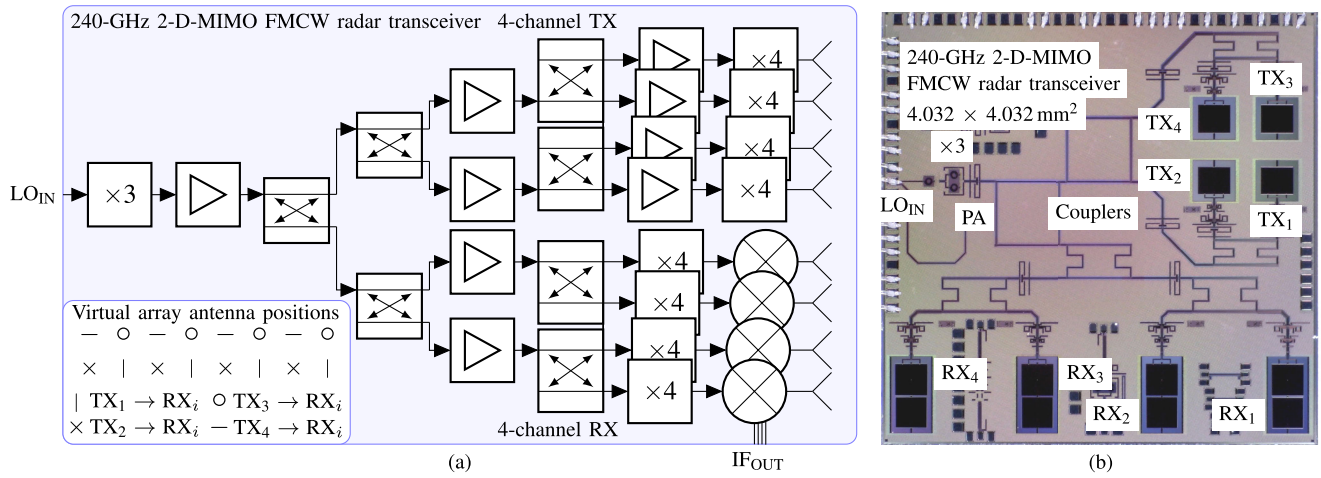
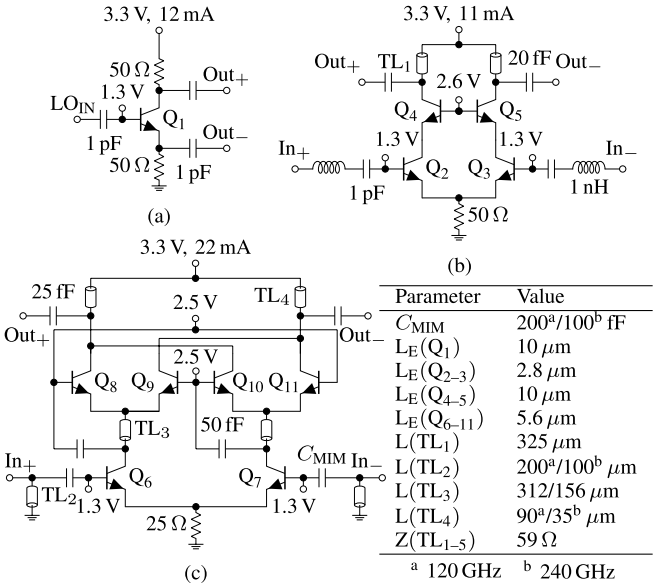


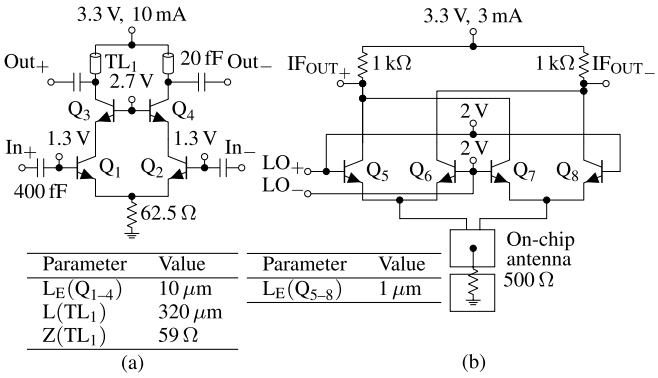
Fig. 1. 240-GHz 2-D-MIMO FMCW radar transceiver. (a) Block diagram and virtual 2 × 8 array with $\lambda/2$ interelement spacing. (b) Chip micrograph.



Parameter	Value
C_{MIM}	200[a]/100[b] fF
$L_E(Q_1)$	10 μm
$L_E(Q_{2-3})$	2.8 μm
$L_E(Q_{4-5})$	10 μm
$L_E(Q_{6-11})$	5.6 μm
$L(TL_1)$	325 μm
$L(TL_2)$	200[a]/100[b] μm
$L(TL_3)$	312/156 μm
$L(TL_4)$	90[a]/35[b] μm
$Z(TL_{1-5})$	59 Ω

[a] 120 GHz [b] 240 GHz

Fig. 2. Schematics of the (a) 20-GHz balun, (b) 20–60-GHz tripler, and (c) 120- and 240-GHz doubler. Current consumption includes biasing.



Parameter	Value
$L_E(Q_{1-4})$	10 μm
$L(TL_1)$	320 μm
$Z(TL_1)$	59 Ω

Parameter	Value
$L_E(Q_{5-8})$	1 μm

Fig. 3. Schematic of the (a) 60-GHz amplifier and (b) 240-GHz mixer. The input of the 60-GHz amplifier is matched using a 100-Ω differential line of 60-μm length. The LO-input of the 240-GHz mixer is matched using two 40-μm 59-Ω shorted stubs, followed by a 45-μm 100-Ω differential line in series with two 25-fF capacitors, connected to the LO_+ and LO_- ports, respectively. Current consumption includes biasing.

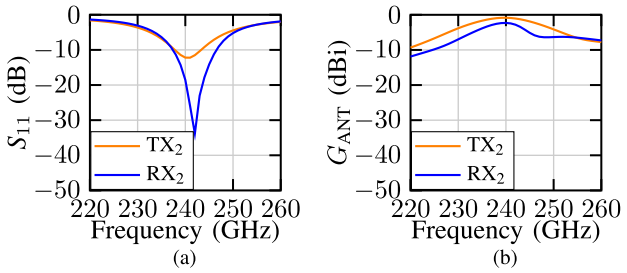


Fig. 4. On-chip antenna simulation of (a) S_{11} and (b) realized gain.

voltages are generated using a resistive divider, integrated into the same current mirror above the mirror transistor. Emitter resistors are chosen accordingly for the current mirror factor and provide improved tolerance against process variations. Fig. 4(a) and (b) depicts the simulated input matching and realized gain (G_{ANT}) of the on-chip antennas, for the second TX and RX. The TX and RX antennas are spaced $\lambda/2$ and λ, respectively. From 220 to 260 GHz, the simulated isolation between TX and RX antennas is better than 50 dB, and therefore the simulated RX mixer RF input compression point of −7 dBm will be sufficient, considering a typical simulated TX output power (P_{out}) of −1 dBm.

III. Measurements

Over-the-air measurements are performed with the 240-GHz MIMO radar transceiver, mounted on a rotational stage in an optical-bench-like setup at a distance of 15 cm. The output power of a J-band converter, used in the TX mode for the characterization of the chip RXs, is measured using a power meter. The receiving J-band up/down mixer is connected to the signal and spectrum analyzer for effective isotropic radiated power (EIRP) measurements. Fig. 5 presents the simulated and measured normalized antenna gain patterns of TX_2 and RX_2. At 240 GHz, Fig. 6(a) demonstrates a measured system conversion gain (CG) of 24.8 dB and a minimum NF_{SSB} of 14.9 dB for RX_2. In Fig. 6(b), the simulated and measured P_{out} and EIRP are shown for TX_2. Radar

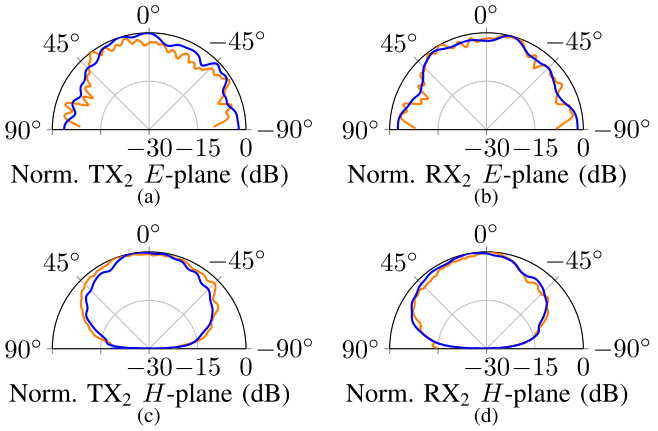


Fig. 5. Measurement (–) and simulation (–) of normalized antenna: (a) E-plane of TX_2, (b) E-plane of RX_2, (c) H-plane of TX_2, and (d) H-plane of RX_2 at $f_{RF} = 240$ GHz.

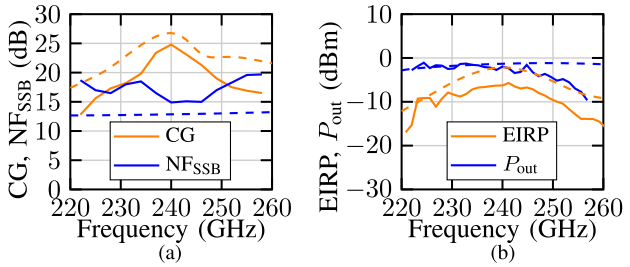


Fig. 6. Measurement (solid) and simulation (dashed) of (a) system gain and noise figure of RX_2 (with 31-dB analog front-end gain) at $f_{IF} = 500$ kHz using the gain method from [18] and (b) EIRP of TX_2 and probed on-wafer output power of the ×12 frequency multiplier chain.

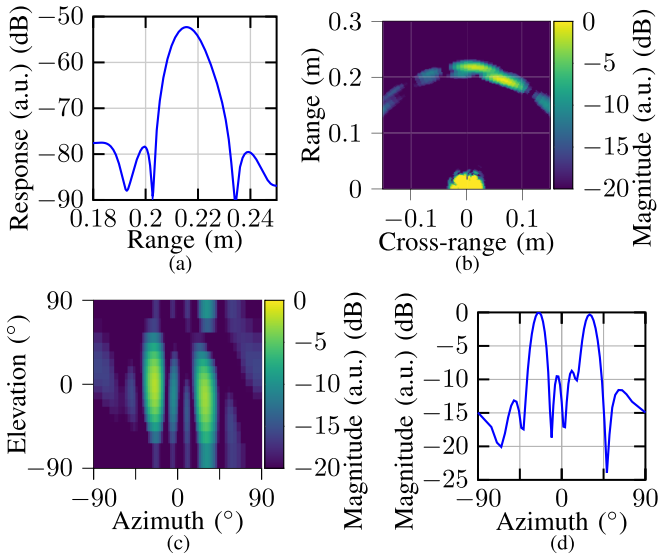


Fig. 7. FMCW radar measurement with 24 GHz of RF bandwidth of (a) single target and channel, (b) 1-D beamformed response of two targets separated by ≈2 cm in range, (c) 2-D beamformed response of two targets at 22 cm separated by ≈55° in azimuth, and (d) corresponding azimuth cut. Targets are −15.6-dBsm trihedral corner reflectors with 1 cm side length.

measurements in Fig. 7 use an onboard frequency source with a linear frequency sweep from 19.4 to 21.4 GHz in 1 ms, resulting in 24 GHz of RF bandwidth, considering the ×12 multiplication factor of the transceiver. A detailed description of a similar demonstrator platform can be found in [13] and

TABLE I
SILICON-INTEGRATED FMCW RADAR TRANSCEIVERS IN THE J-BAND

f_{max}/f_{RF} (GHz)	TX/RX/ MIMO	P_{out}/P_{dc} [b] (mW)	NF_{SSB} (dB)	FoM [c] (dB)	Ref.
280/220–320	1/1/No	0.3[a]/168	22.2	1.2	[8]
370/198–250	1/1/No	1.5/-	18.8[a]	-	[9]
370/204–265	1/1/No	1.0/750	17.0[a]	5.4	[10]
450/210–270	1/1/No	3.2/1600	21.1	3	[11]
500/234–254	1/1/No	0.3/305	20.5[a]	0.6	[12]
370/232–238	1/1/No	1.0/1300	20.0	0.0	[13]
370/233–257	**4/4/2×8**	**0.6/366**	**14.9**	**8.4**	**This**

[a] Sim. [b] $P_{dc_{1\text{-TX, 1-RX}}}$ [c] $\text{FoM} = P_{out_{dBm}} - NF_{SSB_{dB}} - P_{dc_{dBm}} + 51.1$

[19]. From Fig. 7(a), a peak-to-null range resolution [20] of 7.5 mm can be estimated, considering the Hann window, which is used to improve sidelobe suppression at the cost of twice as large peak-to-null width, when compared to a boxcar window. The peak is wider than the theoretical range resolution of 6.25 mm, due to amplitude shaping on the RF signal caused by the bandwidth-limited on-chip antennas [9]. The SNR from Fig. 7(a) can be compared to the expected SNR from the following equation:

$$\text{SNR} = \frac{P_T G_{TX} G_{RX} \lambda^2 \sigma}{(4\pi)^3 R^4 k_B T_0 B F_N} \tag{1}$$

with $P_T = -1.6$ dBm, TX antenna gain $G_{TX} = -1.6$ dBi, RX antenna gain $G_{RX} = -5$ dBi, wavelength $\lambda = 1.23$ mm, target radar cross section $\sigma = -15.6$ dBsm, target distance $R = 0.22$ m, Boltzmann's constant k_B, temperature $T_0 = 300$ K, noise bandwidth $B = 1$ kHz, and $F_N = 15$ dB, at 244.8 GHz. The SNR of 33 dB from (1) is calculated, in agreement with the measurement. Fig. 7(b) emphasizes the benefit of 24 GHz of RF bandwidth, allowing two targets separated by 2 cm in range to be distinguished even though their angular separation is below the theoretical angular resolution of 14.3° at broadside. In Fig. 7(c), the 2-D-MIMO beamformed response is given for two trihedral corner reflectors with −15.6 dBsm, placed at 22 cm in range and separated by 55° in azimuth, with the azimuth cut shown in Fig. 7(d). An angular resolution of 14.6° in azimuth is estimated from the 3-dB beamwidth, in agreement with the theoretical value of 14.3°. To the authors' best knowledge, this work is the first demonstration of an MIMO FMCW radar at 240 GHz using silicon-integrated technologies and compares favorably with state-of-the-art silicon-integrated single-channel J-band FMCW radar transceivers in terms of the figure-of-merit (FoM), illustrated in Table I.

IV. CONCLUSION

A miniaturized and efficient 240-GHz 4-TX 4-RX 2-D-MIMO FMCW radar transceiver has been designed in a 130-nm SiGe BiCMOS technology with an f_T/f_{max} of 250/370 GHz using patch antennas on a single 4.032×4.032 mm^2 chip. Current matching is used in the direct conversion mixer RF-input, dc-coupled to the on-chip antenna. At 240 GHz, an RX CG of 24.8 dB, a NF_{SSB} of 14.9 dB, and a P_{out} of −2 dBm have been measured.

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