A 7–115-GHz Distributed Amplifier With 24-dBm Output Power Using Quadruple-Stacked HBT in InP

Nguyen L. K. Nguyen, *Member, IEEE*, Can Cui, *Graduate Student Member, IEEE*, Duy P. Nguyen, *Member, IEEE*, Alexander N. Stameroff, *Member, IEEE*, and Anh-Vu Pham, *Fellow, IEEE*

***Abstract*— In this letter, we present the designs and development of a wideband, high output power quadruple-stacked heterojunction bipolar transistor (HBT) distributed amplifier (DA). In particular, the stacked HBT configuration can improve gain and output power while achieving a very wide bandwidth. To validate the proposed design concept, a quadruple-stacked HBT DA is designed in an indium phosphide (InP) process. The measurement results show an average gain of 16 dB from 7–115-GHz bandwidth with a maximum of 24-dBm saturated output power (P_{sat}). To the best of the authors' knowledge, this is the first time quadruple-stacked HBT is used in a DA to achieve the highest output power compared with other published work in the same frequency range.**

***Index Terms*— 6G, distributed amplifier (DA), heterojunction bipolar transistor (HBT), indium phosphide (InP), millimeter wave (mm-W), stacked HBT, wideband.**

I. Introduction

MILLIMETER-WAVE (mm-W) power amplifiers have been the focus of academic research and industry innovation, since the demand for high-speed communication systems [1], high-resolution radars [2], and 5G/6G measurement instrumentation [3] is increasing rapidly [4]. Various demonstrations have been introduced in III–V technologies, such as gallium nitride (GaN), gallium arsenide (GaAs), and indium phosphide (InP) [5], [6], [7]. In addition, silicon-based processes, such as complementary metal–oxide–semiconductors (CMOS), silicon on insulator (SOI), and silicon germanium (SiGe), are also heavily investigated [8], [9], [10], [11], [12].

InP has been proven to be a good technology at frequencies beyond 100 GHz with typical process parameters reported in [3] and [6] that offers high cutoff frequency fT, high breakdown voltage, low loss substrate, and reasonable efficiency [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. A 175-GHz InP distributed amplifier (DA) is presented in [23] that achieves 10-dBm output power and 12 dB of gain. In [24], an 11.5-dBm output power with 13 dB of gain DA covering more than 110-GHz bandwidth is presented. Several design techniques have also been introduced to improve the output power, gain, and bandwidth of InP DAs [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. Specifically, stack configurations of up to three heterojunction bipolar transistor (HBT) devices have been deployed for InP amplifiers to increase the power up to 100 mW [12], [13], [14], [15], [16], [17], [18], [19]. Although great efforts have been made to extend the operating bandwidth and power, previously published works have not demonstrated an output power up to 250 mW while maintaining a bandwidth above 100 GHz.

In this letter, we present the design of high-power, wideband DAs in an InP technology. To achieve a high output power, a quadruple-stacked HBT DA is employed. The DA achieves a 7–115-GHz bandwidth with a 16-dB average gain. The maximum achievable saturate output power (P_{sat}) is 24 dBm, with the corresponding output power at 1-dB compression ($P_{1\,dB}$) of 21.6 dBm. To the best of the authors' knowledge, this is the first time a quadruple-stacked using InP HBT device is utilized in a DA configuration. In addition, the proposed quadruple-stacked DA achieves the highest output power among reported DAs with similar or larger bandwidths.

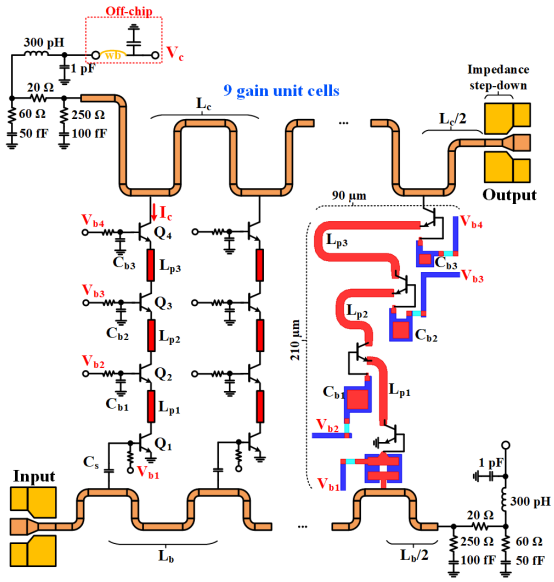


Fig. 1. Complete diagram and layout of the nine-stage quadruple-stacked HBT DA.

II. Circuit Design and Implementation

Fig. 1 illustrates the schematic of the proposed distributed power amplifier with the layout of the quadruple-stacked gain cell shown for the last stage. Since the loaded input line is a lossy transmission line due to the series base resistance

Manuscript received 1 October 2022; revised 18 December 2022; accepted 12 January 2023. Date of publication 23 January 2023; date of current version 7 June 2023. *(Corresponding author: Nguyen L. K. Nguyen.)*

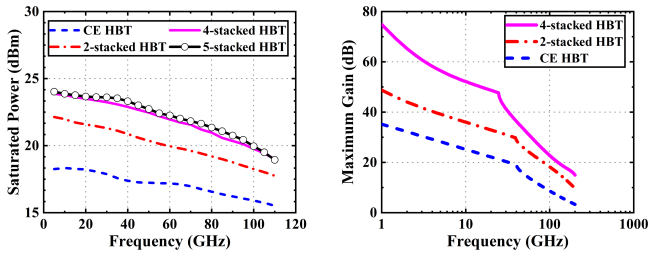
Nguyen L. K. Nguyen, Can Cui, and Anh-Vu Pham are with the Department of Electrical and Computer Engineering, University of California at Davis, Davis, CA 95616 USA (e-mail: nlknguyen@ucdavis.edu).

Duy P. Nguyen was with the Department of Electrical and Computer Engineering, University of California at Davis, Davis, CA 95616 USA. He is now with MACOM Technology Solutions, Santa Clara, CA 95050 USA.

Alexander N. Stameroff is with Keysight Technologies, Santa Rosa, CA 95403 USA.

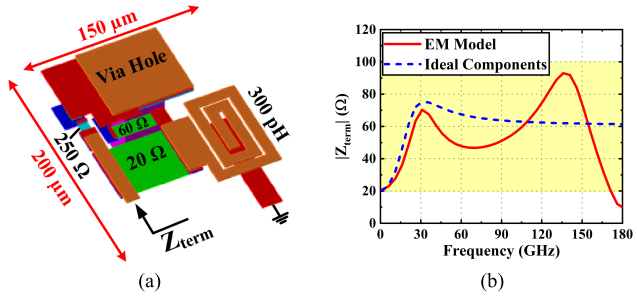
Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWT.2023.3237683.

Digital Object Identifier 10.1109/LMWT.2023.3237683



(a) (b)

Fig. 2. (a) Simulated output power of a nine-stage k-stacked 10-μm HBT. (b) Simulated maximum gain of different unit gain cells using 10-μm transistor.



(a) (b)

Fig. 3. (a) Compact layout and (b) simulated impedance of the wideband termination network.

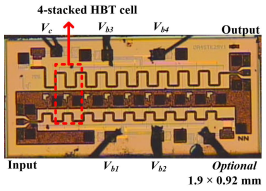


Fig. 4. Chip photograph of the quadruple-stacked HBT DA.

of the HBT devices, the traveling input signal is gradually attenuated toward the termination resistor. As a result, there exists an optimal number of stages from which no input signal is further amplified due to the heavy attenuation. Hence, it is observed from the simulation that the gain and output power of the DA no longer increase, as the number of stages exceeds nine. At the same time, as the stacking order increases, the phase misalignment becomes more profound and causes the voltage swing not to add up in phase [1]. Moreover, the smaller base capacitance at higher stacked HBT leads to a more severe leakage current to the base that detrimentally impacts the output current phasor [27]. Therefore, stacking beyond four transistors does not indicate any output power improvement, as shown in Fig. 2(a). Fig. 2(b) demonstrates the maximum available gain of a single common emitter, a double-stacked HBT, and a quadruple-stacked HBT gain unit cell. At 110 GHz, the quadruple-stacked HBT provides ≈5 and 14 dB compared with the double-stacked and the single common-emitter topology, respectively. Therefore, in order to achieve above 22-dBm output power with the operation frequency covering up to W-band, a quadruple-stacked HBT with input capacitive coupling is employed. Furthermore, a compact on-chip wideband termination network is developed to provide wideband matching while providing an on-chip dc bias scheme.

The transistor Q_1–Q_4 is 10 μm in length with a nominal quiescent current of 12.5 mA. The base capacitors for Q_2–Q_4 are valued at 92, 60, and 25 fF, respectively. The values of these capacitors reduce gradually, as the stacking goes up to provide a proper voltage swing at each transistor. Each transistor's base terminal is biased through a 1-kΩ resistor. Peaking inductors are employed between each transistor to extend the bandwidth. The input line base inductance, L_b, and the output collector line inductance, L_c, are 60 and 90 pH, respectively, with a termination resistor of $R_{term,b} = R_{term,c} = 60\ \Omega$. An impedance step-down matching is implemented with the output RF pad to achieve better matching. Both input and output inductors are realized using a high-impedance microstrip line.

The quadruple-stacked HBT DA employs a wideband on-chip biasing circuit to eliminate the use of an external bias tee. The output termination network is designed to have an effective impedance of around 60 Ω. Fig. 3(a) shows the layout of the wideband termination network. The wideband termination with a wideband on-chip biasing network features a very compact design with a size of 200 × 150 μm. Fig. 3(b) demonstrates the simulated impedance of the termination network using ideal components and electromagnetic (EM) models. Although the frequency limitation of the EM model is due to the nonideal spiral inductor, the impedance is kept within the −10-dB matching region from 20 to 100 Ω up to 170 GHz. The input termination can utilize a similar network for the purpose of biasing the previous stage if necessary.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED DA

Design parameters		Four-stacked DA
Number of stages	N	9
Emitter length	L_e	10 μm
Bias conditions	V_c	10 V
	I_c	12.5 mA
	$V_{b1}, V_{b2}, V_{b3}, V_{b4}$	1.15, 2.1, 4.2, 5.8 V
Capacitors	C_s	20 fF
	C_{b1},C_{b2},C_{b3}	92, 60, 25 fF
Inductors	L_b, L_c	60, 95 pH
	L_{p1}, L_{p2}, L_{p3}	30, 43, 55 pH
Terminations	*Output*	60 Ω
	Input	60 Ω
Chip size	$L \times W$	1.9 × 0.92 mm^2

At each input of the stacked HBT gain cell, a coupling capacitor, $C_s = 20$ fF, is used to improve bandwidth and provide a dc block at the input terminal. The coupling capacitor C_s is designed using four identical metal–insulator–metal (MIM) capacitors connected in a series and parallel configuration to reduce the effects of process variation [16]. The chip photograph of the quadruple-stacked HBT DA is shown in Fig. 4. The total chip size is 1.9 × 0.92 mm, including all pads. The input and output ports of the DA are connected to 100-μm pitch ground–signal–ground (GSG) pads. The design parameters are summarized in Table I.

III. EXPERIMENTAL RESULTS

The proposed amplifier is designed and fabricated in an InP HBT process [17]. The InP process has a transition frequency f_T of 290 GHz and a maximum frequency f_{max} of 390 GHz. The nominal device collector junction current bias condition is $J_c = 1.3$–1.6 mA/μm at an ambient temperature $T_a = 25$ °C. The process offers high-quality factor MIM capacitors with low-loss thin-film dielectric wirings. The prototype is built on a test printed circuit board (PCB) substrate with the voltage supply pads being wire bonded onto a 500-pF single-layer capacitor. The bases of the transistors Q_1–Q_4 are biased at 1.15, 2.1, 4.2, and 5.8 V, accordingly. Note that the

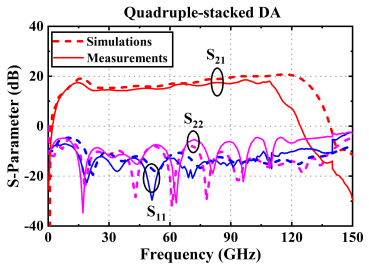


Fig. 5. Measured and simulated S-parameters of the quadruple-stacked DA.

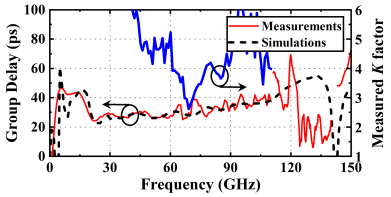


Fig. 6. Measured and simulated group delay and stability factor of the DA.

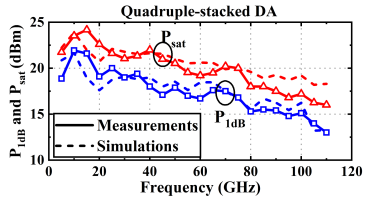


Fig. 7. Measured and simulated P_{sat} and $P_{1\,\text{dB}}$ over the frequency of the DA.

collector–emitter bias voltage of Q_1 is lower than the rest to optimize for the gain and power performance. The biasing pad at the bottom right of the chip can be used as a wideband bias tee for a previous stage if necessary.

Fig. 5 illustrates the small-signal S-parameter measurements of the proposed quadruple-stacked HBT DA. The solid lines are the measured results, and the dashed lines represent the simulated ones. The amplifier achieves an average gain of 16 dB, covering a bandwidth from 7 to 115 GHz. The input return loss remains below −10 dB, and the output return loss is better than −8 dB across the operating frequency. Overall, the simulations relatively predict the measurement results of the amplifier with a slight reduction in bandwidth. One possible reason for the degradation could be severe couplings from the output transmission line to the ground planes and the adjacent dc biasing traces.

Fig. 6 presents the measured stability factor K and the group delay in picosecond (ps). The DA is unconditionally stable with $K > 1$, and $|\Delta|$ is verified to be less than one. From 10 to 110 GHz, the quadruple-stacked DA has a group delay variation of ±10 ps. The small-signal measurements are conducted in different frequency bands: 0–67 GHz (1.85-mm coaxial cable), 67–110 GHz (WR-10 waveguide), 110–140 GHz (WR-6 waveguide), and 140–180 GHz (WR-5 waveguide) using a Keysight vector network analyzer (PNA-X) and appropriate frequency extenders. The calibration is done using short-open-load-thru (SOLT) below 67 GHz and thru-reflect-line (TRL) for the waveguide bands above 67 GHz.

Figs. 7 and 8 demonstrate the measured and harmonic balance simulated large-signal characteristics of the proposed DA. The maximum achievable P_{sat} is 24 dBm, with the corresponding $P_{1\,\text{dB}}$ of 21.6 dBm, as shown in Fig. 7. The DA can still provide 16-dBm P_{sat} at the 3-dB bandwidth 115 GHz. The proposed quadruple-stacked HBT DA achieves a power roll-off slope of 0.85 dB/10 GHz across the bandwidth. Fig. 8 illustrates the power sweep measurement at 25 and 75 GHz. At 75 GHz, the quadruple-stacked DA achieves a measured P_{sat} of 20 dBm, a $P_{1\,\text{dB}}$ of 16.9 dBm, and a maximum power added efficiency (PAE) of 6.8%. Table II summarizes the performance of state-of-the-art wideband amplifiers in the same frequency range. Only [27] achieves up to 23.5-dBm output power using a quadruple-stacked FET in SOI technology. However, the bandwidth in [27] is limited to 104 GHz with a power roll-off slope of 3.83 dB/10 GHz, which is 2.98 dB higher than our work. To the best of our knowledge, the quadruple-stacked DA achieves the highest output power among the reported DAs with similar or higher bandwidth to date.

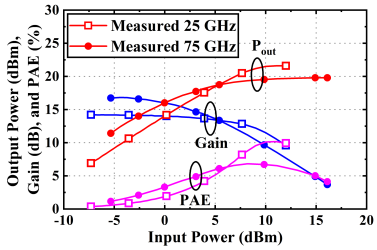


Fig. 8. Measured output power, gain, and PAE of the DA at 25 and 75 GHz.

TABLE II
COMPARISON WITH STATE-OF-THE-ART WIDEBAND POWER AMPLIFIERS

Reference	Process	Gain (dB)	BW (GHz)	f_T/f_{max} (GHz)	$P_{sat,\,max}$ (dBm)	PAE (%)	Die size (mm^2)
[20]	InP	10	38-220	375/650	9.2 @77GHz	5 @77 GHz	0.33
[21]	InP	17.8	96-122	400/700	20.2 @110GHz	22.5 @110 GHz	0.38
[22]	InP	10	40-105	270/750	12 @92GHz	43 @93 GHz	0.73
[19]	InP	10.5	60-145	290/390	20.9 @75GHz	19.2 @110 GHz	0.96
[8]	SiGe	8.5	dc-135	230/300	11 @20GHz	-	0.36
[25]	SiGe	12	14-105	300/-	17 @50GHz	12.6 @50 GHz	1.51
[26]	SiGe	14.5	52-142	-/210	1.6 @75GHz	-	0.45
[9]	SOI	16	1.5-103	290/250	22 @5GHz	19.5 @5 GHz	0.33
[27]	SOI	33	2.5-104	290/250	23.5 @15GHz	19 @15 GHz	0.58
[28]	GaAs	11	dc-110	380/500	11 @75GHz	-	1.69
This Work	**InP**	**16**	**7-115**	**290/390**	**24 @15GHz**	**6.8 @75 GHz**	**1.75**

IV. CONCLUSION

In this letter, we demonstrate the development of a high-power and wide bandwidth quadruple-stacked HBT DA. A nine-stage DA is designed and fabricated in an InP process offering an f_T/f_{max} of 290/390 GHz. The amplifier achieves a 16-dB gain over 7–115-GHz bandwidth. The maximum P_{sat} is 24 dBm, with a corresponding $P_{1\,\text{dB}}$ of 21.6 dBm.

ACKNOWLEDGMENT

The authors would like to thank the support of Keysight Technologies, Santa Rosa, CA, USA, under the Core Technology University Research Program.

REFERENCES

[1] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013.

[2] L. Zhang, N. L. K. Nguyen, J. Chen, O. Momeni, and X. Liu, "A 3.2 mW 2.2–13.2 GHz CMOS differential common-gate LNA for ultra-wideband receivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 715–718.

[3] Global Communication Semiconductors. *InP HBT Technologies*. gcsincormp.com. Accessed: Dec. 17, 2022. [Online]. Available: http://www.gcsincorp.com/dedicated_pure-play_wafer_foundry/InP%20HBT%20Technologies.php

[4] G. Nikandish, R. B. Staszewski, and A. Zhu, "The (R)evolution of distributed amplifiers: From vacuum tubes to modern CMOS and GaN ICs," *IEEE Microw. Mag.*, vol. 19, no. 4, pp. 66–83, Jun. 2018.

[5] K.-L. Deng, T.-W. Huang, and H. Wang, "Design and analysis of novel high-gain and broad-band GaAs pHEMT MMIC distributed amplifiers with traveling-wave gain stages," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 11, pp. 2188–2196, Nov. 2003.

[6] M. J. W. Rodwell, M. Le, and B. Brar, "InP bipolar ICs: Scaling roadmaps, frequency limits, manufacturable technologies," *Proc. IEEE*, vol. 96, no. 2, pp. 271–286, Feb. 2008.

[7] A. Margomenos et al., "70–105 GHz wideband GaN power amplifiers," in *Proc. 7th Eur. Microw. Integr. Circuit Conf.*, Oct. 2012, pp. 199–202.

[8] J. Hoffman, S. P. Voinigescu, P. Chevalier, A. Cathelin, and P. Schvan, "A low noise, DC-135GHz MOS-HBT distributed amplifier for receiver applications," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2015, pp. 1–4.

[9] O. El-Aassar and G. M. Rebeiz, "A compact pMOS stacked-SOI distributed power amplifier with over 100-GHz bandwidth and up to 22-dBm saturated output power," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 2, pp. 9–12, Feb. 2019.

[10] P. Jinho and D. J. Allstot, "A matrix amplifier in 0.18 μm SOI CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 561–568, Mar. 2006.

[11] K. Entesari, A. R. Tavakoli, and A. Helmy, "CMOS distributed amplifiers with extended flat bandwidth and improved input matching using gate line with coupled inductors," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 2862–2871, Dec. 2009.

[12] N. L. K. Nguyen et al., "A wideband SiGe power amplifier using modified triple stacked-HBT cell," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 1, pp. 52–55, Jan. 2021.

[13] N. L. K. Nguyen, D. P. Nguyen, A. N. Stameroff, and A. Pham, "A 1–160-GHz InP distributed amplifier using 3-D interdigital capacitors," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 5, pp. 492–495, Mar. 2020.

[14] D. P. Nguyen, N. L. K. Nguyen, A. N. Stameroff, V. Camarchia, M. Pirola, and A.-V. Pham, "A wideband highly linear distributed amplifier using intermodulation cancellation technique for stacked-HBT cell," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2984–2997, Jul. 2020.

[15] D. P. Nguyen, N. L. K. Nguyen, A. N. Stameroff, and A.-V. Pham, "A highly linear InP distributed amplifier using ultra-wideband intermodulation feedforward linearization," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1356–1359.

[16] N. L. K. Nguyen, D. P. Nguyen, A. Stameroff, and A.-V. Pham, "A high output power 1–150 GHz distributed power amplifier in InP HBT technology," in *Proc. IEEE Asia–Pacific Microw. Conf. (APMC)*, Dec. 2020, pp. 95–97.

[17] P. T. Nguyen, N. L. K. Nguyen, A. N. Stameroff, and A.-V. Pham, "A DC-170 GHz InP distributed amplifier using transmission line loss compensation technique," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 841–844.

[18] P. T. Nguyen, N. L. K. Nguyen, A. N. Stameroff, and A.-V. Pham, "A review of millimeter-wave InP distributed amplifiers," in *Proc. IEEE 22nd Annu. Wireless Microw. Technol. Conf. (WAMICON)*, Apr. 2022, pp. 1–4.

[19] N. L. K. Nguyen, N. S. Killeen, D. P. Nguyen, A. N. Stameroff, and A.-V. Pham, "A wideband gain-enhancement technique for distributed amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3697–3708, Sep. 2020.

[20] S. Yoon, I. Lee, M. Urteaga, M. Kim, and S. Jeon, "A fully-integrated 40–222 GHz InP HBT distributed amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 460–462, Jul. 2014.

[21] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "71–95 GHz (23–40% PAE) and 96–120 GHz (19–22% PAE) high efficiency 100–130 mW power amplifiers in InP HBT," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[22] V. Radisic, C. Monier, K. K. Loi, and A. Gutierrez-Aitken, "W-band InP HBT power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 9, pp. 824–826, Sep. 2017.

[23] T. Shivan et al., "A 175 GHz bandwidth high linearity distributed amplifier in 500 nm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1253–1256.

[24] F. Thome and A. Leuther, "First demonstration of distributed amplifier MMICs with more than 300-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2647–2655, Sep. 2021.

[25] K. Fang, C. S. Levy, and J. F. Buckwalter, "Supply-scaling for efficiency enhancement in distributed power amplifiers," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 1994–2005, Sep. 2016.

[26] H. Rashtian and O. Momeni, "Gain boosting in distributed amplifiers for close-to-FMAX operation in silicon," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 3, pp. 1039–1049, Mar. 2019.

[27] O. El-Aassar and G. M. Rebeiz, "A cascaded multi-drive stacked-SOI distributed power amplifier with 23.5 dBm peak output power and over 4.5-THz GBW," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3111–3119, Jul. 2020.

[28] C. Zech et al., "An ultra-broadband low-noise traveling-wave amplifier based on 50nm InGaAs mHEMT technology," in *Proc. German Microw. Conf. (GeMiC)*, Mar. 2012, pp. 1–4.