A 142-GHz 4/5 Dual-Modulus Prescaler for Wideband and Low Noise Frequency Synthesizers in 130-nm SiGe:C BiCMOS

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***Abstract*— In this contribution, the simulation and measurement results of a 4/5 dual-modulus prescaler, operating from dc to 142 GHz with a power consumption of 144 mW, are presented. For a division ratio of 4, the maximum operation frequency of 166 GHz is even higher. The prescaler is the core of a fully programmable dual-modulus frequency divider, which is a crucial component of modern measurement systems. The effect of the physical lengths and the resulting internal delays on the prescaler's performance is analyzed. Furthermore, the voltage level of the fully differential emitter-coupled logic (ECL) is optimized in terms of phase noise and maximum operating frequency. The monolithic microwave integrated circuit (MMIC) is realized in a 130-nm SiGe:C BiCMOS technology with f_T/f_{max} = 470/650 GHz.**

***Index Terms*— Dual-modulus divider, emitter-coupled logic (ECL), frequency divider, mmWave radar, phase-locked loop (PLL), SiGe heterojunction bipolar transistor (HBT).**

I. Introduction

MICROWAVE and THz measurement systems cover well-known applications like radar [1] and device characterization [2] as well as emerging applications like biomedical sensing [3] and plasma diagnostics [4]. Fully programmable frequency dividers are a key component in the high-end frequency synthesizers of such systems. These frequency synthesizers are typically realized as a fractional phase-locked loop (PLL) [5], [6]. To achieve a high system performance, the essential frequency divider must meet several requirements.

To modulate the output frequency of a frequency synthesizer, the division ratio of the frequency divider must be modulated [1]. Thus, the division ratio needs to be fully programmable and synchronously loaded into the divider. A high modulation frequency of the division ratio, which is commonly equal to the output frequency of the divider, is essential for the PLL's noise performance and control speed [1], [7]. If the programmable frequency divider operates at high input frequencies so that it can directly handle the output frequency of the PLL's oscillator, an additional static divider, which is commonly used, can be omitted. This reduces the complexity of the system and is beneficial for delta-sigma modulation. The swing of the output frequency due to the delta-sigma modulation decreases, which again lowers the requirements for the phase frequency detector (PFD) [8]. Furthermore, due to the high output frequency of the divider, the PLL's in-loop division ratio can be decreased, which reduces the PLL's phase noise. A wide division factor range is also important for the delta-sigma modulation and the synthesizer's performance. With a higher resolution of the frequency-modulated measurement signal, the measurement system benefits in terms of linearity and accuracy. The phase noise of the frequency synthesizer is affected by the additive phase noise of the frequency divider. Therefore, it should be particularly low.

These requirements can be achieved by a dual-modulus divider [9]. It is realized by the combination of one dual-modulus prescaler with two fully programmable counters. The dual-modulus prescaler is the component that limits the input frequency because the two frequency counters operate only at the prescaler's output frequency. A low additive phase noise can be achieved by a synchronization data flip-flop (DFF) at the output of the frequency divider [10]. As prescalers are the limiting key components for dual-modulus dividers, a serious effort is put into their development.

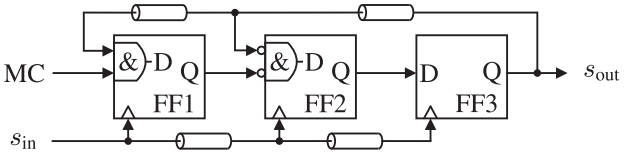

Fig. 1. Schematic of a 4/5 dual-modulus prescaler consisting of three synchronous FFs operating at the input frequency f_{in} of the signal s_{in}. The MC selects the division factor to be 4 or 5.

II. Architecture and Circuit Design

A. Principle

A 4/5 dual-modulus prescaler is realized by three DFFs, as shown in Fig. 1. The FF1 and FF2 have an additional AND gate at the data input. As the output of FF3 is fed back to the input of FF1 and FF2, the FFs operate as a frequency

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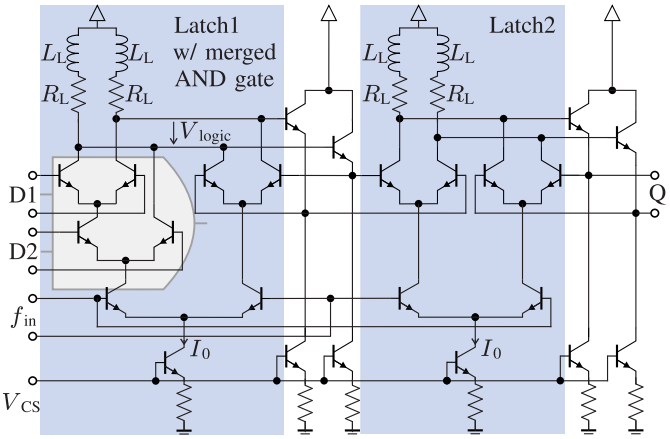

Fig. 2. Schematic of a fully differential DFF with merged AND gate in ECL with inductive shunt peaking.

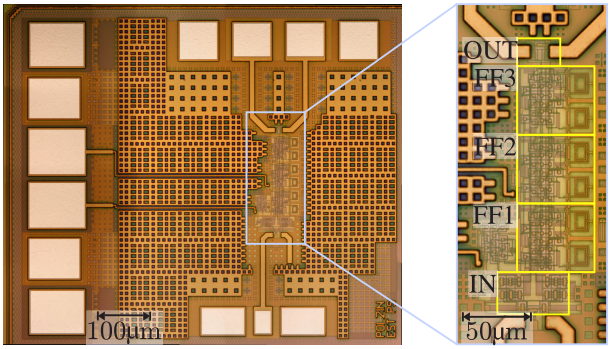

Fig. 3. Micrograph of the dual-modulus prescaler (left) and core circuit magnification (right) with input (IN), output buffer (OUT), and three FFs.

divider. All three FFs divide the input frequency by $N = 5$ if the modulus control (MC) is high. Whereas, FF2 and FF3 divide the input frequency by $N = 4$, while FF1 is deactivated, if MC is low. The effect of delaying the feedback as well as the input signal between the DFFs due to the circuit's physical size increases with the operation frequency. Thus, the transmission lines in Fig. 1 account for this delay.

B. Circuit Design

In order to achieve the highest operating frequencies, fully differential emitter-coupled logic (ECL) is used [9], [11]. To reduce the accumulated gate delay, the AND gates are merged into the first latch of FF1 and FF2, as shown in Fig. 2. The corresponding stacking of differential amplifiers reduces the collector–emitter voltage. However, we ensured that collector–emitter voltage is well above 0.4 V in any case, to maintain a high transistor speed. An additional method to enhance the operation bandwidth is inductive shunt peaking [12]. It utilizes an additional inductance L_L in series with the load resistor R_L, as depicted in Fig. 2. This improves the frequency response of the effective load impedance, i.e., including the transistors' input and output impedances as well as parasitics, so it remains longer constant toward higher frequencies. The self-resonance of the inductance has to be at a frequency reasonably higher than the desired operation frequency of the prescaler. Since the circuit is fully differential, a spiral inductor with a center tap is used. The main advantage is the small area occupied by this inductor. Contrary to a realization by transmission lines [13], the inductance cannot be adjusted after fabrication and the quality factor is lower. The latter can be compensated for by decreasing the value of the load resistor R_L, to keep the voltage swing of the logic gates constant.

C. Technology

The dual-modulus prescaler is implemented in IHP's 130 nm SiGe:C BiCMOS technology SG13G3 [14]. It features heterojunction bipolar transistors (HBTs) with a maximum transit frequency $f_T = 470$ GHz and a maximum oscillation frequency $f_{max} = 650$ GHz. The emitter size is $0.11 \times 1\,\mu m^2$ and can be scaled by parallelizing multiple emitters. For the applied collector–emitter voltages between 0.4 and 0.8 V the highest transit frequency is achieved at a collector current density $j_c \approx 22.7\,mA/\mu m^2$. Simulations are conducted using the Vertical Bipolar Intercompany (VBIC) model of the HBT.

D. Realization

The dual-modulus prescaler was designed with single emitter HBTs and the optimum collector current density of $j_c = 22.7\,mA/\mu m^2$ to achieve a high operation frequency with moderate power consumption. This leads to a collector current of $I_c \approx I_0 = 2.5$ mA in the latches and a power consumption of 144 mW drawn from a 3.3 V supply. It was demonstrated in [13] and [15], that an even higher current density can be advantageous to reach the maximum operation frequency of frequency dividers. Thus, the node V_{CS} in Fig. 2 is connected to an accessible current mirror, so that current through the logic gates and the emitter followers of the fabricated monolithic microwave integrated circuit (MMIC) can be externally adjusted. However, in that case, the prescaler's bias points are not optimal anymore. The logic voltage swing of the DFFs is 200 mV. A micrograph of the MMIC is shown in Fig. 3. In the magnified section the DFFs are highlighted and the six inductors can be identified. The input and output buffers draw 41 and 7.5 mA, respectively.

III. Simulations

The voltage swing of the logic gates $\hat{V}_{logic} = Z_L \cdot I_0$ affects the speed as well as the noise of the prescaler. Therefore, the maximum input frequency and the additive phase noise are simulated with different voltage swings and depicted in Fig. 4. For the simulations, the current density is constant and the load resistor is correspondingly modified. Inductive peaking is not simulated, as it must be optimized and simulated for each voltage swing individually, which would diminish the general validity. The maximum input frequency can be achieved with a voltage swing of $\hat{V}_{logic} = 140$ mV, but for voltage swings $\hat{V}_{logic} < 110$ mV, the prescaler does not operate properly. Thus, a slightly higher swing is preferable. As the additive phase noise also depends on the input frequency, its envelope is depicted for input frequencies from 20 to 100 GHz. While Fig. 4 shows the additive phase noise floor at an offset frequency of 1 MHz, the flicker noise corner is around 10 kHz. As a good tradeoff between the lowest phase noise and the maximum input frequency, the voltage swing was chosen to 200 mV. This also offers a low susceptibility to manufacturing tolerances. The inductive

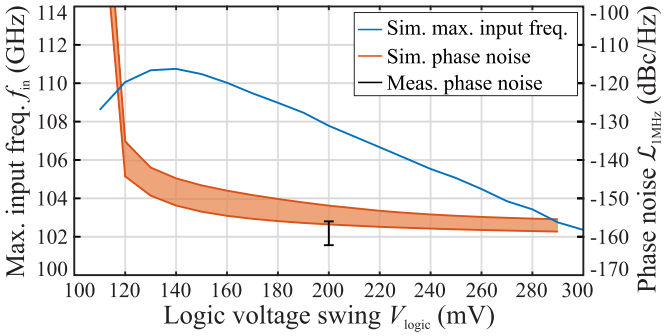

Fig. 4. Simulated maximum input frequency and additive phase noise as a function of the logic voltage swing as well as the measured additive phase noise for $V_{logic} = 200\,\text{mV}$.

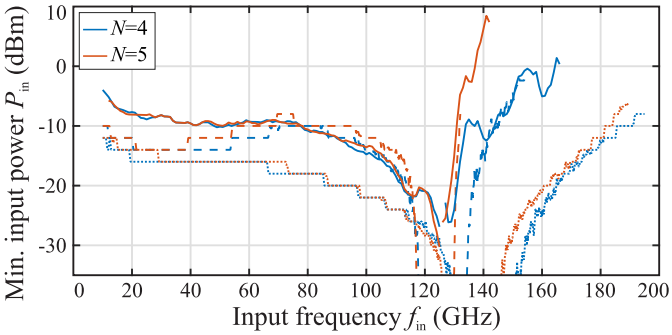

Fig. 5. Simulation with (dashed) and without (dotted) transmission delay as well as measurement (solid) of the prescaler's sensitivity.

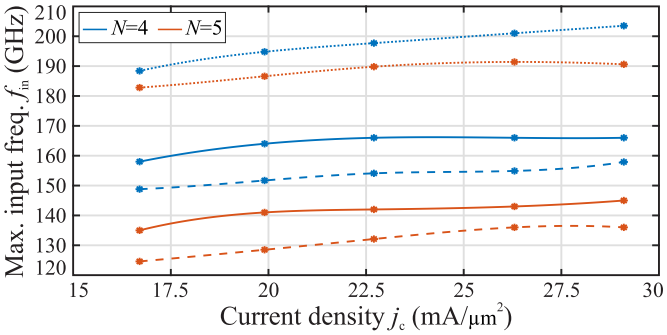

Fig. 6. Simulation with (dashed) and without (dotted) transmission delay as well as measurement (solid) of the prescaler's maximum input frequency as a function of the transistors' current density.

peaking is optimized to keep the voltage swing and group delay constant toward higher frequencies. Up to 150 GHz the resulting spiral inductor exhibits a inductance between 100 and 118 pH and a parasitic series resistance between 11 and 20 Ω, while the self-resonance is at 325 GHz. Frequency dividers are typically characterized by the minimum required power of a sinusoidal input signal as a function of the frequency. Typically, this sensitivity shows a minimum at the self-resonance of the frequency divider due to its feedback structure. For the high desired frequencies, not only the gate delay and transit frequency but also the physical length of the circuit becomes crucial. Therefore, simulations with ideal connections and simulated transmission lines between the DFFs are compared. The 2.5-D electromagnetic (EM) simulations are performed with Sonnet. In Fig. 5, the simulated sensitivity curves for the divider ratios $N = 4$ and $N = 5$ at the design current densities of $j_c = 22.7\,\text{mA}/\mu\text{m}^2$ are shown. Without simulated transmission delay, the prescaler operates up to 190 GHz and the sensitivity for both N differs only slightly. Whereas, with simulated transmission delay, the maximum input frequency decreases to 154 and 132 GHz for $N = 4$ and $N = 5$, respectively. The difference between the two division ratios is much higher due to the additional connection to FF3. To compare the effect of the current density j_c, the maximum input frequency as a function of j_c is depicted in Fig. 6. The maximum frequency slightly increases toward higher current densities. The effect of the delay lines becomes clear, too.

IV. Measurements

A. Measurement Setup

For measuring the sensitivity of the dual-modulus prescaler, two different measurement setups were used to cover the frequency range from 10 to 170 GHz. The input signal from 10 to 125 GHz is synthesized by a Keysight N5291 Network Analyzer System with an extended frequency range. The power spectrum of the output signal was measured with an R&S FSWP in spectrum analyzer mode and the MMIC was contacted with a Cascade Infinity Probe. The range from 110 to 170 GHz was covered by the PNA-X in combination with a vector network analyzer (VNA) millimeter wave converter Virginia Diodes (VDI) WR6.5-VNAX, which was connected to the chip by a Cascade Infinity Waveguide Probe.

B. Measurement Results

The measured sensitivity curves for the dual-modulus prescaler are depicted in Fig. 5. Both the measured frequency range up to 125 GHz and the measurements with the VDI WR6.5-VNAX fit well together. For $N = 4$ and $N = 5$, the prescaler operates up to a maximum input frequency of 166 and 142 GHz, respectively. This is 10 GHz higher than the simulations due to the fact that the measured prescaler operates properly with higher input power. Despite this, the simulated and measured sensitivity curves are in good agreement. The self-resonance is nearly the same.

The measurements were also performed with different current densities j_c from 16.7 to 29.1 mA/μm^2. To make the effect of j_c more evident, the maximum input frequency as a function of j_c is depicted in Fig. 6. Up to the design current density $j_c \leq 22.7\,\text{mA}/\mu\text{m}^2$, the measured maximum input frequency increases with the current density. For $j_c > 22.7\,\text{mA}/\mu\text{m}^2$, the measured maximum input frequency barely increases, proving the design current density as optimum. However, the simulated maximum input frequency continuously increases over the entire current density range. This is due to the limited modeling of high current effects in the VBIC model of the HBTs used in the simulations. Nevertheless, simulations and measurements are in good agreement.

The additive phase noise in Fig. 4 was measured using the R&S FSWP for $V_{logic} = 0.2\,\text{V}$ and $6\,\text{GHz} \leq f_{in} \leq 28\,\text{GHz}$. The measured flicker noise corner is in the range of

TABLE I
COMPARISON OF STATE-OF-THE-ART PRESCALERS

Ref	Technology	N	$f_{\text{in,max}}$ (GHz)	BW (GHz)	$P_{\text{con.}}$ (mW)	Technique
This work	130 nm SiGe	4/5	142	142	144	ECL i.p.
[13]	90 nm SiGe	4/5	117	117	92	ECL i.p.
[15]	130 nm SiGe	4/5	94	94	91	ECL i.p.
[16]	90 nm CMOS	4/5	44	44	45	CML i.p.
[17]	130 nm SiGe	2/3	117	117	94	ECL i.p.
			128	48	94	ECL i.p.
[18]	130 nm SiGe	2/3	70	70	66	ECL i.p.
[11]	140 nm SiGe	4	133	133	210	ECL
			105	105	51	ECL
			87	87	14	CML
[19]	90 nm SiGe	2	242	122	155	dyn. div.
[20]	130 nm SiGe	2	92	90	55	CML
			89	75	25	CML

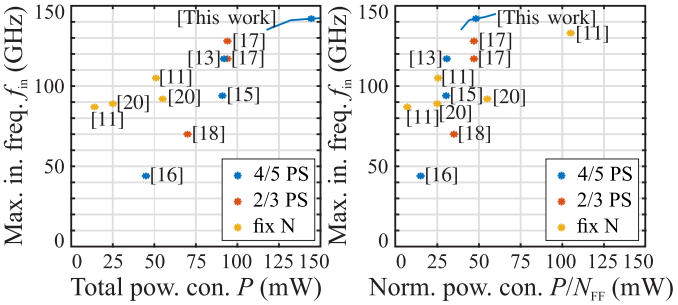

Fig. 7. Maximum input frequency in relation to the total (left) and normalized to one FF (right) power consumption P for state-of-the-art prescalers.

10–40 kHz. Integrating offset frequencies from 100 Hz to 1 MHz results in a jitter between 0.5 and 1.9 fs.

C. State of the Art

A comparison of state-of-the-art high-speed prescalers is given in Table I. Fig. 7 illustrates their maximum input frequency in relation to their power consumption. Typically, 2/3 prescalers and 4/5 prescalers are realized with two and three FFs, respectively. Thus, this work achieves the highest reported input frequency for dual-modulus prescalers while maintaining a good normalized power consumption.

V. CONCLUSION

We presented a 4/5 prescaler operating at input frequencies up to 142 GHz for a division ratio of $N = 5$. For $N = 4$ the maximum input frequency of 166 GHz is even higher. The prescaler is a crucial component for a fully programmable, high-speed frequency divider, required in the PLLs of high-end measurement systems. To achieve maximum operation speed and low additive phase noise, the logic voltage swing was optimized to 200 mV. It was shown that the current density for the highest f_T is optimum. By comparing simulations with and without transmission lines, their negative impact on the maximum operation frequency is exposed. Although the layout is already compact, efforts on optimizing the MMIC's layout can still push the frequency upward.

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