

A 5–10-GHz Highly Configurable IEEE 802.15.4a/4z-Compatible IR-UWB Coherent Transmitter in 28-nm CMOS

Li Zhang¹, Member, IEEE, Nguyen L. K. Nguyen¹, Member, IEEE, Jingjun Chen¹, Member, IEEE, Xiaoguang Liu², Senior Member, IEEE, and Omeed Momeni³, Senior Member, IEEE

Abstract—This letter presents an IEEE 802.15.4a/4z-compliant integrated impulse radio ultrawideband (IR-UWB) coherent transmitter that supports all channels in Band 2 from 6.5 to 10 GHz. A wideband phase-locked loop (PLL) with dual LC quadrature voltage-controlled oscillators (QVCOs) is implemented that covers more than 5-GHz frequency range. The PLL features a phase noise of -99.8 dBc/Hz at 1-MHz frequency offset and an rms jitter of 2.3 ps, which ensures reliable coherent operation. The quadrature clocks also make easy future I/Q receiver integration. The pulse envelope and width are digitally controlled, thanks to our flexible digital pulse-shaping configuration. Implemented in a 28-nm CMOS process with a supply voltage of 0.9 V, the chip occupies a core area of 0.21 mm² and supports channel 5–15 with a peak pulse repetition frequency (PRF) of 499.2 MHz. The transmitter has a maximum output swing of 430 mV and the power consumption is 1.3 nJ/pulse at a PRF of 15.6 MHz.

Index Terms—CMOS, digital power amplifier (DPA), IEEE 802.15.4, impulse radio (IR), phase-locked loop (PLL), transmitter, ultrawideband (UWB).

I. INTRODUCTION

WITH an increasing demand for accurate indoor and outdoor ranging and location, ultrawideband (UWB) technology draws much attention in the field of smartphones, intelligent vehicles, health monitoring, and the Internet of Things (IoT) due to its capability in providing centimeter-level location accuracy under impulse-radio (IR) operation. In comparison to the legacy standard IEEE 802.15.4a, the newly released IEEE 802.15.4z standard improves upon the security of ranging and mandates a coherent operation mode for high-rate PHY [1]. Although free-running digitally controlled oscillators (DCOs) are preferred due to their low power consumption and short startup time, the poor clock

Manuscript received 12 November 2022; accepted 28 November 2022. Date of publication 2 January 2023; date of current version 10 May 2023. (Corresponding authors: Xiaoguang Liu; Omeed Momeni.)

Li Zhang, Nguyen L. K. Nguyen, and Omeed Momeni were with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA (e-mail: zjuzhang@ucdavis.edu; nlknguyen@ucdavis.edu; omomeni@ucdavis.edu).

Jingjun Chen was with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA. He is now with Qualcomm Atheros, Inc., Santa Clara, CA 95051 USA (e-mail: meechen@ucdavis.edu).

Xiaoguang Liu was with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA. He is now with the School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China (e-mail: liuxg@sustech.edu.cn).

Color versions of one or more figures in this letter are available at <https://doi.org/10.1109/LMWT.2022.3228237>.

Digital Object Identifier 10.1109/LMWT.2022.3228237

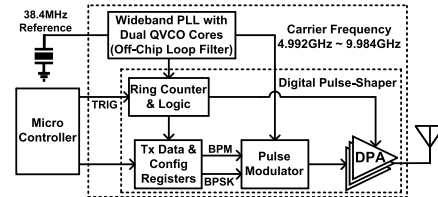


Fig. 1. Proposed IR-UWB Tx architecture.

quality cannot meet the stringent frequency accuracy and jitter requirements for coherent operation, even with the help of frequency tuning or calibration [2], [3], [4]. Therefore, in this work, as prior standard coherent systems do [5], [6], [7], a continuously running phase-locked loop (PLL) for clock generation is adopted that covers a wide frequency range from below 5 GHz to beyond 10 GHz.

Different approaches have been explored to generate the UWB pulse that meets the spectral emission regulations as prescribed by Federal Communications Commission (FCC). Conventional IR-UWB transmitters use a digital synthesizer and a low-pass filter (LPF) [7] or direct baseband pulse-shaping filters [8], [9], whose output is up-converted to RF with a mixer and amplified using a linear driver amplifier. However, high power dissipation, limited frequency range, as well as big die area in such transmitters are undesirable. As a result, digital pulse-shaping utilizing a low-supply CMOS process has become a dominant strategy because of its low power consumption and high programmability [2], [10], [11].

In this work, we present a more flexible digital pulse-shaping method using a highly configurable ring counter and a parallel digital power amplifier (DPA) stages. The major contributions of our work include the following.

- 1) The design achieves the highest degree of pulse-shaping configurations reported in the literature.
- 2) A low-jitter PLL is implemented using dual LC quadrature voltage-controlled oscillators (QVCOs) for reliable coherent operation.
- 3) Integrated quadrature clocks improve the receiver signal-to-noise ratio (SNR).

II. IR-UWB TRANSMITTER ARCHITECTURE

The architecture of the proposed IR-UWB transmitter is shown in Fig. 1. Transmitter data and configuration bits are stored in on-chip registers before pulse generation through a microcontroller. The PLL is locked to an external 38.4 MHz reference and generates target carrier frequencies from 4.992 to 9.984 GHz, which are then used to drive the ring counter and pulse modulator. The output of the last stage within the ring counter serves as the clock to synchronize

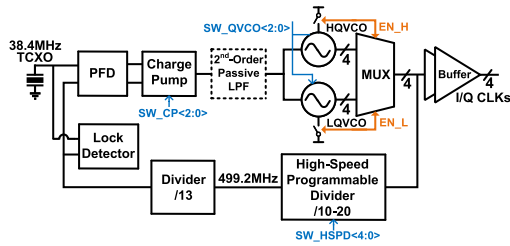


Fig. 2. Dual LC-QVCO-based PLL architecture.

the burst position modulation (BPM) and binary phase shift key (BPSK) transmitter data bits. Outputs of the ring counter and logic block are used to drive corresponding DPA cells. Parallel DPA cells are combined to transmit FCC-compliant pulses through commercial wideband antenna without the need for bulky off-chip filtering.

A. Wideband PLL With Dual LC QVCO Cores

Fig. 2 shows the wideband integer-N-type-II PLL architecture in this work. The PLL uses two LC QVCOs to provide continuous frequency coverage of Band 2 with a sufficient margin and overlap to accommodate the process, voltage, and temperature (PVT) variations and modeling inaccuracies. The use of QVCOs allows easy generation of quadrature clocks that are essential in improving the receiver's SNR [6], [7], [8]. A 3-bit current-controlled charge pump is implemented to tune the PLL bandwidth. The second-order loop filter is implemented off-chip to save chip area. A transmission gate-based multiplexer selects between the two QVCOs for different carrier frequencies. On the feedback path, a high-speed programmable divider is used to bring the carrier frequency down to a fixed frequency of 499.2 MHz. The divider incorporates the control logic into a conventional cascade prescaler and achieves an extended division ratio of 8–31 with four prescalers [12], [13]. The 499.2-MHz clock can be used as the chip rate clock, or fed to a frequency doubler to generate the 998.4-MHz clock for the receiver back-end [7]. The output of the divide-by-13 block and buffered 38.4-MHz temperature-compensated crystal oscillator output are compared by the phase frequency detector. An analog lock detector [14] with a 10-bit counter depth is implemented as an indicator for PLL operation status.

The quadrature clocks are generated by direct current coupling between two LC VCOs. Such structure suffers from inherent frequency uncertainty because it can support two oscillation modes as explained in [15], [16], and [17]. To avoid such uncertainty, RC phase shifters are used in this work in the coupling path as illustrated in Fig. 3 to ensure the loop gain of the desired mode is dominant. Therefore, one oscillation mode is boosted, while the other is suppressed. A combination of a capacitor bank-based coarse tuning and a varactor-based fine tuning is used for both QVCOs. Each capacitor bank consists of eight unit cells over 3-bit control. To further improve phase noise performance, high-quality factor (Q) MOM capacitors and parallel switches are used to increase the overall Q of the resonant tank. If desired, quadrature carrier frequencies in Band 1 (3.4944–4.4928 GHz) can also be obtained by dividing the corresponding frequencies by two within Band 2.

B. Digital Pulse Shaping Architecture

Fig. 4 explains the detailed operation principle of the digital pulse-shaping method. The fully symmetric ring counter is

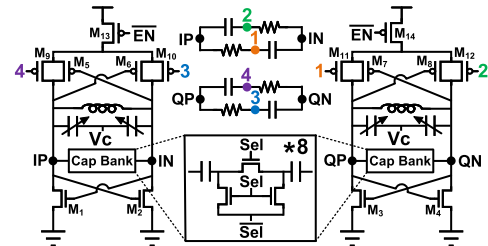


Fig. 3. Structure of QVCO with bimodal oscillation suppression technique.

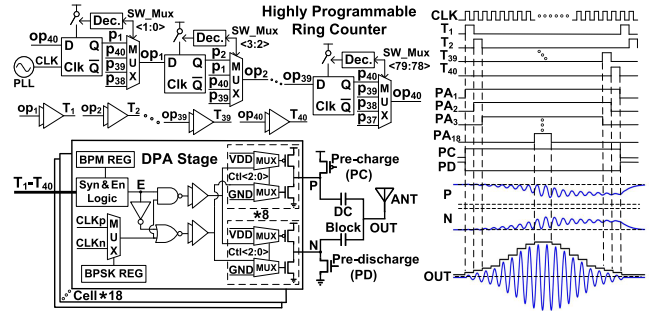


Fig. 4. Digital pulse shaping and waveform illustration.

clocked by the PLL output and consists of 40 true single-phase-clock (TSPC) digital flip-flop (DFF) and transmission-gate-based 4:1 multiplexer unit cells. Due to its high programmability, the ring counter is able to bypass up to 30 unit cells for different pulsewidth and signal bandwidth. Bypassed DFFs are disabled to save power. As a result, if all unit cells are enabled, a maximum of 40 consecutive rectangular pulse windows as long as the clock period is created from T_1 to T_{40} as shown in Fig. 4. The pulse envelope shaping function is implemented by 18 parallel DPA stages. Within each DPA stage, a logic AND operation is first performed between all T_n 's and corresponding envelope configuration bits to determine whether this DPA stage should be ON or OFF during each T_n . If BPM data is logic "1," an enable signal at node E is generated by performing OR function on all ON T_n 's. The BPSK data selects either CLK_p or CLK_n to modulate the pulse. Before propagating to the dual-path tri-state inverter output cells, the CLK is controlled by the enable signal at node E, which turns the inverters ON or OFF.

Between pulses, nodes P and N are precharged and pre-discharged to VDD and GND, respectively. Output current from two paths that have in-phase RF components, but out-of-phase low-frequency components are then capacitively combined at the antenna using on-chip DC block capacitors as illustrated in Fig. 4. This ensures that the DC component of the combined DPA output remains close to half-VDD independent of the modulation and helps reduce spectral content in the 960–1610-MHz frequency corner [2]. Also, the DC block capacitors and antenna serve as a high-pass filter that further reduces emission at low frequencies. Both up and down paths in each DPA stage consist of eight tri-state inverter unit cells configurable with 3 bits of output power control to meet the power spectrum density (PSD) requirement of -41.3 dBm/MHz [1] for different mean pulse repetition frequencies (mPRFs).

The proposed digital pulse shaping architecture achieves a significantly high degree of flexibility in programming the pulse envelope and width. The proposed structure is able to modulate BPM and BPSK bits with a Gaussian or other desired

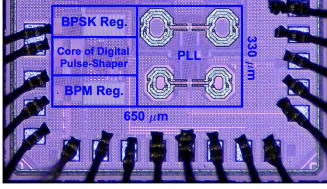


Fig. 5. Die micrograph of the proposed transmitter.

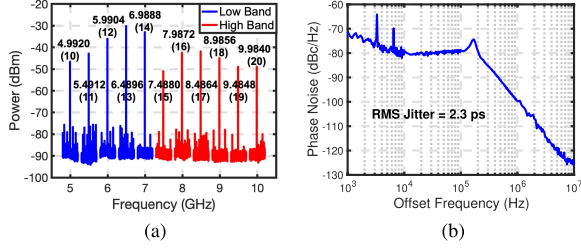


Fig. 6. Measured (a) spectrum of PLL carrier frequencies and (b) PLL phase noise and rms jitter at 6.4896 GHz.

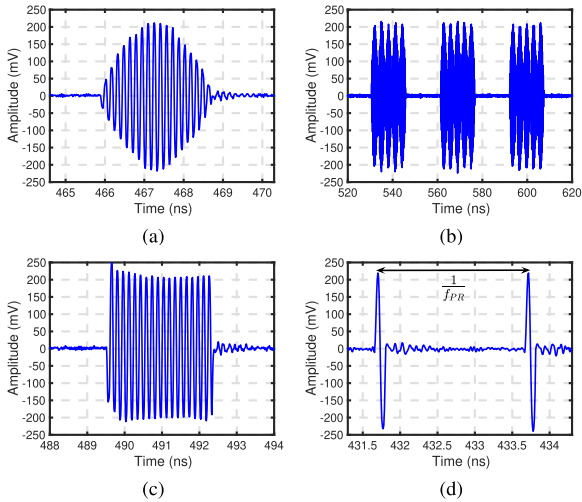


Fig. 7. Measured time-domain waveform of (a) Gaussian envelope pulse for channel 5, (b) burst of pulses for channel 5, (c) square envelope pulse, and (d) monocycle pulse with a maximum PRF of 499.2 MHz.

enveloped pulse with programmable pulsewidth from 0 to 4 ns at 9.984-GHz carrier frequency, and 0 to 8 ns at 4.992 GHz. A 4-ns pulsewidth is sufficient to meet the minimum 499.2-MHz signal bandwidth requirement.

III. MEASUREMENT RESULTS

The proposed IR-UWB transmitter is fabricated in a 28-nm CMOS process. Fig. 5 shows the die micrograph of the chip after wire-bonding. Anritsu MS2830A signal analyzer and Tektronix MSO72004C oscilloscope are used for frequency-domain and time-domain measurements.

The PLL is able to provide wide carrier frequencies with continuous integer multiples of 499.2 MHz from 10 to 20 as shown in Fig. 6(a). In the post-layout simulation, the corresponding I/Q mismatch of these carrier frequencies is within 1° . The measured phase noise is -99.8 dBc/Hz at 1-MHz frequency offset and the rms jitter is 2.3 ps with a carrier frequency of 6.4896 GHz for channel 5 and channel 7 as shown in Fig. 6(b).

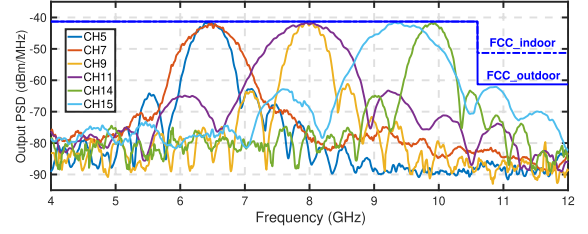


Fig. 8. Measured PSD of the proposed transmitter in Band 2.

TABLE I
COMPARISON WITH COHERENT IR-UWB TRANSMITTERS

Reference	This work	[10]	[5]	[6]
Technology	28nm CMOS	28nm CMOS	22nm FinFET	40nm CMOS
Supply(V)	0.9	0.9	0.7	1.25
Supported channels	5–15	1–15	5,6,8,9	5–15
Monocycle pulse generation	Yes	No	No	No
Mod. BW(GHz)	0.5/1/1.33[‡]	0.5/1	0.5	0.5/1.35
Date rate(Mb/s)	0.11–27.24	6.81	0.11	0.11–31.2
Quadrature LO	Yes	No	No	Yes
LO RMS jitter(ps)	2.3	0.34*	9 [†]	3.48 [§]
Ref. freq.(MHz)	38.4	499.2	38.4	38.4
Active Power(mW)	20.3	4.9**	0.3	61.6
Energy(pJ/pulse)	1300	39.5	170	3949 ^{§§}
@ PRF(MHz)	15.6	124.8	15.6	15.6
Die area(mm ²)	0.21	0.15	0.09	0.77 ^{§§§}

[‡] Several GHz for pulse radar application

* 499.2-MHz external PLL

** Not including external PLL

[†] Simulated without reference noise

[§] Declared as pulse jitter

^{§§} Calculated from active power consumption

^{§§§} Including Tx, CLKPLL, and RFPLL estimated from die micrograph

Fig. 7(a) shows the transmitted Gaussian envelope pulse waveform for channel 5 with a maximum peak-to-peak amplitude of 430 mV, including 2-dB loss from the wirebonds, PCB traces, SMA connectors, and cables. Fig. 7(b) shows a pulse burst transmission. The highly configurable transmitter is also capable of generating a rectangular envelope pulse as shown in Fig. 7(c), while Fig. 7(d) shows a monocycle pulse with a peak pulse repetition frequency (PRF) of 499.2 MHz, which can be used for UWB pulse radar applications due to its short pulse duration and high resolution [18], [19].

The transmitter supports all channels in Band 2. The measured PSD shows the compliance with the FCC mask for all supported channels as illustrated in Fig. 8. The performance of this work is summarized and compared with state-of-the-art coherent IR-UWB transmitters in Table I. Our work features the highest degree of pulse-shaping configurations and is the only one capable of generating UWB monocycle pulses. Besides, only our work and [6] have implemented the quadrature clocks. However, the rms jitter and power consumption in [6] are significantly higher than our work.

IV. CONCLUSION

This letter presents an IEEE 802.15.4a/4z-compatible fully integrated IR-UWB coherent transmitter in 28-nm CMOS that supports all channels in Band 2. In addition, the transmitter can be used for UWB pulse radar applications. The wideband PLL based on dual LC QVCO cores provides high-quality I/Q clocks for coherent modulation and future I/Q receiver integration. Pulse envelope, width, and amplitude are all highly configurable to meet FCC regulations under different channels and data rates without off-chip filtering.

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