Device engineering guidelines for performance boost in IGZO front gated TFTs based on defect control

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Amorphous InGaZnO thin film transistors (a-IGZO TFTs) have been investigated for their applications in display panels and sensors. These IGZO TFTs are BEOL compatible and can be stacked for 3D integration making them attractive for logic and memory including neuromorphic computing applications [1-3]. For different target applications, the device performance can be varied by appropriate stack engineering. Defects in the IGZO layer strongly impact the device performance and operating regimes. Therefore, defect control is fundamental in tailoring the performance to meet the target specifications. Hydrogen and oxygen vacancies act as shallow donors in IGZO [4]. The presence of hydrogen in the processing steps contributes to the hydrogen doping. The contact metal scavenges oxygen from IGZO, resulting in oxygen vacancies. Thus, the doping in these devices is sensitive to the stack as well as the processing. In this work, we discuss different architectures, stack engineering, and device design guidelines for performance boost based on defect control.

Two different process integration flows are discussed – gate-first and gate-last. In the gate-last integration scheme (contact metal is deposited on entire active followed by trench etch giving self-aligned contacts and gate stack is deposited in the trench), there are fewer hydrogen critical steps making it preferable for higher threshold voltage (V_t) [5]. Also, the gate-last process provides the flexibility of integrating different contact barrier metals for oxygen scavenging control. Usually, the as-processed devices have large defect concentration leading to very negative V_t. One simple solution is post-processing anneal in oxygen ambient to passivate the oxygen vacancies. As a result, V_t increases while the maximum current reduces. Initially, on current (I_{on} @ V_{gt} = 1 V) increases due to SS improvement. With further anneals, SS saturates while R_{par} continues to increase. So, I_{on} tends to saturate (optimized I_{on}-V_t defined at this anneal) and then reduces with stronger anneals. Having a continuous SiO_2 layer under IGZO passivates defects in the channel region as well as under the contacts, increasing the R_{par} significantly. To overcome this limitation, targeted defect passivation in the channel is achieved using oxygen tunnel (OT) module, where SiN below the contacts acts as an oxygen blocking layer, while SiO_2 under the channel acts as an oxygen conduit [6]. This results in ~100× lower R_{par} in devices with OT for similar anneal compared to continuous buffer devices. Material deposition and the composition also strongly impact the defect density, thereby the electrical performance [7].

Improved electrostatic control and higher currents can be achieved by scaling the gate dielectric thickness, but it may have larger initial defect concentration and requiring stronger anneal for optimization. V_t increase is also observed on thinning down IGZO, and even positive V_t is obtained in devices with IGZO thickness less than 5 nm, thus eliminating the need for oxygen anneal. However, in this case, the V_t is also dependent on the OT or different continuous buffer layers due to the sensitivity of the active layer.

Furthermore, to reduce the R_{par}, we incorporate raised contacts [8]. In addition to providing the opportunity to decouple the contact interface from the channel material, the raised contacts move the sources of doping (hydrogen from the W fill in the interconnects, and oxygen scavenging by the contact metal) away from the channel [9]. Thus, initial defect concentration is lower and milder anneal is required. The contact interface is also farther from the oxygen tunnel allowing higher defect density in the contact regions.

Figure 1 shows the schematic of the stack integrated with gate-last integration flow with oxygen tunnel module and the raised contacts. Incorporating the above design guidelines, we demonstrate excellent performance in scaled front gated a-IGZO TFTs (Fig 2).

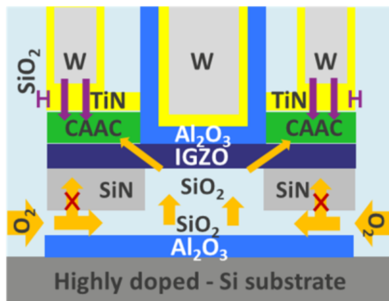

Fig. 1 Device schematic with gate-last process flow, oxygen tunnel module, and raised contacts.

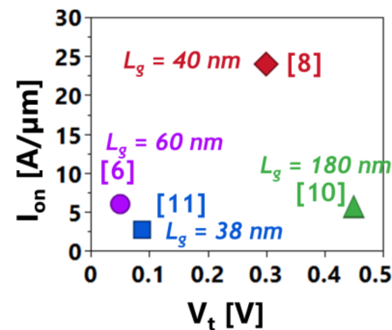

Fig. 2 Performance benchmarking of scaled front gated a-IGZO TFTs.

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