2022 International Conference on IC Design and Technology (ICICDT) | 978-1-6654-5901-3/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICICDT56182.2022.9933084

Invited Talk #4

SOI CMOS technologies for RF and millimeter-wave communication systems

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Radio Frequency (RF) performance of an integrated circuit (IC) does not only depend on the analog and high frequency characteristics of the active devices, i.e. the transistors, but also the quality of the back-end of line (BEOL) process which defines the losses along the interconnection lines and the quality factor of the passive elements such as the inductors and tunable capacitors, as well as the electromagnetic properties of the substrate on which the RF IC is lying.

The parasitic resistances (metal lines and vias) and capacitances (dielectric layers) along the interconnection constitute a low-pass filter which drastically limits the operational frequency of ICs [1]. Advanced BEOL process provides higher number of metal lines, thicker metal layers, low-k dielectric interlayers and denser vias using carbon nanotubes are investigated for diminishing the parasitic resistances between metal layers [2, 3]. The substrate losses, crosstalk and non-linearities remain the major challenges for designing high-performance RF ICs in Si-based technologies. The root cause of missing RF performance of high-resistivity (HR) Silicon-on-Insulator (SOI) substrate was found by demonstrating the existence of a parasitic surface conduction [4, 5] below the buried oxide (BOX) and the way to disable it by introducing traps. In 2005, the possibility of creating SOI substrates characterized with an effective resistivity [6] as high as 10 k□.cm thanks to the introduction of a thin undoped polysilicon layer below the BOX of a HR SOI substrate was demonstrated [7].

Today, Partially Depleted (PD) SOI transistors with a channel length of 90 or 130 nm combined with a HR trap-rich SOI substrate is the mainstream technology for RF ICs. New generation of mobile communication systems such as 5G and 6G require higher cut-off frequency for the system, better linearity and lower power consumption. Moreover, the integration of high-quality inductors requires higher number and thicker metal layers. To fulfil those requirements, RF SOI must move to shorter nodes. Fully Depleted (FD) electronic regime is a promising approach to continue the scaling down of MOSFETs while controlling the short channel effects (SCE). In order to limit SCE, the channel thickness must be approximately 1/4 and 2/3 of the channel length, respectively, in the case of ultra-thin body and buried oxide (UTBB) and FinFET. Technological aspects, electrostatics, scalability and variability issues in UTBB FD-SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [8, 9].

In this paper, the main interesting features of the FD SOI CMOS technology for RF and millimeter-wave applications are presented. Firstly, the low-power and high-frequency performance of FD SOI [10]-[12] featuring various types of back gate contacts are shown for operation at cryogenic [13] and high temperature [14]. The benefit of the back gate biasing to improve the RF noise characteristics [15] as well as the transistor linearity [16] is demonstrated. Secondly, the importance of moving from standard to high-resistivity Si substrate to reduce the crosstalk issues [17], interconnection RF losses and non-linearities [18] are presented. The non-linear model for the engineered trap-rich SOI substrate is detailed [19, 20], and finally a brief review of SOI ICs in RF and millimeter-wave domain is given [21-24].

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