A 1.6-GHz Sub-Nyquist-Sampled Wideband Beamformer on an RFSoC

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***Abstract*— This paper presents how to simultaneously achieve elemental sub-Nyquist sampling and true-time-delay (TTD) beamforming using a contemporary RF system-on-a-chip (RFSoC) by outlining the development of a 1.6 GHz S-band phased array system implemented using a Xilinx 8-channel 4 GSPS RFSoC. RFSoCs integrate a high speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC) with a Field Programmable Gate Array (FPGA) and system-on-a-chip (SoC) architecture on a singular device, enabling direct sampling of RF signals. Thus, the RFSoC is the only hardware in this beamformer apart from the antenna aperture. This enabling technology facilitates the development of compact all-digital arrays, which massively increases the available degrees of freedom in system control enabling a paradigm shift in industry and engineering communities. The efficacy of our modular approach is confirmed via our research testbed.**

***Index Terms*— Digital beamforming, wideband phased array, RF system-on-a-chip, beam squint, pulse dispersion, true time delay, chamber measurements.**

I. Introduction

THE RF system-on-a-chip (RFSoC) is a contemporary device which integrates multiple analog-to-digital converter (ADC) and digital-to-analog converter (DAC) channels into a Field Programmable Gate Array (FPGA) and System-on-a-Chip (SoC) Integrated Circuit (IC), providing potential footprint and power reductions of 50% and 75% [1], respectively. Researchers have been exploring the role of the RFSoC in next-generation phased array applications including bistatic radar [2], synthetic aperture radar [3], near-field calibration [4], real-time signal generation [5], and fully-digital radar systems [6]. Several examples of RFSoC-based phased array systems can be found in current literature [7], [8], [9], [10], [11], [12], demonstrating sample rates of $1-4$ GSPS in various system architectures. In [7], a minimum variance distortionless response (MVDR) beamformer is digitally implemented on an RFSoC with ADCs operating at 125 MHz. Its system architecture incorporates an RF downconverter with an 8 MHz passband. The authors in [8] demonstrate a multi-beam digital beamformer which employs direct sampling of 1 GHz, 100 MHz bandwidth quadratic-amplitude modulation (QAM) signals at a sample rate of 4 GSPS. A 16-element phased array with ADCs operating at 2 GSPS is shown in [9] which supports an 800 MHz bandwidth. However, at a carrier frequency of 28 GHz, narrowband beamforming was sufficient. Beamforming measurements summarized in [10] utilize the Integrated Multi-use Phased Array Common Tile (IMPACT) [11] which supports an instantaneous bandwidth (IBW) of about 500 MHz. Beamforming using a tightly coupled dipole array (TCDA) is demonstrated at 3.5 GHz, 4.9 GHz, and 9.5 GHz, without mention of test signal bandwidth. The authors in [12] provide narrowband measurements and discuss a wideband beamforming engine with equalization.

In this paper, we present an 8-element fully-digital sub-Nyquist-sampled wideband receive array utilizing an RFSoC. This system matches or exceeds key performance metrics of the aforementioned literature such as digital bandwidth, absolute bandwidth, sampling frequency, and fractional bandwidth. Demonstrated with a linear chirp signal, a commonly used radar waveform, with a 1.6 GHz bandwidth centered at 3 GHz, array elements are directly sampled by 4 GSPS ADCs such that the chirp waveform is centered in the second Nyquist zone and, upon sampling, folds into the first Nyquist zone. Signal compensation supporting the entire digital bandwidth is applied at complex baseband following the digital downconverter (DDC). Sub-Nyquist-sampled beamforming enables direct sampling below the Nyquist frequency while maintaining waveform bandwidth. This simplifies system design by mitigating the need for traditional analog downconversion circuitry while allowing for lower sample rates, and thus lower power consumption, than would be required to support Nyquist sampling at the carrier frequency. Sub-Nyquist sampling has been utilized in wideband spectrum sensing [13] and direction-of-arrival (DoA) estimation [14]. Additionally, researchers in the ultrasound community [15], [16] and optical tomography community [17] have leveraged the concept of sub-Nyquist sampling to reduce power and layout requirements.

This paper is organized as follows. Relevant theory is presented in Section II, including a comparison of narrowband and wideband beamforming, implications of sub-Nyquist-sampled beamforming, and the design of finite impulse response (FIR) fractional-sample delay filters for an embedded system. An overview of the wideband beamforming testbed is provided in Section III, including the hardware, firmware, and software. Section IV presents the results of bench-top and over-the-air (OTA) far-field anechoic chamber measurements. Comparisons between narrowband and wideband beamsteering measurements are presented as well as measured versus

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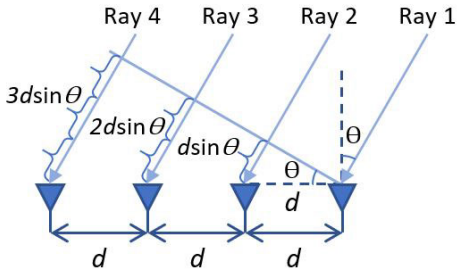

Fig. 1. Ray tracing geometry for 4-Element ULA.

simulated wideband beamsteering performance. A summary is provided in Section V.

II. Problem Formulation and Relevant Theory

This section provides the theoretical basis on which the demonstrated results are based. Section II-A provides an overview of phased array beamforming for both narrowband and wideband signals. Section II-B discusses digital true time delay (TTD) units and their application to wideband beamforming. A procedure for designing a digital fractional-sample delay filter bank is also provided. Lastly, Section II-C discusses compensation implications of sub-Nyquist-sampled beamsteering.

A. Beamforming

The fundamental intent in phased array beamforming, also known as *classical beamforming* [18], is to determine sensor signal compensation which causes signals to combine coherently for a given steering direction. Other beamsteering techniques may seek to broaden the beam to expand spatial coverage or to mitigate the effects of directional interferers through directional nulling or adaptive beamsteering by maximizing the signal to interference and noise ratio (SINR) [19]. However, the focus herein will be on the coherent summation of signals for a given direction. It is well known [20], [21], [22], that the time delay between elements in a uniform linear array (ULA) for a signal phase front to propagate from the first element to element n is given by

$$\Delta t_{\mathrm{n},\theta} = \frac{(n-1)d\sin\theta}{c} \ , \tag{1}$$

as shown in Figure 1. Classical beamforming seeks to compensate the inter-element time delay, either through TTD devices or by approximating the time delay via phase shifters. As phase shifters apply a frequency-invariant shift in phase, element compensation is defined by

$$\phi_n = 2\pi f_{\mathrm{c}} \Delta t_{\mathrm{n},\theta_{\mathrm{st}}} \ , \tag{2}$$

where f_{c} is the waveform's center frequency and $\Delta t_{\mathrm{n},\theta_{\mathrm{st}}}$ is the compensation time delay for element n in the direction θ_{st}. In contrast, TTD units apply a direct time delay, resulting in the frequency-variant phase shift described by $\phi_n(f) = 2\pi f \Delta t_{\mathrm{n},\theta_{\mathrm{st}}}$.

Bandwidth limitations due to the use of phase shifters, such as beam squint and pulse distortion are well documented [23], [24], [25]. Beam squint occurs when the ULA phase gradient is defined by Eq. (2), yielding progressively degrading beam accuracy with increasing $\Delta f = |f - f_{\mathrm{c}}|$. This phenomenon becomes more drastic with increasing steering angles. The frequency range over which the main beam response is within 3 dB of the peak response for the worst-case steering direction provides an estimate for system bandwidth [22]. Pulse dispersion arises when phase shifters are unable to provide more than one cycle of delay. Thus, when the propagation time across the aperture, known as the aperture fill time [26] t_{fill}, is greater than one cycle, compensation is wrapped to within 0° to 360° resulting in phase coherent signals lacking time alignment. The aperture fill time provides an additional estimate of system bandwidth [26] for a given steering angle, as described by $B = \frac{1}{t_{\mathrm{fill}}}$, although less conservative than the beam squint bandwidth constraint [24]. In order to increase the bandwidth of larger arrays, which have smaller beamwidths and large aperture fill times [21], TTD units may be incorporated at the sub-array level when elemental TTD units are impractical.

B. True Time Delay Units

The RFSoC facilitates elemental digital implementation of TTD units through a combination of integer and fractional-sample delays. While integer-sample delays are trivially implemented by shifting digital signal samples, fractional-sample delays require a digital filter. This section provides a design method for fractional-sample delay FIR filter synthesis as well as considerations for embedded system applications.

1) Ideal Fractional-Sample Delay Filter: The ideal fractional-sample delay filter has a frequency response with unity gain and linear phase [27], as prescribed by the time shift property of the Fourier transform. Thus, the ideal frequency response for a discrete FIR filter with delay t_{a}, is given by

$$H_{\mathrm{d}_{1/T_{\mathrm{s}}}}(f) = e^{-i2\pi f t_{\mathrm{a}}}, \ \ |f| \leq \frac{F_{\mathrm{s}}}{2} \ . \tag{3}$$

which is periodic over the interval F_{s}. The magnitude and phase responses are given by $|H_{\mathrm{d}_{1/T_{\mathrm{s}}}}(f)| = 1$ and $\angle H_{\mathrm{d}_{1/T_{\mathrm{s}}}}(f) = -2\pi f t_{\mathrm{a}}$, respectively, where different fractional-sample delays correspond to different phase slopes. The corresponding set of filter taps can be computed by taking the Discrete-Time Inverse Fourier transform of the desired periodic frequency response, as given by

$$\begin{aligned} h_{\mathrm{d}}[n] &= T_{\mathrm{s}} \int_{1/T_{\mathrm{s}}} e^{i2\pi f(nT_{\mathrm{s}} - t_{\mathrm{a}})} df \\ &= \mathrm{sinc}\left(\pi\left(n - \frac{t_{\mathrm{a}}}{T_{\mathrm{s}}}\right)\right) \ . \end{aligned} \tag{4}$$

As the resulting sinc response [28] is both infinite and non-causal, it is not possible to implement the ideal fractional-sample delay filter.

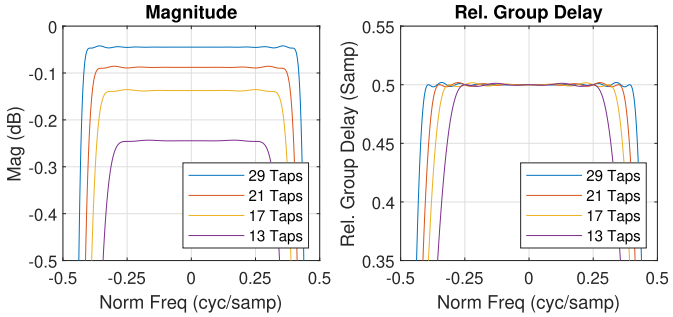

Fig. 2. Filter length comparison: $\frac{1}{2}$-Sample Delay, 16-bit fixed-point.

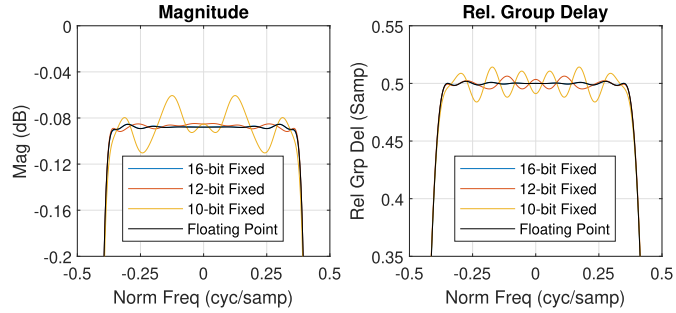

Fig. 3. Fixed-point precision comparison: $\frac{1}{2}$-sample delay, 21-Taps.

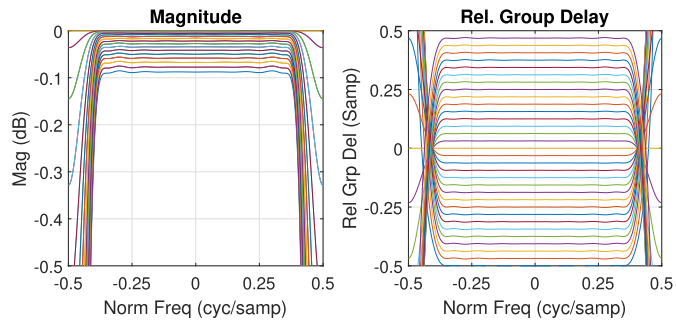

Fig. 4. Filter Bank: $\frac{1}{32}$-Sample Resolution, 21-Tap, 16-bit fixed-point. Each trace shows the frequency response for one of the 32 fractional-sample delay FIR filters.

2) Approximate Fractional-Sample Delay Filter: In order to design a finite, causal approximation, the ideal response must be appropriately truncated and shifted [28]. In general, merely truncating the response to some finite length l_{len} produces undesirable ripple in the frequency domain. A symmetric window function improves the ripple response appreciably at the acceptable cost of a small reduction in magnitude. Although many window functions exist, a Blackman window was utilized for the fractional-sample delay filter bank in this implementation. It is recommended to select an odd filter length given the majority of the sinc function energy is concentrated near the center of the response. Additionally, limiting the fractional-sample delay to $-0.5 \leq \frac{t_a}{T_s} < 0.5$ minimizes filter asymmetry. To achieve causality, the finite windowed sinc response is shifted to the right by $\frac{l_{\text{len}}-1}{2}$, assuming an odd length l_{len}. Thus, the final taps for a t_a-delay filter with odd length l_{len}, designed to operate on a signal sampled at frequency $F_s = \frac{1}{T_s}$, are given by

$$h_d[n] = w[n]\text{sinc}\left(\pi\left(n - \frac{t_a}{T_s} - \frac{l_{\text{len}}-1}{2}\right)\right), \tag{5}$$

where $w[n]$ is some window function, in this case a Blackman window, of length l_{len} and n is subject to the constraint $0 \leq n \leq l_{\text{len}} - 1$.

3) Filter Length: Considerations must be made for embedded system implementations given limited system resources. Figure 2 provides a comparison of the magnitude response and group delay for $\frac{1}{2}$-sample delay filters of various lengths. As longer filters provide lower loss and increased bandwidth, one must ensure sufficient hardware resources to maintain accuracy in high digital bandwidth applications.

4) Fixed-Point Quantization: FIR filters are typically implemented using fixed-point numerical representation rather than floating point due to computational efficiency. Figure 3 shows degradation in the frequency response due to different fixed-point precisions for a 21-tap $\frac{1}{2}$-sample delay filter. Black traces show the floating point response. Subsequent traces show the 16-bit, 12-bit, and 10-bit responses, respectively. Reduced coefficient precision causes increased ripple. Although the magnitude ripple is quite small, and likely inconsequential for most applications, group delay variations, particularly for 10-bit fixed-point coefficients, may be prohibitively large.

5) Fractional-Sample Delay Resolution: In real-time applications, filter coefficients are typically pre-computed for a finite set of prescribed delays rather than computed in real-time. Figure 4 shows the magnitude response and relative group delay of an example filter bank with a $\frac{1}{32}$-sample resolution. The relative group delay ignores the integer-sample delay associated with the FIR filter. The filter bank consists of thirty-two 21-tap filters with 16-bit fixed-point coefficients. A zero-fractional-sample delay filter is included, which provides the group delay reference for the rest of the filter bank. This ensures that the fractional-sample filter bank group delay is applied regardless of whether a nonzero fractional-sample delay is required for a given steering operation. Due to symmetry about the group delay reference, the magnitude responses of the negative relative shifts match those of the positive relative shifts. As quantization lobes due to finite fractional-sample delay resolution degrade system SNR [29], one must ensure sufficient resolution to support system requirements. In this example, the bank of 32 FIR filters has a resolution of 15.625 ps at a baseband sample rate of 2 GSPS. This gives a worst case phase resolution of about 21.4° at $F_{\text{high}} = 3.8$ GHz, slightly better than a 4-bit phase shifter.

C. Sub-Nyquist-Sampled Beamforming

Although bandpass sampling is theoretically valid for arbitrarily high Nyquist zones, the $3-$dB cut off for the RFSoC ADCs used in this testbed constrains the input spectrum to 4 GHz. As outlined in Section I, the beamformer testbed is designed to operate at a sample frequency of 4 GHz and support a 1.6 GHz bandwidth centered in the second Nyquist zone at 3 GHz. Spectrum aliasing due to sub-Nyquist sampling affects the relative phase of received signals, impacting beamformer compensation. This phenomenon is also present

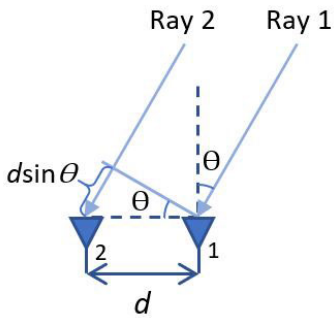

Fig. 5. Ray tracing geometry for 2-Element array.

when beamforming at complex baseband due to frequency shifting [8]. To determine the necessary phase shift, we consider a monochromatic planewave $x(t) = \cos(2\pi Ft)$ incident on the two-element ULA in Figure 5. The elemental signals are given by $x_{\mathrm{n}}(t) = \cos(2\pi F(t - \Delta t_{\mathrm{n}}))$, where $\Delta t_1 = 0$ and $\Delta t_2 = \frac{d \sin\theta}{c}$, as described in Eq (1). The sampled signals are given by

$$x_{\mathrm{n}}[m] = \cos\left(2\pi f m - 2\pi \frac{f}{T_{\mathrm{s}}} \Delta t_{\mathrm{n}}\right) , \tag{6}$$

where $t = mT_{\mathrm{s}}$, $F = fF_{\mathrm{s}} = \frac{f}{T_{\mathrm{s}}}$, and the sample period and sample frequency are given by T_{s} and F_{s} respectively. Because sinusoids are 2π periodic, when the magnitude of the normalized discrete frequency f exceeds 0.5, the time-varying component of the sinusoidal argument aliases to a new normalized frequency f' such that $-0.5 \leq f' < 0.5$, as given by

$$x_{a,\mathrm{n}}[m] = \cos\left(2\pi f' m - 2\pi \frac{f}{T_{\mathrm{s}}} \Delta t_{\mathrm{n}}\right) . \tag{7}$$

The constant phase term in Eq. (7) contains the original discrete frequency f rather than the aliased frequency f'.

To align the two receive tones, the first sensor signal must be digitally delayed by $\Delta t = \Delta t_2$. A delay sample index can be defined as $m_{\mathrm{d}} = m - m_0$, where the delay sample offset $m_0 = \frac{\Delta t}{T_{\mathrm{s}}}$, generally not an integer. Substituting m_{d} into $x_1[m]$ of Eq. (6) yields

$$x_{d1}[m] = \cos\left(2\pi f m - 2\pi f \frac{\Delta t}{T_{\mathrm{s}}}\right) , \tag{8}$$

which is coherent with the delayed tone $x_2[m]$ given in Eq. (6). By substituting m_{d} into the aliased signal $x_{a,1}[m]$ in Eq. (7), as given by

$$x_{ad,1}[m] = \cos\left(2\pi f' m - 2\pi f' \frac{\Delta t}{T_{\mathrm{s}}}\right) , \tag{9}$$

we note that the resulting phase offset differs from that in $x_{a,2}[m]$ in Eq. (7), namely $-2\pi \frac{f}{T_{\mathrm{s}}} \Delta t_{\mathrm{n}}$. A correction phase is defined as the difference in phase offsets between Eqs. (7) and (9), as given by

$$\begin{aligned} \phi_{corr} &= -2\pi \frac{\Delta t}{T_{\mathrm{s}}} (f - f') \\ &= -2\pi \Delta t \Delta F \ . \end{aligned} \tag{10}$$

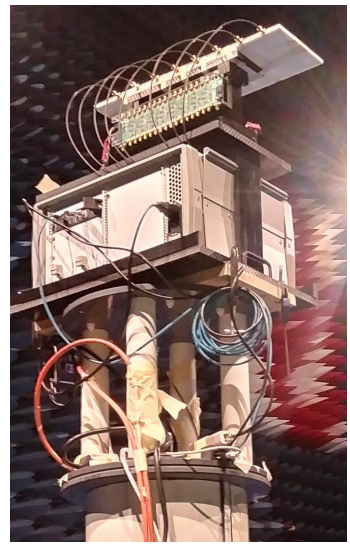

Fig. 6. Research testbed mounted in far-field anechoic chamber.

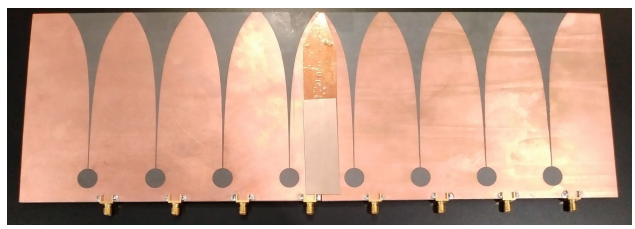

Fig. 7. Wideband vivaldi array used in the testbed in Figure 6.

This correction phase depends on the frequency difference ΔF between the original and aliased frequencies and the propagation delay Δt between the current and reference elements. Thus sub-Nyquist-sampled digital beamforming can be implemented via TTD filters and phase shifters. Note that pulse distortion should be considered if this correction phase grows beyond a single cycle.

III. Research Testbed

The wideband beamforming testbed is shown in Figure 6 mounted in the University of Oklahoma's (OU) far-field anechoic chamber. A Xilinx RFSoC is housed within the Pentek 3U virtual path cross-connect (VPX) chassis held at the base of the black high density polyethylene (HDPE) frame that was designed for this project. Eight MMCX-to-SMA cables provide the RF interfaces between the antenna elements and the RFSoC ADC channels for digital beamforming, which is controlled via a Secure Shell (SSH) interface to the Petalinux operating system (OS) running on the embedded real-time processor. To utilize the network analyzer for chamber measurements, the beamformer output is sourced out of the channel 1 DAC following digital upconversion. The upper chassis frame supports the wideband Vivaldi antenna aperture, shown in further detail in Figure 7. Specifically designed and fabricated at OU for this endeavor, the 8-element horizontally polarized linear array supports better than 2 GHz of bandwidth centered at 3 GHz. A 50 mm pitch yields half lambda spacing at the center of the band. The aperture's 66% fractional

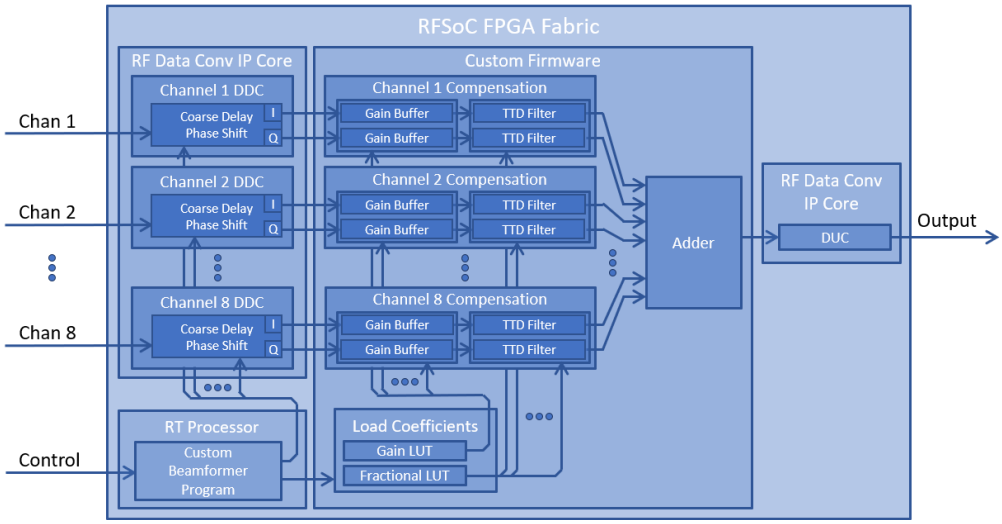

Fig. 8. Functional block diagram for the true time delay beamformer firmware design.

bandwidth supports the full digital bandwidth of the RFSoC, which utilizes 80% of the Nyquist zone providing a 1.6 GHz bandwidth at a sample frequency of 4 GHz. To facilitate analog baseline measurements to which the digital RFSoC results may be compared, a narrowband phase-amplitude control (PAC) board is mounted below the aperture. Used for beamsteering experiments throughout OU's Advanced Radar Research Center (ARRC) [30], the PAC board is included to provide a method for analog narrowband beamsteering measurements given in Section IV. It consists of eight analog channels, each providing 6-bit amplitude and 6-bit phase shifter control, with 0.5 dB resolution and 5.625° resolution respectively. A USB battery box and Raspberry Pi provide power and control to the PAC board.

The Pentek Quartz Model 5950 is a VPX board that employs our Xilinx Zynq UltraScale+ RFSoC. MMCX RF connectors provide transformer-coupled RF interfaces to the eight 4 GSPS ADCs and eight 6.4 GSPS DACs that are resident on the RFSoC. The full-scale inputs have a maximum of 8 dBm into 50 ohms. The input RF chains were designed to have a 3 dB passband of 10 MHz to 3700 MHz. The board also houses additional resources, such as DDR4 Random Access Memory (RAM), power management, and interleaved ADC calibration circuitry. Interleave calibration is periodically carried out whenever there is no signal present at the input. The Model 5950 board is housed in the Pentek VPX chassis shown in Figure 6, which provides power conversion, cooling, and interface access via the Pentek Rear Transition Module (RTM). The FPGA fabric within the Xilinx RFSoC facilitates extensive customization. The Pentek FPGA Design Kit (FDK) enables convenient set-up and initial operation, incorporating the Xilinx real-time processor, RF data converter IP cores, and the necessary logic for various interfaces to the Pentek hardware including 100 GigE UDP, PCI Express, and DDR4 RAM. Much of this interface logic was subsequently removed as beamformer control was provided via an SSH interface and the beamformer output was measured via a network analyzer out of the channel 1 DAC. Internal channel-channel synchronization was provided by the RF data converter IP core.

The functional block diagram for the custom FPGA image is provided in Figure 8. As discussed in Sections II-B and II-C, sub-Nyquist-sampled TTD beamforming requires an integer-sample delay, fractional-sample delay, and phase shifter for channel compensation. Xilinx's RF data converter IP core provides user control of the ADC and DAC, and subsequently DDC and DUC, resources. The 4 GSPS real-valued data generated by each of the eight ADCs is frequency shifted to baseband and decimated by a factor of two in the corresponding DDC. Because a real-valued signal is conjugate symmetric, decimation by two fully retains the digital bandwidth supported by the 4 GSPS system. The DDC provides an integer-sample delay of up to seven samples as well as phase offset control of the digital mixer's numerically controlled oscillator (NCO). This allows the integer-sample delay and relative phase shift to be implemented through software control of the DDC for single beam applications rather than through custom FPGA firmware. The gain buffer enables the application of various tapers as well as narrowband channel-channel leveling, if desired. Fractional-sample delays are implemented via instantiation of FIR filters. The conjugate-symmetric fractional-sample delay filter is implemented via real-valued coefficients allowing for independent filtering of the I and Q data streams. Finally, the compensated channel signals are summed in the adder and passed to the DUC, which interpolates by a factor of 2 and frequency shifts the beamformer output to the carrier frequency for transmission via the DAC interface.

In order to utilize the full digital bandwidth, the fractional-sample filter bank was designed to process multiple samples in parallel. While the complex baseband spectrum is represented by complex-valued samples at 2 GSPS, the fractional-sample filter bank is designed to operate at the FPGA fabric frequency of 250 MHz. This requires parallel processing of eight samples for both the I and Q data streams for each of the eight channels. Figure 9 shows an interleaved real-valued FIR

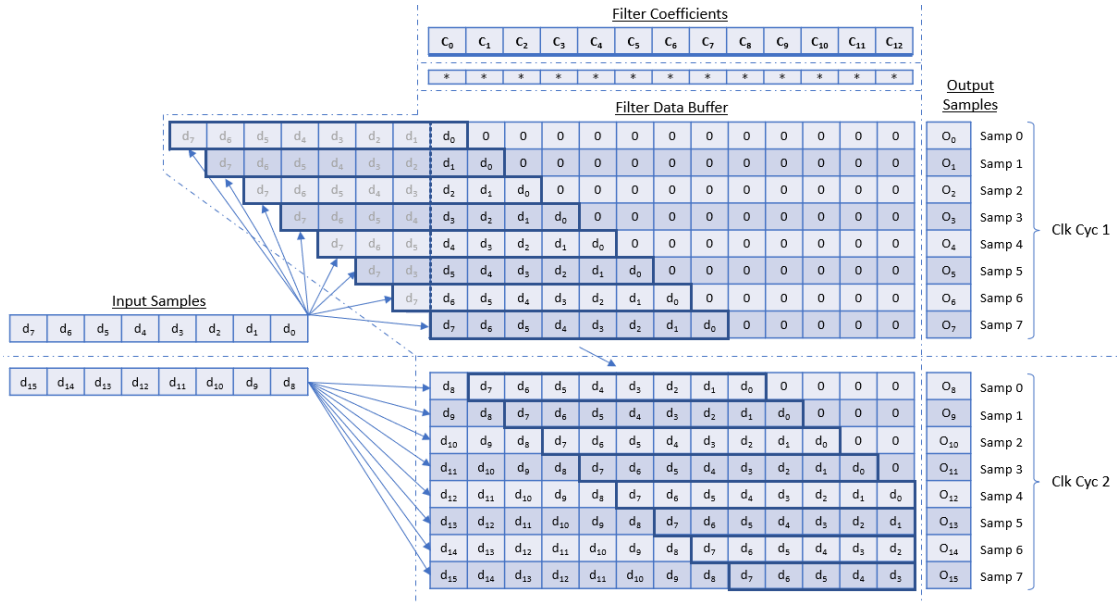

Fig. 9. Interleaved FIR filter diagram: parallel processing required to support full digital bandwidth.

TABLE I
WIDEBAND BEAMFORMER FPGA RESOURCE UTILIZATION

Resource	Utilization	Available	%
LUT	63808	425280	15.0
LUTRAM	3215	213600	1.5
FF	106831	850560	12.6
BRAM	28	1080	2.6
DSP	2304	4272	53.9
IO	35	347	10.1
BUFG	8	696	1.2
MMCM	1	8	12.5

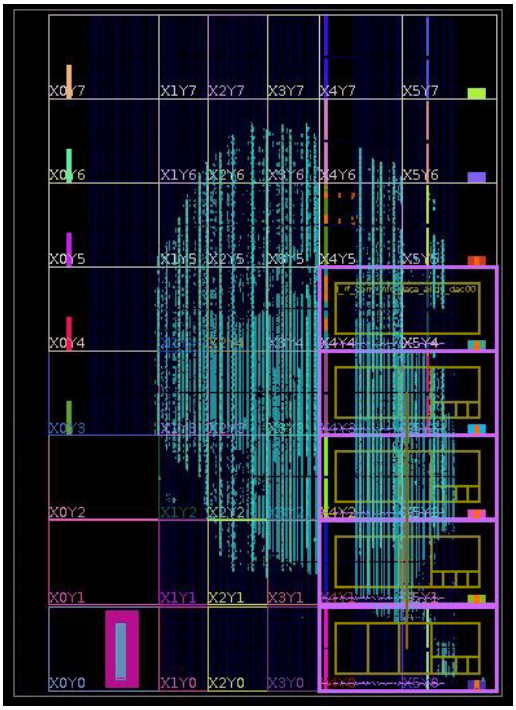

Fig. 10. True time delay Beamformer firmware layout: ADCs and DACs are located in the lower right.

filter implementation which processes eight samples per clock cycle. To maintain data throughput without further decimation, the filter must compute an output sample for each possible buffer offset necessitating resources for eight simultaneous filter instantiations. For each clock cycle, data in a given row is shifted eight samples to the right to make room for the next input sample set. The greyed-out samples represent registers which hold current input samples not required for the corresponding output sample but which must be stored for the upcoming clock cycle. This architecture requires eight multipliers per filter tap to produce eight output samples per clock cycle. Two interleaved filter instantiations are required for each of the eight channels, resulting in 128 multipliers per fractional-sample delay filter tap. The fractional-sample delay filter length was set to 17 taps, consuming 2176 DSP units for the fractional-sample delay filter banks. Filter coefficients utilized 16-bit fixed point precision and were computed for a $\frac{1}{32}$-sample resolution.

Device utilization is provided in Table I and the design layout is given in Figure 10. The primary resource of interest is DSP utilization, requiring 2176 DSPs for the fractional-sample delay filter banks and 128 DSPs for the gain buffers, enabling efficient taper application. A custom-designed IP core, shown in Figure 11, was developed in C++ using Vivado HLS and contains the fractional-sample delay filter bank and summation node. Vivado HLS provides an environment which facilitates rapid development of register transfer logic (RTL) designs using higher level programming languages such as C and C++. HLS enables the user to control how arrays are managed in memory or registers and dictate how hardware resources are allocated when implementing functional operations, such as parallelizing loop iterations and pipelining data flow.

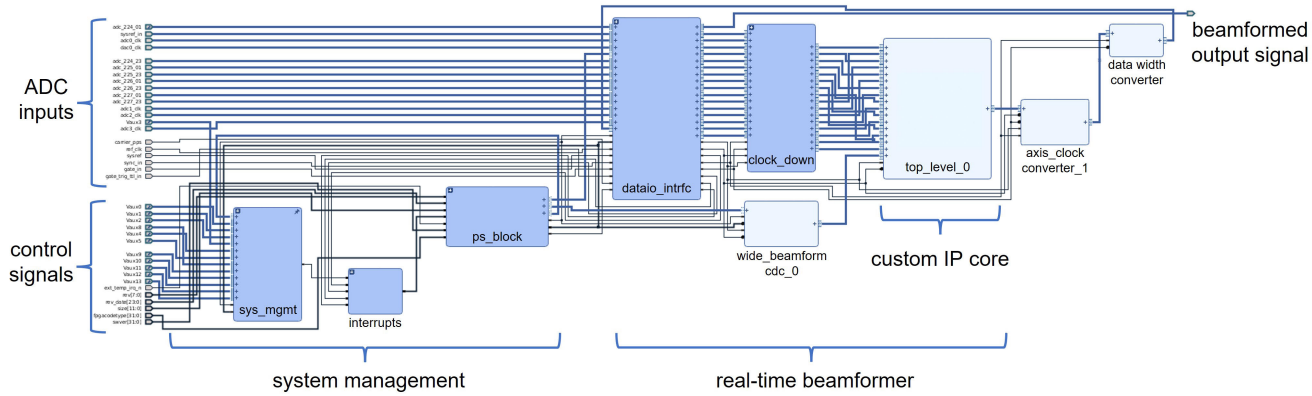

Fig. 11. FPGA firmware block diagram.

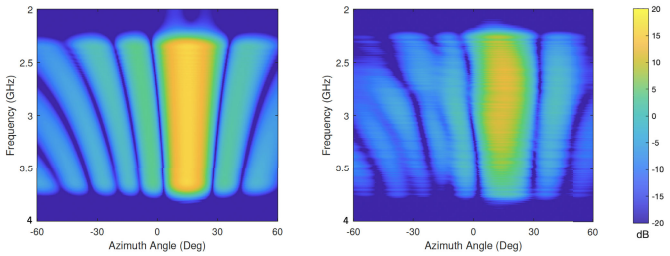

Fig. 12. Wideband simulation results steered to $\theta_{st} = 15°$, Left: Ideal Input Channel Data, Right: Measured channel data.

As discussed in the previous section, parallel resource allocation is necessary to take advantage of the full digital bandwidth. A custom C program executes within the embedded processor which memory maps the beamformer IP core, computes the necessary steering commands for the prescribed direction, and provides control data to the DDC, gain buffers, and fractional-sample delay filter bank.

IV. Results

In this section, we present simulated and measured results of beamformer performance. Section IV-A shows simulation results for ideal and measured channel waveforms. Following the completion of bench testing, far-field chamber OTA measurements were captured for several steering locations for both narrowband and wideband operating modes. These are presented and discussed in Section IV-B.

A. Bench-Top Loopback Tests

System modeling allowed comparisons of various performance parameters, such as fractional-sample filter lengths, fixed point resolutions, and fractional-sample resolutions. Bit-accuracy was incorporated to aid in the HLS development of beamformer firmware, allowing for the generation of test vectors for use with the HLS testbench. A chirp waveform, commonly used in radar systems, spanning 80% of the Nyquist zone was externally looped back over-the-wire to each ADC channel through an 8-1 splitter, allowing for simultaneous channel frequency response characterization. This captured data was fed into the system model to estimate the measured performance of the RFSoC wideband beamformer. Figure 12 shows a comparison of simulation results when sourced with ideal channel data and measured channel data. As the measured channel data lacks equalization, namely wideband magnitude and phase alignment, the measured channel data provides an expectation of the uncalibrated beamformer response.

B. Over-the-Air Results

OTA results were measured in OU's far-field anechoic chamber, shown previously in Figure 6. Wideband measurements were captured for three test cases: narrowband beamsteering using analog phase shifters on OU's PAC board, narrowband beamsteering using digital phase shifters on the RFSoC, and wideband beamsteering using digital TTD and phase shifters on the RFSoC. For each operating mode, the main beam was steered to 15°, 30°, and 45° at the center frequency of 3 GHz. Given the $\frac{\lambda}{2}$ aperture spacing at 3 GHz, a grating lobe can seen in the wideband beamsteering results at the high end of the 2 to 4 GHz measurement bandwidth. Measurements were captured for $-60° \leq \theta \leq 60°$. Note that the following figures employ the same intensity scale as is given in Figure 12.

Analog narrowband beamsteering results acquired using OU's PAC board, shown in Figure 13, provide a baseline for digital results measured on the RFSoC. Immediately apparent is the beam squint due to the large fractional bandwidth of the incident signal, which becomes more drastic with steering angle. The 3 dB beamwidth ranges from 17° to 10° over the signal bandwidth while the sidelobe level is about 11 dB. The RFSoC digital beamformer implementation supports narrowband beamsteering via phase control of the digital mixer's NCO. These results are shown in Figure 14 with a 3 dB beamwidth from 17° to 11° over the signal bandwidth and average sidelobe level around 9 dB. The main beam position and shape show strong alignment between the analog and digital narrowband beamsteering results, although less definitive nulls and degraded sidelobe levels shown in Figure 14 indicate stronger channel-channel magnitude and phase alignment in the PAC board. As wideband equalization on the RFSoC is not part of this paper, frequency-variant channel-channel magnitude and phase errors degrade sidelobe performance in the digital beamforming results.

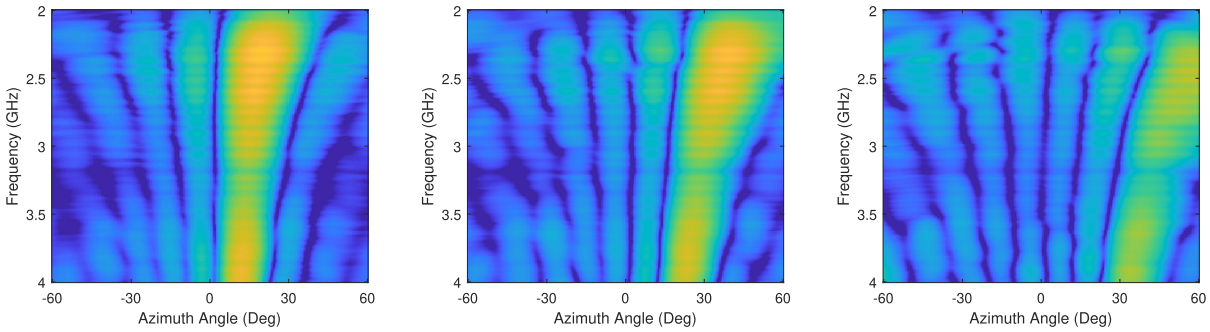

Fig. 13. Analog narrowband beamsteering results using OU's PAC board steered to 15°, 30°, and 45°.

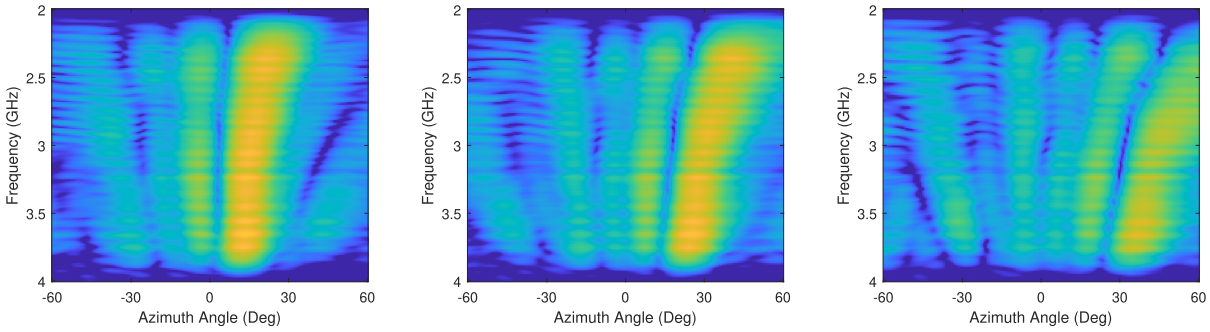

Fig. 14. Digital narrowband beamsteering results using the RFSoC steered to 15°, 30°, and 45°.

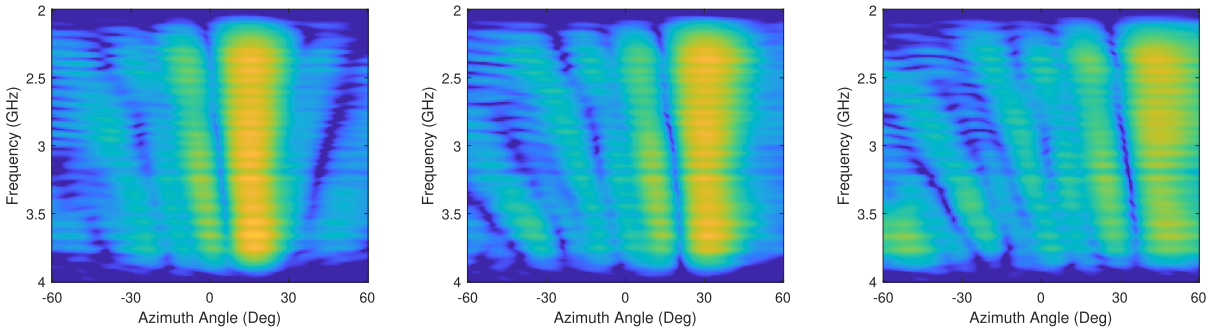

Fig. 15. Digital wideband beamsteering results using the RFSoC steered to 15°, 30°, and 45°.

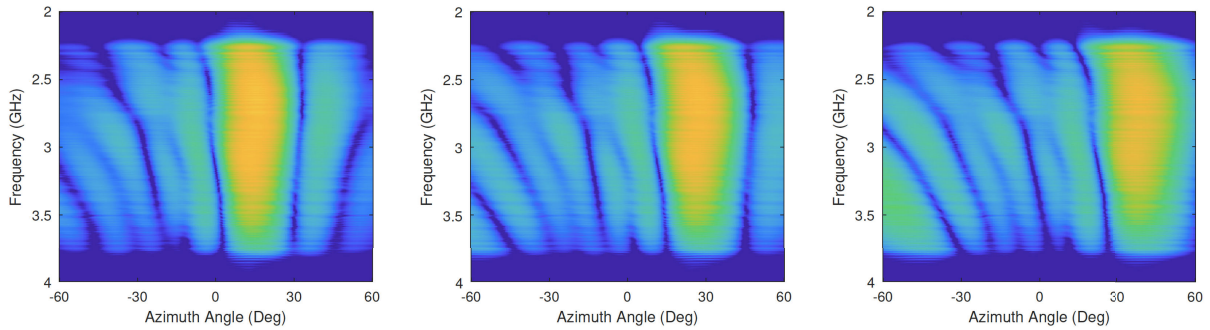

Fig. 16. Simulation results using measured channel data steered to 15°, 30°, and 45°.

Wideband digital beamsteering results are provided in Figure 15. Mainbeam angle accuracy maintained throughout the signal bandwidth indicates effective implementation of digital TTD and phase shifters required to mitigate beam squint over the large fractional bandwidth at complex baseband. The 3 dB beamwidth spans from 16° to 10° over the signal bandwidth while the average sidelobe level is about 9 dB. Bench-top measured channel data incorporated into system simulations, provided in Figure 16, show reasonable agreement with Figure 15. Similar sidelobe patterns indicate that effective

wideband equalization will improve sidelobe performance. We have described an approach to equalization for wideband systems in a recent paper [31], while the paper at hand concentrates on the wideband digital beamforming method.

V. Conclusion

Recently, the RFSoC is a unique, state-of-the-art, highly integrated device that incorporates an FPGA, an SoC architecture, and high speed ADCs and DACs operating at gigahertz speeds onto a monolithic device. In this paper, we have demonstrated the operation of an 8-element fully-digital sub-Nyquist-sampled array utilizing an RFSoC that implements digital TTD to achieve wideband digital beamforming. Array elements directly sample, at 4 GSPS, a 1.6 GHz linear chirp signal centered at 3 GHz, which folds into the first Nyquist zone upon sampling. As our theoretical equations show, signal compensation supporting the entire digital bandwidth is then applied at complex baseband following the digital downconverter. It is worth noting that the substantial resource requirements for the fractional-sample delay filter bank are dependent on several parameters: IBW, filter length, fractional-sample delay resolution, and fixed-point resolution. The authors sought to implement a beamformer which took full advantage of the available IBW while achieving a fractional-sample delay resolution of at least a 4-bit phase shifter. Sub-Nyquist-sampled beamforming enables direct sampling below the Nyquist frequency while maintaining waveform bandwidth. This simplifies system design by mitigating the need for traditional analog downconversion circuitry while allowing for lower sample rates, and thus lower power consumption. We acknowledge that for practical implementations, a multi-channel matching circuit, front-end amplification, and analog filtering would be best suited between the antenna and ADCs. Most importantly, we have confirmed that beam squint has been avoided. Given these concepts, this paper contributes the development and demonstration of a wideband digital beamformer on an RFSoC. A prototype system and chamber measurements confirm the efficacy of our approach.

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References

[1] J. Vivekanandan, A. Karboski, and E. Loew, "Airborne polarimetric Doppler weather radar: Antenna aperture and beam forming architecture," in *Proc. IEEE Int. Symp. Phased Array Syst. Technol. (PAST)*, Oct. 2019, pp. 1–6.

[2] N. Peters, C. Horne, and M. A. Ritchie, "ARESTOR: A multi-role RF sensor based on the Xilinx RFSoC," in *Proc. 18th Eur. Radar Conf. (EuRAD)*, Apr. 2022, pp. 102–105.

[3] S. Prager, B. Hawkins, M. Anderson, S. Chung, and M. Lavalle, "Development of ultra-wideband software defined radar testbed to support SAR tomographic mission formulation," in *Proc. IEEE Int. Geosci. Remote Sens. Symp. (IGARSS)*, Jul. 2022, pp. 4799–4802.

[4] N. R. Dusari and M. Rawat, "Multi tile synchronization and calibration of Xilinx RF SoC ZCU216 for digital beamforming," in *Proc. IEEE Wireless Antenna Microw. Symp. (WAMS)*, Jun. 2022, pp. 1–5.

[5] D. Werbunat et al., "Multiplexing of OFDM-based radar networks," in *Proc. IEEE Radar Conf. (RadarConf)*, May 2021, pp. 1–6.

[6] M. Harger, M. D. Conway, H. Thomas, M. Weber, A. Morris, and T. Hoffmann, "An update on the fully digital phased array development for next generation weather radar," in *Proc. IEEE Radar Conf. (RadarConf)*, Mar. 2022, pp. 1–6.

[7] R. Fagan, F. C. Robey, and L. Miller, "Phased array radar cost reduction through the use of commercial RF systems on a chip," in *Proc. IEEE Radar Conf. (RadarConf)*, Apr. 2018, pp. 935–939.

[8] S. Jang, R. Lu, J. Jeong, and M. P. Flynn, "A 1-GHz 16-element four-beam true-time-delay digital beamformer," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1304–1314, May 2019.

[9] S. Pulipati et al., "A direct-conversion digital beamforming array receiver with 800 MHz channel bandwidth at 28 GHz using Xilinx RF SoC," in *Proc. IEEE Int. Conf. Microw., Antennas, Commun. Electron. Syst. (COMCAS)*, Nov. 2019, pp. 1–5.

[10] T. Hoffmann et al., "Rapid integration of a flexible, wideband beamformer with wideband antenna technology," in *Proc. IEEE Int. Symp. Phased Array Syst. Technol. (PAST)*, Oct. 2019, pp. 1–5.

[11] T. Hoffmann et al., "IMPACT—A common building block to enable next generation radar arrays," in *Proc. IEEE Radar Conf. (RadarConf)*, May 2016, pp. 1–4.

[12] T. Hoffmann et al., "Measured performance of the IMPACT common module—A building block for next generation phase arrays," in *Proc. IEEE Int. Symp. Phased Array Syst. Technol. (PAST)*, Oct. 2016, pp. 1–7.

[13] H. Sun, W. Chiu, J. Jiang, A. Nallanathan, and H. V. Poor, "Wideband spectrum sensing with sub-Nyquist sampling in cognitive radios," *IEEE Trans. Signal Process.*, vol. 60, no. 11, pp. 6068–6073, Nov. 2012.

[14] F. Wang, J. Fang, H. Duan, and H. Li, "Phased-array-based sub-Nyquist sampling for joint wideband spectrum sensing and direction-of-arrival estimation," *IEEE Trans. Signal Process.*, vol. 66, no. 23, pp. 6110–6123, Dec. 2018.

[15] C. A. Samson, A. Bezanson, and J. A. Brown, "A sub-Nyquist, variable sampling, high-frequency phased array beamformer," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 64, no. 3, pp. 568–576, Mar. 2017.

[16] A. Burshtein, M. Birk, T. Chernyakova, A. Eilam, A. Kempinski, and Y. C. Eldar, "Sub-Nyquist sampling and Fourier domain beamforming in volumetric ultrasound imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 5, pp. 703–716, May 2016.

[17] I. Gurov, M. Taratin, and A. Zakharov, "High-speed signal evaluation in optical coherence tomography based on sub-Nyquist sampling and Kalman filtering method," *AIP Conf. Proc.*, vol. 860, pp. 146–150, Oct. 2006.

[18] B. D. Van Veen and K. M. Buckley, "Beamforming: A versatile approach to spatial filtering," *IEEE ASSP Mag.*, vol. 5, no. 2, pp. 4–24, Apr. 1988.

[19] F. B. Gross and J. Volakis, *Smart Antennas*. New York, NY, USA: McGraw-Hill, 2005.

[20] R. J. Mailloux, *Phased Array Antenna Handbook*. Norwood, MA, USA: Artech House, 2017.

[21] R. Rotman, M. Tur, and L. Yaron, "True time delay in phased arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 504–518, Mar. 2016.

[22] R. C. Hansen, *Phased Array Antennas*, vol. 213. Hoboken, NJ, USA: Wiley, 2009.

[23] M. Longbrake, "True time-delay beamsteering for radar," in *Proc. IEEE Nat. Aerosp. Electron. Conf. (NAECON)*, Jul. 2012, pp. 246–249.

[24] R. L. Haupt, "Phased array bandwidth defined by beam squint and pulse dispersion," in *Proc. IEEE Int. Symp. Antennas Propag. USNC-URSI Radio Sci. Meeting*, Jul. 2019, pp. 387–388.

[25] W. D. Jemison, "Analysis of the AO-FDPC optical heterodyne technique for microwave time delay and phased array beamsteering applications," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 7, pp. 1832–1843, Jul. 2002.

[26] T. Clark and E. Jaska, "Million element ISIS array," in *Proc. IEEE Int. Symp. Phased Array Syst. Technol.*, Oct. 2010, pp. 29–36.

[27] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay [FIR/all pass filters design]," *IEEE Signal Process. Mag.*, vol. 13, no. 1, pp. 30–60, 1996.

[28] V. Valimaki and T. I. Laakso, "Principles of fractional delay filters," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process.*, vol. 6, Jun. 2000, pp. 3870–3873.

[29] J. Corbin and R. L. Howard, "TDU quantization error impact on wideband phased-array performance," in *Proc. IEEE Int. Conf. Phased Array Syst. Technol.*, May 2000, pp. 457–460.

[30] M. Herndon, M. Yeary, and R. Palmer, "Studies of front-end distortion characterization via mutual coupling measurements in phased array systems," in *Proc. IEEE Int. Radar Conf. (RADAR)*, Apr. 2020, pp. 798–803.

[31] K. Steiner and M. Yeary, "Least-squares equalizer demonstrations using a full-digital bandwidth sub-Nyquist-sampled wideband beamformer on an RFSoC," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 58, no. 6, pp. 5519–5532, Dec. 2022.

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