Selection of Power Semiconductor Devices for A Standalone System Based on Power Loss Analysis

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Abstract—This paper presents a comprehensive methodology for the selection of power semiconductor devices in a standalone photovoltaic (PV)-battery system (SPBS) based on power loss analysis. The SPBS configuration is modeled analytically, and the waveforms for the system are obtained in a Hardware-In-the-Loop (HIL) and by simulation environment using Matlab. The study focuses on identifying the most cost-effective power semiconductor devices by assessing power loss at three distinct operating points. The algorithm evaluates losses in each component, facilitating the selection of optimal devices for enhanced system performance. The evaluation is performed for different operational modes, incorporating worst-case scenarios for current and voltage, providing a robust analysis of system behavior. By emphasizing the importance of power loss analysis in isolated PV systems, this research contributes to the advancement of energy efficiency in SPBS. The proposed methodology enables the identification of power semiconductor devices experiencing the highest losses, aiding in the selection of components that minimize overall losses and maximize energy utilization from PV panels and batteries.

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/8731

Index Terms— Analytical Model; Power Loss Analysis; Power Semiconductor Devices; Standalone Photovoltaic-Battery System (SPBS).

I. INTRODUCTION

Currently, power electronics devices play a vital role in the operation of electrical systems and devices such as power supplies, electric vehicles, and renewable energy systems [1], [2]. The selection of power electronics devices is crucial in designing efficient and reliable systems. One of the key considerations in device selection is the power loss analysis [3]. It involves analyzing the datasheet parameters, conducting simulations, and performing experimental tests to estimate the power loss in the device. The results of the analysis are then used to compare different devices and select the most suitable one for the application [4].

Power loss can be determined through three different modes: the physical model, the SPICE model, and the analytical model. The physical model, which considers parameters such as geometry and doping, offers greater accuracy, however, requires more computation time. In contrast, SPICE is widely

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used, providing good accuracy with lower computational time than the physical model, however, it is not suitable for working with databases involving a high number of devices. Finally, the analytical or mathematical model, based on equivalent circuits, offers better computation time, the significant challenge for this model lies in enhancing its accuracy [5].

Additionally, this analysis depends on different types of semiconductor technologies, their operating principles, and applications. Initially, all devices were manufactured based on silicon (Si). Still, technological evolution related to this semiconductor has practically reached its limits, imposing constraints on voltage rating, operating temperature, and switching frequency. These factors reduce the efficiency of static power converters. Thus, semiconductor technologies are being developed to address this need, with an emphasis on devices based on materials with a wide-bandgap (WBG) such as Silicon Carbide (SiC) and Gallium Nitride (GaN) [6]–[8]. Due to the high switching speed of WBG devices, it is possible to reduce switching losses and increase switching frequencies. Furthermore, it is possible to reduce the volume and weight of passive components used, reducing the amount of raw materials necessary to implement the prototype [9].

In the literature, numerous works apply power loss analysis. In the research by Chen et al. [10], a detailed loss analysis of phase-shifted full-bridge (FB) converters with auxiliary networks is presented, and a simplified loss analysis model is introduced. Using this model, the losses of FB converters with p-type and π-type auxiliary networks are thoroughly studied and compared. Ayachit and Kazimierczuk [11] present the derivation of the efficiency and the steady-state DC voltage transfer function of a lossy quadratic buck converter. Conduction losses for each component in the circuit are derived, and the total converter losses are expressed as functions of the duty cycle and the output power. In this case, an analytical model through simulations is employed.

The power loss of a 3-level Neutral-Point Clamped (NPC) inverter (3LNPCI) and a 3-level T-type inverter (3LTI) are classified and calculated according to the switching states in the study developed by Lee et al. [12]. As the switching loss depends on switching frequency, the power loss analyses have been done at the different operating points. power loss is calculated based on the physical model and PSIM thermal module by using the real parameter values of switching devices. Similarly, Naayagi [13] presented guidelines for selecting suitable power devices (IGBTs) for a 20 kW dual active bridge (DAB) converter prototype designed for aerospace applications. In this case, a loss analysis is conducted based on the physical model.

In Peng et al. [14], a simple and accurate analytical loss model for SiC power devices is proposed. This loss model considers the package and PCB parasitic elements in the circuits, non-linearity of device intrinsic capacitance, and ringing losses. The proposed model identifies the switching waveform subintervals and develops the analytical equations in each switching subinterval to calculate the switching losses. Besides, the research developed by Gurpinar and Castellazzi [15] compares the use of Si IGBT, SiC MOSFET, and GaN HEMT (high-electron-mobility transistor) in a T-type inverter. This study shows that GaN HEMT has the lowest gate driver losses above 100 kHz and SiC MOSFET has the lowest gate losses due to continuous current requirements. An experimental physical model was used to find this power loss.

Also, an analytical model is presented in the study of Castro et al. [16] to predict power loss and waveforms of high-voltage silicon superjunction (SJ) MOSFET during hard-switching operation. This model depends on the datasheet parameters of the semiconductors, as well as the parasitics obtained from the printed circuit board characterization. The high accuracy of the model is validated with experimental measurements in a double-pulse buck converter setup. In addition, Ahmed et al. [17] presents a power loss analysis of three-level neutral-point-clamped (3L-NPC) inverter using physical and analytical models. The switching energy loss of SiC MOSFET is measured and determined experimentally via an inductive clamp double pulse test (DPT) at the real working condition of the circuit. Then, this experimental data is used in the thermal description file of the device's library of PLECS simulation software to determine the total power loss. The power loss of the SiC 3L-NPC inverter is measured and compared with the theoretical results. This work presents accurate results, however, requires more computation time.

Additionally, Kwak and Ma [18] present a comparative power loss analysis among three types of converters: half-bridge buck converter, multi-level buck converter, and hybrid Dickson converter. The performance of each converter is evaluated in a high-voltage process, with major power switches implemented using power LDMOS (laterally-diffused metal-oxide semiconductor) FETs. The comparison among the power converters provides insights into the trade-off among silicon cost, system volume, and efficiency. In the article developed by Wang et al. [19], the simulation model of the inverter based on SiC MOSFETs is established to obtain its power loss. It is found that the total power loss of the inverter is linearly increased with the rise of switching frequency, which is mainly caused by the switching losses of MOSFET. Also, this analysis is verified by the experimental results.

Finally, Prado et al. [20] propose a simple and accurate analytical model for estimating switching losses on power MOSFETs. The proposed model is compared to other frequently used methods, confirming its accuracy across different voltage levels. The evaluation included four different MOSFET part numbers spanning three technologies: SiC, SJ, and conventional Si. This analytical model is recommended for applications that design converters by evaluating a large database of transistor part numbers.

In light of these considerations, this paper introduces a methodology for the selection of power semiconductor devices in a standalone photovoltaic battery system, based on power loss analysis. In isolated PV systems, analyzing losses is crucial for maximizing energy utilization from both PV panels and batteries. Therefore, enhancing system efficiency involves minimizing losses attributable to switching devices. This study aims to apply a power loss analysis for the system and to identify cost-effective devices with lower losses. The assessment encompasses an analysis of losses under various operation modes of the system, considering worst-case scenarios for both current and voltage in each device.

The paper is organized as follows: Section II describes the principles of the isolated SPBS. Section III presents the power loss analysis using the analytical models. Section IV showcases the results obtained after applying this analysis. Finally, Section V provides conclusions drawn from this work.

II. SYSTEM CONFIGURATION

The SPBS used as a reference in this work is presented in Fig. 1 and consists of a PV source, a battery, and an AC load connected through three power converters [21]. The power system is formed by two PV panels Tallmax from Trina Solar connected in series, and a Huawei VRLA battery. The parameters obtained from its datasheets are found in Table I [22], [23]. The DC bus voltage (V_{dc}) selected is 400 V to obtain an AC voltage (V_{load}) of 127 V_{rms} at the selected frequency of Latin America grids (60 Hz). Also, the power electronics system is formed by an isolated interleaved boost (IIB) converter, a Cuk bidirectional converter, and a 3-Level T-type ($3LT^2$) NPC inverter. The values of its passive components are obtained in [21] and are represented in Table II, where the high-frequency transformer (HFT) is considered ideal. Also, this SPBS works into four operation modes described in Table III, and detailed in [21].

TABLE I
PARAMETERS OF PV PANEL AND BATTERY USED

Parameters	Value
PV Maximum Power (P_{mpp})	450 Wp
Voltage at MPP (V_{mpp})	41 V
Current at MPP (I_{mpp})	10.98 A
Open circuit voltage (V_{oc})	49.6 V
Short-circuit current (I_{sc})	11.53 A
Battery voltage (V_{bat})	48 V
Battery capacity (Q)	20 Ah
Battery constant voltage (E_0)	49.1 V

III. POWER LOSS ANALYSIS

Based on previous analysis, the analytical models presented in [20], [24] and [25] are selected to carry out the power loss analysis in MOSFETs, IGBTs, and diodes of this work.

In MOSFETs, the on-state (P_{con}) and switching (P_{sw}) losses can be calculated using the following equations [20]:
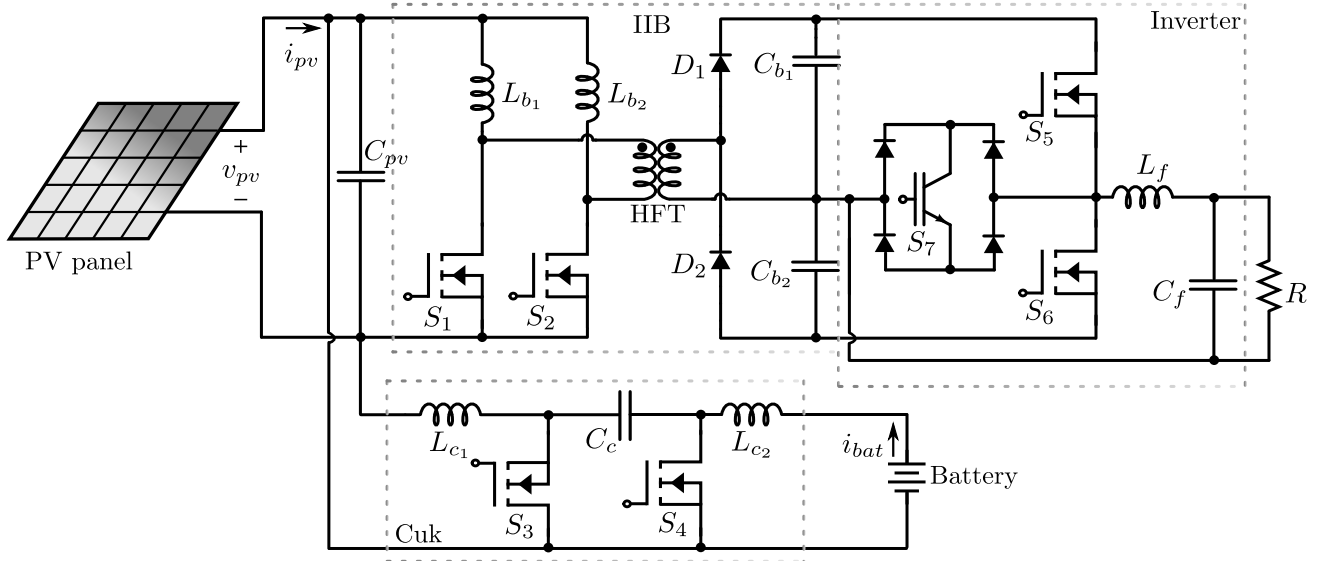
$$P_{con} = R_{DSon}I_{rms}^2; \tag{1}$$

Fig. 1. SPBS configuration used as reference.

TABLE II
VALUES OF PASSIVE COMPONENTS

Component	Value
IIB inductors (L_{b1-2})	350 μH
IIB capacitors (C_{b1-2})	220 μF
Cuk inductors (L_{c1-2})	500 μH
Cuk capacitor (C_c)	220 μF
Inverter inductor (L_f)	2.5 mH
Inverter capacitor (C_f)	80 μF

TABLE III
SYSTEM OPERATION MODES

Mode	Power Condition	PV Condition	Battery
1	$P_{pv} > P_{load}$	MPPT	Charging
2	$P_{pv} < P_{load}$	MPPT	Discharging
3	SOC $full$	Voltage Control	Disconnected
4	$P_{pv} = 0$	Disconnected	Discharging

$$P_{sw} = f V_{DS}(T_{on}I_{on} + T_{off}I_{off})/2; \qquad (2)$$

where R_{DSon} is the drain-to-source on-state resistance of the active component; I_{rms} is the root mean square current through the active component; f is the switching frequency; V_{DS} is the drain-to-source voltage over the active component; and I_{on}, I_{off}, T_{on} and T_{off} are the respective gate currents and overlap time of the active component turn-on and turn-off.

In IGBT, to determine the switching losses, the energy curves for the turn-on and turn-off presented in the datasheet are used [24]. The on-state losses can be calculated using an approximation of the IGBT as a series connection of a DC voltage source (V_{CE0}) representing the voltage at zero collector-emitter currents, and a collector-emitter on-state resistance (r_c) [25].

$$V_{CE0}(i_c) = V_{CE0} + r_c i_c. \qquad (3)$$

The V_{CE0} and r_c are obtained from the on-state characteristics curves provided by the manufacturer, where

$$r_c = \frac{\Delta V_{CE}}{\Delta i_c}. \qquad (4)$$

Therefore, the on-state losses can be written as,

$$P_{CIGBT} = V_{CE0}I_{MED} + r_c(I_{RMS})^2. \qquad (5)$$

The same procedure applies to the diode on-state losses, using the on-state characteristics curve (I×V) from the datasheet.

Similar to the previous cases, to determine the energies coming from reverse recovery in diodes and in MOSFETs body diode, the energy curves provided by the manufacturer are used.

According to [25], the reverse recovery energy (E_{rr}) can be obtained using,

$$E_{rr} = \frac{1}{4}Q_{rr}V_{Drr}; \qquad (6)$$

where V_{Drr} is the voltage across the diode during reverse recovery and Q_{rr} is the reverse recovery charge.

Furthermore, a database is used for MOSFETs, IGBTs, and diodes. For MOSFETs and diodes, Si and SiC components are considered in the database, while for IGBT, devices based on Si are used. For MOSFETs and diodes, SiC technology reduces the reverse recovery losses, as in voltages in hundreds of volts, reverse recovery can significantly reduce the efficiency of Si devices [26]. As presented in Fig. 1, the IGBT used has no diode, but the surrounding diodes provides four-quadrant operation (i.e bidirectionality).

For loss evaluation and device selection, an algorithm is developed to calculate the losses applied to the isolated configuration used, as observed in the flowchart in Fig. 2. The first step consists of obtaining the current and voltage waveforms for each active component. The evaluation is performed for different operational modes, incorporating worst-case scenarios for current and voltage, providing a robust analysis of system behavior (Section IV). Also, the databases
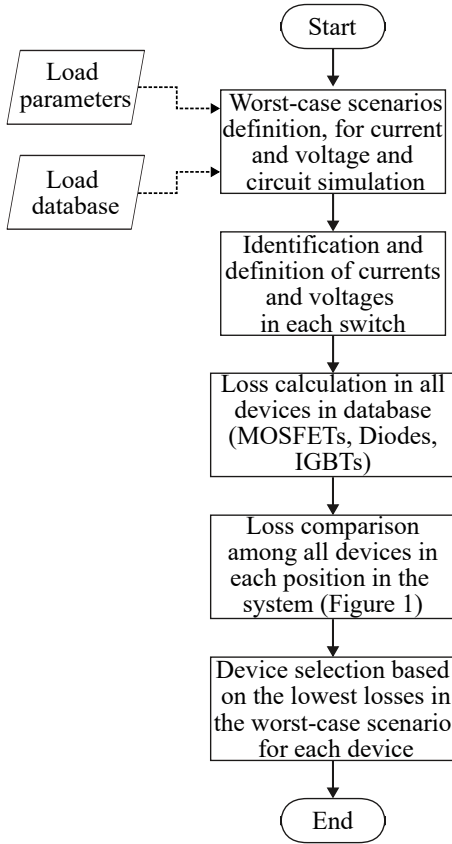
Fig. 2. Algorithm developed for loss evaluation and device selection.

TABLE IV
OPERATING POINTS USED

Point	PV Power	AC Load Power	Battery
1	900 Wp	500 W	Charging
2	450 Wp	1000 W	Discharging
3	0	1000 W	Discharging

This test starts by varying the irradiation from 700 W/m^2 to 300 W/m^2, and the system switches from Mode 1 to Mode 2, as shown in Fig. 4. In this situation, the battery that is storing energy starts to supply energy, so i_{bat} goes from a negative value to a positive value, and i_{out} maintains the same value since the load power is fixed. Also, the voltage values of 400 V on the DC link and 127 V$_{rms}$ at AC output are maintained, respectively. Then, the irradiation is varied from the previous value to 0, so the SPBS starts operating in Mode 4, as shown in Fig. 5. Furthermore, i_{bat} continues at a positive value, but its value increases as the system needs more battery power to supply the AC load. Also, i_{out} maintains the same previous value. Voltage values on the DC link and AC output are kept at 400 V and 127 V$_{rms}$.

Therefore, to carry out the power loss analysis, three different operating points are selected, to find in which system operation modes the losses are greatest in each component. These points are represented in Table IV, which includes three of four operation modes of the system where the battery is connected. The mode where the battery is disconnected is not analyzed, as the Cuk converter is not switched.

Thus, the first operating point is selected when the PV power panel (P_{pv}) is 900 Wp and the AC load power (P_{load}) is 500 W. In this case, as P_{pv} is greater than P_{load}, the battery is charging. From these values and those presented in Section II, this point is emulated in HIL simulation, and voltages and currents waveforms for all power semiconductor devices for a period of 100 μs can be obtained, as observed in Fig. 6. A full period of 10 kHz was used to encompass all the necessary parameters, since it is the lowest frequency used in the three power converters. Therefore, using the Matlab environment, the algorithm begins selecting the databases and parameters, identifies the voltage and current values, from the waveforms in Fig. 6, and calculates the losses in each component, as illustrated in Fig. 7. In this case, the switches S_1, S_2, S_3, S_4,

to use (Diodes, MOSFETs, IGBTs), and all the parameters taken into consideration in the analytical loss models presented are loaded in this step. The waveforms are obtained by using a circuit simulator, and this is validated first using hardware-in-the-loop (HIL) equipment. Furthermore, it identifies and defines the current and voltage levels applied to each device separately in each switch, obtaining the average, RMS, maximum, and minimum values for each one. Those are used to calculate the losses in all devices in the database. After obtaining the losses, all devices are compared, and the ones with the lowest losses for each position (Fig. 1) are selected for use in the power converters.

IV. RESULTS

In this Section, the SPBS is emulated using HIL equipment. The setup used to obtain the experimental waveforms comprises a Typhoon HIL-402, a DSP TMS320F28335 board, a Tektronix TBS1102C oscilloscope, and a computer, as shown in Fig. 3. Then, two PV panels Tallmax of 450 Wp and a Huawei VRLA battery of 48 V and 40 Ah are used and entered into the PV panel and battery models present in the Typhoon HIL software. Also, all current, voltage, and passive components values from tables I and II presented in Section II are inserted. Also, the switching frequencies used are: f_{sw} = 50 kHz for IIB and Cuk converters; and f_{inv} = 10 kHz for the 3LT^2 NPC inverter. Then, a test is performed to verify the waveforms, where the irradiation is varied keeping the load fixed at 500 W.
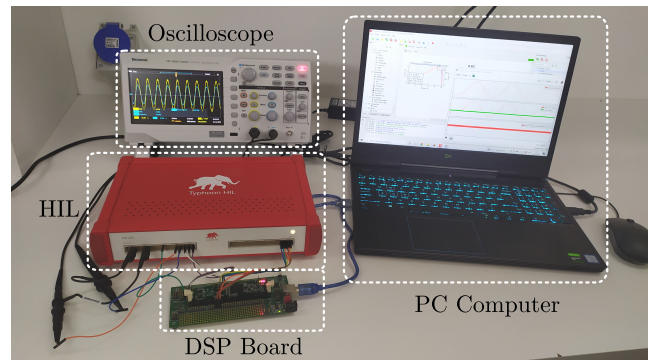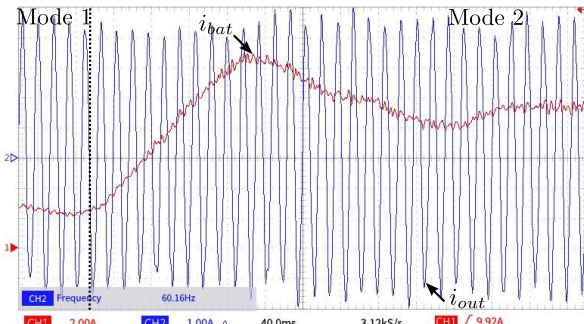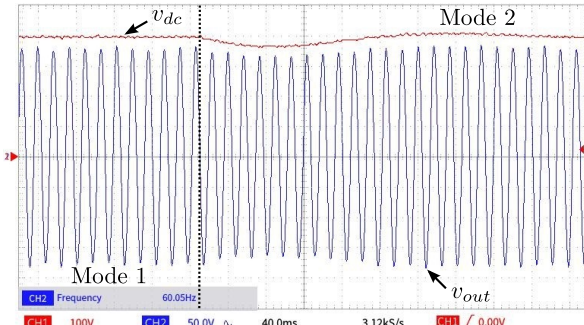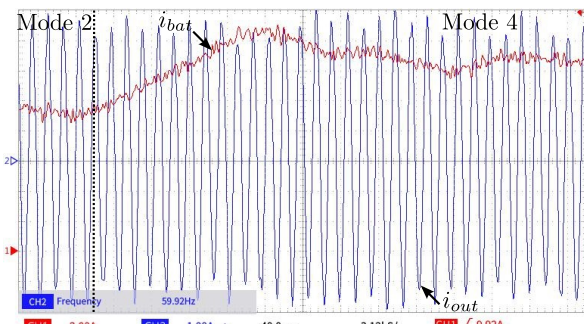

Fig. 3. Experimental testing platform.
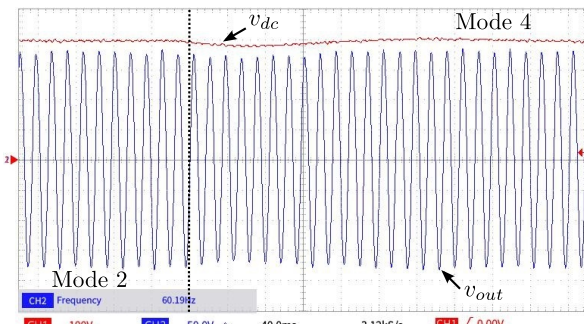
(a) Battery and output currents

(b) DC link and output voltages

Fig. 4. Measured waveforms obtained varying irradiation from 700 W/m^2 to 300 W/m^2 at fixed load power [21].
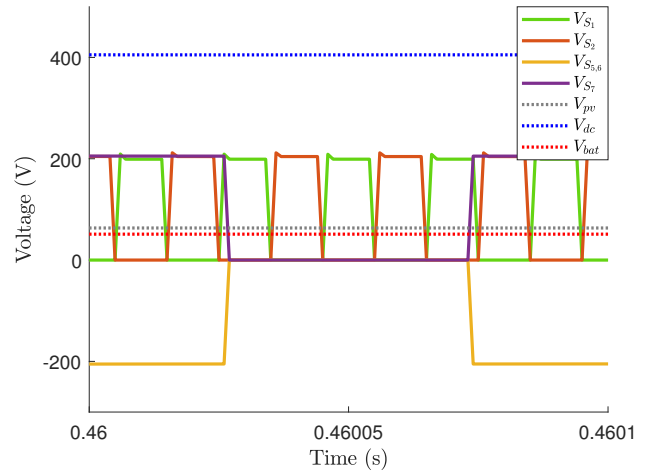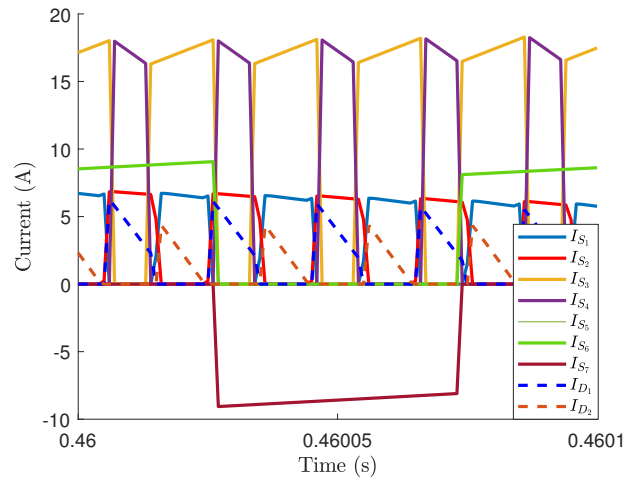

(a) Battery and output currents

(b) DC link and output voltages

Fig. 5. Measured waveforms obtained varying irradiation from 300 W/m^2 to 0 at fixed load power [21].

(a) Voltage waveforms

(b) Current waveforms

Fig. 6. Semiconductor waveforms for first point.

S_5, S_6, and the diodes D_1 and D_2 presented values lower than 1.5 W. About the bidirectional switch S_7 with its diode bridge (P_d), they presented the highest losses since they are always
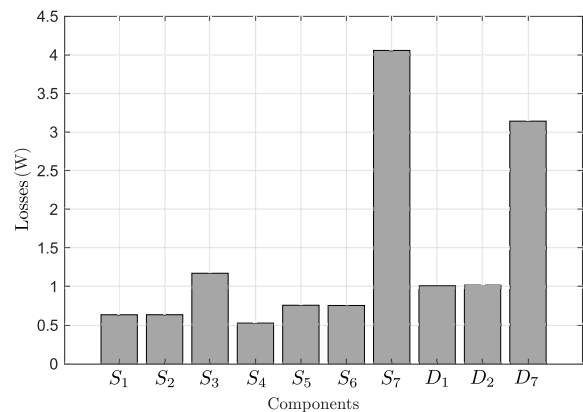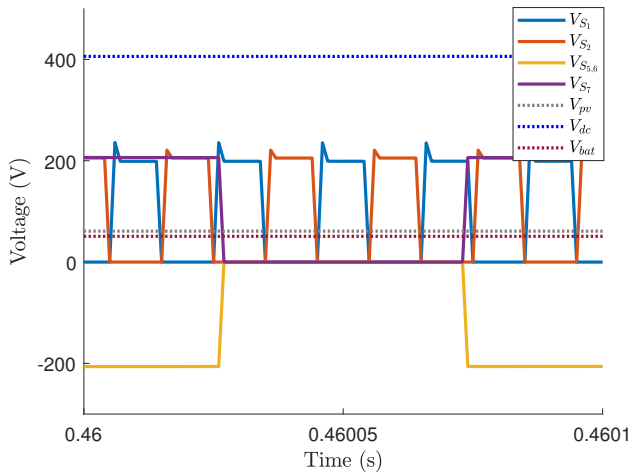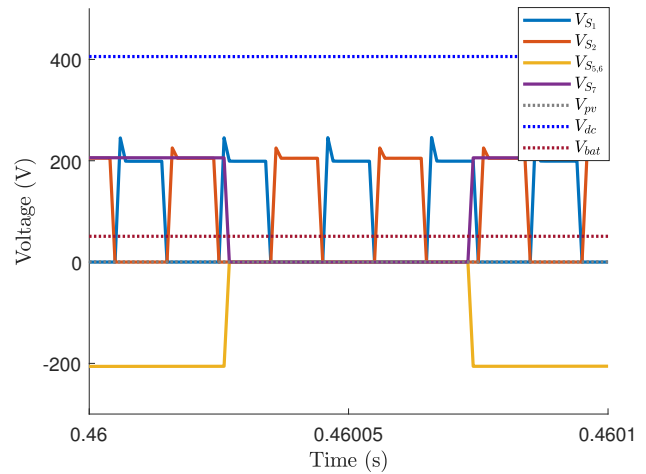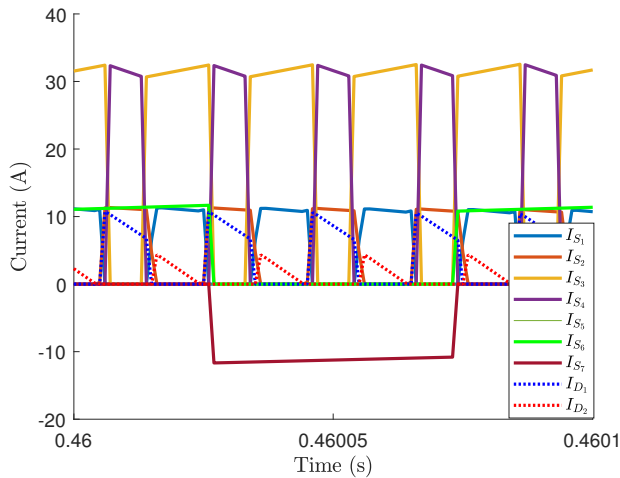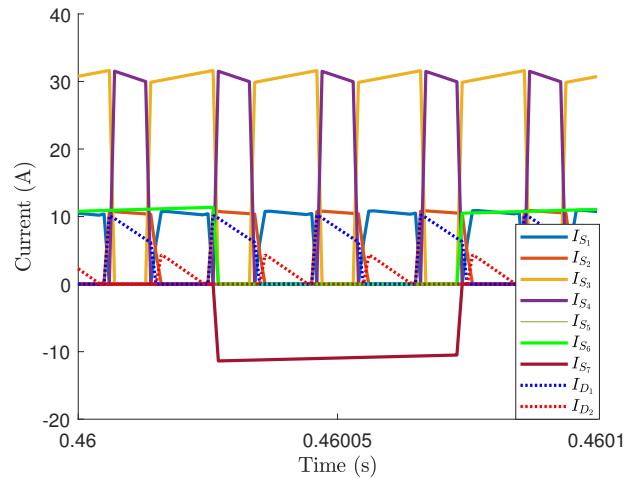

Fig. 7. Losses for the first operating point.

(a) Voltage waveforms

(b) Current waveforms

Fig. 8. Semiconductor waveforms for second point.

(a) Voltage waveforms

(b) Current waveforms

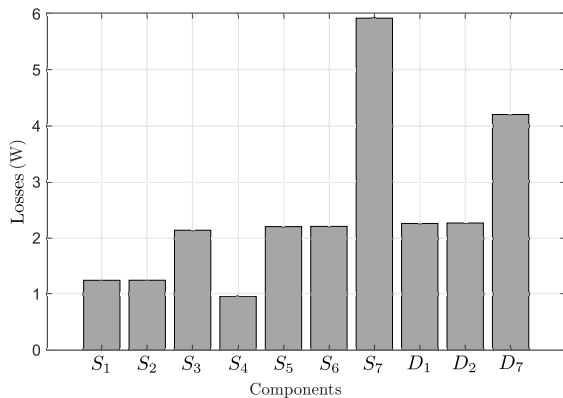Fig. 10. Semiconductor waveforms for third point.

Fig. 9. Losses for the second operating point.

commuting and conducting in both cycles of the AC output voltage. The separate loss values for each active component are represented in Table V, and their sum results in power loss: $P_t = 13.685$ W.

In the second operating point, where the power condition is: $P_{pv} = 450$ Wp and $P_{load} = 1$ kW, the battery begins to discharge to compensate for the demand by AC load. Then, this point is simulated in HIL, obtaining the voltages and currents waveforms for all power semiconductor devices in a period of 100 μs, as observed in Fig. 8. By inserting these previous values and maintaining the same values, the algorithm calculates their losses, as illustrated in Fig. 9 and Table V. It is possible to observe an increase in losses for all power semiconductor devices, which is expected, due to the increase in AC load power. The values of the switches S_3, S_5 and S_6, and the diodes D_1 and D_2 exceed 2 W and the bidirectional switch S_7 with its bridge P_d increases considerably. These values for each active component are represented in detail in Table V, which generates a result of $P_t = 24.633$ W.

Then, at the last operating point, where the PV panels are not generating energy, the battery has to provide the necessary power to feed the AC load ($P_{load} = 1$ kW). Thus, using this power value and maintaining the same values used in previous

operating points, this point is simulated, as observed in Fig. 10. In the Matlab environment, the algorithm identifies the voltage and current pairs in each active component and can calculate their losses based on parameters, databases, etc, as shown in Fig. 11. A similar behavior is observed to the previous one, for all power semiconductor devices except for S_3 and S_4, which had a considerable increase in losses. This is because the current leaving the battery increases to its maximum value, as it is the only power source for the system. Therefore, the separate loss values for each active component can be found in Table V, and their sum generates the following result: $P_t = 26.331$ W. Therefore, this last operation mode is the one that presented a greater number of losses compared to previous ones.

Based on the power loss analysis carried out at these three operating points and the database developed, applying the methodology presented in Section III, it is possible to select the power semiconductor devices to be used in future implementation, as the algorithm runs the loss calculation in all semiconductor devices, selection those with lowest losses among the devices. This selection is represented in Table VI, where the component model is shown, as well as the types, technologies, and their manufacturers. For the isolated inter-leaved boost (IIB) converter, and the Cuk bidirectional converter, Silicon-based FQPF45N15V2-D is selected, as it works in voltages in tens of volts. For the 3-Level T-type ($3LT^2$) NPC inverter and 400 V in DC link, SiC-based C3M0060065D is selected. For the diodes, SiC-based IDH20G65C6 is selected. For the IGBT, Si-based NGB15N41ACL is selected. It is worth highlighting that these devices are selected based on the worst scenario (operating points with the highest losses), those are highlighted in bold in Table V.

V. CONCLUSIONS

This paper has presented a power loss analysis, using the analytical model, applied to a SPBS to find the best cost-effective power semiconductor devices. The SPBS configuration used as a reference is presented and emulated using HIL simulation for three different operating points. Then, the algorithm developed in the Matlab environment is applied to these points, using all voltage and current waveforms, parameters, and databases, to find which components experience the highest losses. The algorithm can identify from here the recommended power semiconductor devices to use. The results corroborate the effectiveness of the power loss analysis presented. Highlighting

TABLE V
LOSSES FOR EACH OPERATING POINT, AND TOTAL LOSSES

Devices	Losses for first point (W)	Losses for second point (W)	Losses for third point (W)
S_1	0.632	**1.243**	1.178
S_2	0.633	**1.244**	1.177
S_3	1.171	2.137	**3.601**
S_4	0.525	0.957	**1.617**
S_5	0.756	2.201	**2.204**
S_6	0.753	2.205	**2.205**
S_7	4.055	5.921	**5.938**
D_1	1.005	**2.258**	2.106
D_2	1.016	**2.265**	2.094
P_d	3.139	4.202	**4.211**
Total Losses (W)	13.685	24.633	**26.331**

TABLE VI
POWER SEMICONDUCTOR DEVICES SELECTED FOR THE SPBS

| Devices	Type	Technology	Manufacturer	Model (main feature)
S_1	QFET MOSFET	Si	Fairchild	FQPF45N15V2-D ($R_{DSon} = 0.04$ Ω)
S_2	QFET MOSFET	Si	Fairchild	FQPF45N15V2-D ($R_{DSon} = 0.04$ Ω)
S_3	QFET MOSFET	Si	Fairchild	FQPF45N15V2-D ($R_{DSon} = 0.04$ Ω)
S_4	QFET MOSFET	Si	Fairchild	FQPF45N15V2-D ($R_{DSon} = 0.04$ Ω)
S_5	C3M^{tm} MOSFET	SiC	Wolfspeed	C3M0060065D ($R_{DSon} = 0.079$ Ω)
S_6	C3M^{tm} MOSFET	SiC	Wolfspeed	C3M0060065D ($R_{DSon} = 0.079$ Ω)
S_7	Ignition IGBT	Si	ON Semiconductor	NGB15N41ACL ($V_{CE(on)} = 2.1$ V)
D_1	Schottky Diode	SiC	Infineon Technologies	IDH20G65C6 ($V_f = 1.25$ V)
D_2	Schottky Diode	SiC	Infineon Technologies	IDH20G65C6 ($V_f = 1.25$ V)
D_7	Schottky Diode	SiC	Infineon Technologies	IDH20G65C6 ($V_f = 1.25$ V)
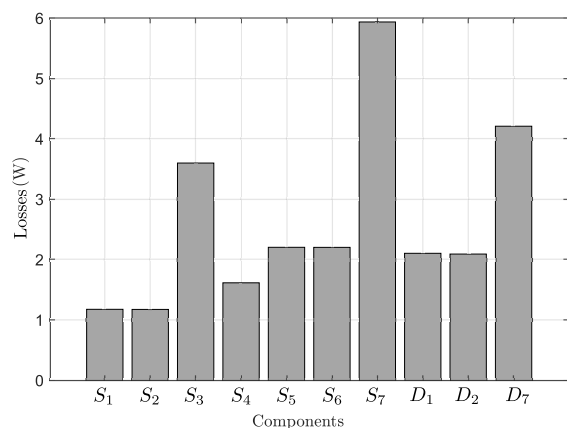
Fig. 11. Losses for the third operating point.

that for this project, scenarios two and three presented the highest losses.

ACKNOWLEDGMENTS

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