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Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter

Slavko Mocevic[1] ✉, Jianghui Yu[1], Boran Fan[1], Keyao Sun[1], Yue Xu[2], Joshua Stewart[1], Yu Rong[1], He Song[1], Vladimir Mitrovic[1], Ning Yan[1], Jun Wang[3], Igor Cvetkovic[1], Rolando Burgos[1], Dushan Boroyevich[1], Christina DiMarino[1], Dong Dong[1], Jayesh Kumar Motwani[1] and Richard Zhang[1]

ABSTRACT

Simultaneously imposed challenges of high-voltage insulation, high d*v*/d*t*, high-switching frequency, fast protection, and thermal management associated with the adoption of 10 kV SiC MOSFET, often pose nearly insurmountable barriers to potential users, undoubtedly hindering their penetration in medium-voltage (MV) power conversion. Key novel technologies such as enhanced gate-driver, auxiliary power supply network, PCB planar dc-bus, and high-density inductor are presented, enabling the SiC-based designs in modular MV converters, overcoming aforementioned challenges. However, purely substituting SiC design instead of Si-based ones in modular MV converters, would expectedly yield only limited gains. Therefore, to further elevate SiC-based designs, novel high-bandwidth control strategies such as switching-cycle control (SCC) and integrated capacitor-blocked transistor (ICBT), as well as high-performance/high-bandwidth communication network are developed. All these technologies combined, overcome barriers posed by state-of-the-art Si designs and unlock system level benefits such as very high power density, high-efficiency, fast dynamic response, unrestricted line frequency operation, and improved power quality, all demonstrated throughout this paper.

KEYWORDS

SiC MOSFET, modular multilevel converter (MMC), switching-cycle control (SCC), integrated capacitor-blocked transistor (ICBT), PEBB, medium-voltage (MV), high density, high efficiency.

Power electronic converters for medium-voltage (MV) have been extensively researched and utilized in a wide variety of applications such as: electric grid interface applications in highly populated urban areas[1,2], electric ship dc system[3], propulsion motor drive[4], railway traction[5], and renewable energy applications[6,7]. Due to often limited and expensive land and space, high-density and high-efficiency converters are required. Compared to the other topologies, modular multilevel converter (MMC) approach is increasingly considered due to features of modularity, scalability, resilience, transformless operation, and high power quality. For MV converters, 10 kV SiC MOSFETs are substituting their 6.5 kV Si IGBT counterparts due to inherent superiority[8], meanwhile offering system benefits of higher efficiency, higher switching frequency, high-density, topology simplification, and high control bandwidth. Consequently, if the power cell's (submodule's) kernel piece is SiC MOSFET, design will be able to meet high-density and efficiency, as shown in the lastest SiC MOSFET-based MMC converters[9–11].

To further improve power density and efficiency, drawbacks of MMC conventional control have to be overcome by reducing large capacitor voltage ripple at low-line-frequencies, caused by the capacitive energy oscillation. Recently, novel control named switching-cycle control (SCC)[12–14], leverages all switching states of the MMC converter enabling balance of the capacitor voltage within switching cycle. This causes a shocking 20–100 times reduction in the capacitor and inductor energy storage[15]. Additionally, topology called integrated capacitor-blocked transistor (ICBT)[16–18] provides an alternative solution to transfer power. It allows direct power flow between the input and output terminals of the converter, without having to transiently store energy in the cell capacitors. As a result, high cell capacitances are not required and arm inductors can be eliminated altogether, elevating power density compared to even SCC MMC.

Potential of these control methodologies combined with SiC MOSFET devices is enormous. First, these converters fully exploit the advantage of the fast commutation speed and high switching frequency offered by SiC, increasing power density and efficiency. Additionally, higher voltage rating and operating temperature of these devices, reduce the power-cell number and relax the cooling system requirements. Second, the converters can operate in both ac and dc conversion modes, a highly sought attribute for modular converters, greatly desired in the MVDC microgrids, as well as for shipboard MVDC distribution. Low frequency operation down to zero hertz also becomes an inherent hallmark of these converters, which is desirable for MV motor drive applications. Third, the proposed control methodologies feature unrestricted voltage and current scaling capability. Forth, and lastly, all these features can be attained using close to commercialization 10 kV SiC MOSFET modules, broadening the market size of these devices in pursue of lower costs and economies of scale.

Being expected to achieve strikingly elevated power density and efficiency, in reality, the power-cell and thus converter design

[1]Center for Power Electronics Systems (CPES), Bradley Departement of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA; [2]Center for Electromechanics (CEM), The University of Texas at Austin, Austin, TX 78758, USA; [3]Department of Electrical and Computer Engineering at the University of Nebraska-Lincoln, Lincoln, NE 68588, USA
Address correspondence to Slavko Mocevic, slavko7@vt.edu

based on 10 kV SiC MOSFET are facing simultaneously imposed challenges of high-voltage insulation, high dv/dt and electromagnetic interference (EMI), component and system protections, as well as thermal management. This paper presents an overview of the development, associated challenges, and demonstration of power-cell's key components. Apart from hardware, to achieve desired goals for modular MV converter, high-speed, high-performance communication and control network is as important and crucial. An overview of communication and control network recent developments are reported in this paper. Finally, modular and scalable two-cell-per-arm 12 kV converter prototype is built and experimental validations for SCC and ICBT are presented.

1 SiC-based power-cell architecture

To demonstrate benefits of SiC-based converter switching at medium-voltage, high-current, and high-frequency, power-cell (vital constitutive piece of the modular converter) will be built, requiring numerous new technologies to be developed and evaluated. The half-bridge power-cell (HB-PEBB) topology is selected, due smaller number of active devices, passive components, lower cost, and lower losses[19]. The HB-PEBB architecture, adopted in this paper, is shown in Figure 1. Kernel piece of the HB-PEBB is 10 kV SiC MOSFET. To fulfil the requirements for novel controls and to switch SiC MOSFET fast and reliably, new gate-driver (GD) is required. It needs to enable switching speeds > 100 V/ns meanwhile minimizing gate-loop inductance and having powerful current booster stage, fast short-circuit protection due to SiC MOSFET's narrow short-circuit withstand time, fast digital communication, and reduced common-mode (CM) current by minimizing input-output capacitance of isolated GD power supply. To not impede on the SiC benefits, busbar with minimized loop inductance, reduced weight, and effectively controlled E-field in and around it, printed circuit board (PCB) planar bus design will be explored. Other major power stage components include embedded dc-bus capacitors and AC inductor enabling high-frequency commutation without necessity for outside passives. Critical variables such as dc-link voltage and heatsink temperature are measured every switching cycle by fast digital sensors and sent to the controller through the fiber optic network. To prevent the propagation of aggressive noises inside the HB-PEBB caused by very fast commutation on high currents and voltages, and to minimize the number of power supplies, it is essential to develop the low input-output capacitance resonant current source power-supply to power the digital sensors and gate-drivers. For the developed HB-PEBB, the energy for auxiliary power system is provided from outside, by wireless power transfer auxiliary power supply (WPT-APS). Other components of the intricate power supply system are mini uninterruptible power supply (mini UPS), pre-charge, and discharge circuit for safe start-up and shut-down operations. Regarding communication and control, powerful computing facilities are distributed between the digital sensors, GD, and HB-PEBB controller which has powerful field programmable gate array (FPGA) and multi-core arm processor. These are connected over a custom optical fiber Mbps network inside the HB-PEBB and Gbps communication network with other HB-PEBBs. The HB-PEBB designed in this way exhibits complete modularity, excellent noise immunity, and a high degree of intelligence, making it capable for more advanced functionalities[20].

The HB-PEBB design objectives are $V_{dc} = 6$ kV, $I = 84$ A, operating at $f_{sw} \geq 5$ kHz, meanwhile keeping device junction temperature $T_j \leq 150$ °C. The insulation system design objectives are

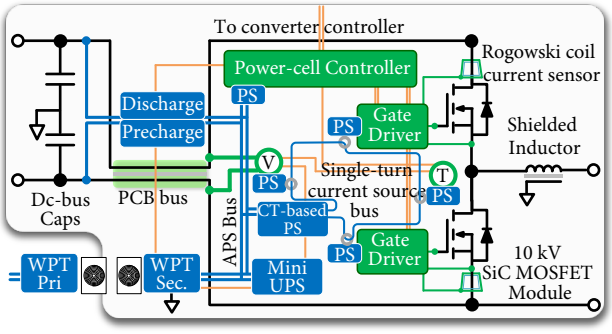

Fig. 1 Developed medium-voltage half-bridge power-cell system architecture diagram.

to maintain partial-discharge (PD) free operation under 6 kV differential-mode and 30 kV common-mode voltage. Additionally, HB-PEBB is expected to achieve strikingly elevated power density of ≥ 10 kW/L, with efficiency $\eta \geq 99\%$. In following, each of HB-PEBB technologies will be described in more details.

2 Semiconductor and gate-driver

2.1 SiC MOSFET power module

Extensive research to improve packaging techniques reducing parasitics influence, mitigating strong electric fields, and reducing EMI has been performed on MV (≥ 3.3 kV) all-SiC MOSFET devices in the recent years in both academia[21,22] and industry[23–27]. To fully explore the benefits of SiC MOSFET devices for MV high-power applications switching on high frequencies (≥ 5 kHz), the latest 10 kV, 240 A (maximum current available) Gen-3 SiC MOSFET XHV-6 from CREE/Wolfspeed is selected[25]. It comprises of 3 modules in parallel, a total of 18 dies per switch position. This module has the highest reported switching speeds and voltage slew rates of refs. [28, 29].

To demonstrate the benefits of XHV-6 device, it is compared with state-of-the-art commercial Si IGBT power module for MV applications from Infineon (FD250R65KE3-K)[30]. Figure 2 shows 16 times smaller SiC MOSFET switching losses than Si IGBT switching at rated current. Regarding conduction losses, SiC MOSFET has lower conduction losses at lower currents contributing to higher efficiency at low loading conditions. Additional comparison parameters are summarized in the Table 1. As seen, manifest benefits of selected 10 kV SiC MOSFET has a potential to substantially change the MV applications in the future.

2.2 Enhanced gate-driver

High-performance enhanced gate-driver (eGD) units are needed

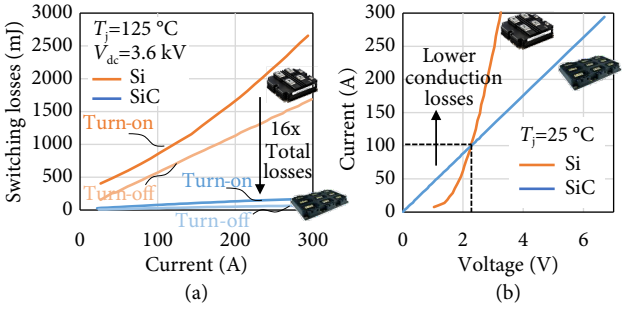

Fig. 2 Loss comparison between the Si IGBT[30] and SiC MOSFET[25,28] power modules. (a) switching losses, **(b)** output characteristics or conduction losses.

Table 1 Comparison between Si IGBT and SiC MOSFET for MV applications

Parameter	Si IGBT	SiC MOSFET
Rated current (A)	250	240
Max. blocking voltage (kV)	6.5	10
Power density (kW/L)	1656	4210
Max. temperature (°C)	125	175
Switching speed (μs)	> 1	< 0.2
Switching frequency	< 500 Hz	> 5 kHz

to maximally utilize 10 kV SiC MOSFET characteristics. Recently, there were a lot of efforts in the gate-driver development for MV SiC devices[31–33]. Even though they have relatively high breakdown voltage and small input-output capacitance, they exhibit relatively large size and limited intelligence for necessary control schemes. Therefore, novel gate-driver having high driving current capabilities, fast short-circuit detection, fast digital communication, and superb common-mode transient immunity (CMTI) is developed.

To enable extremely fast commutations of MV SiC MOSFET modules, current booster stage should feature: (1) high driving current; (2) low gate-loop inductance; (3) low losses; (4) compatible with soft turn-off upon short-circuit fault; (5) scalability to fit various current ratings. BJT totem-pole (TP) multi-cell configuration structure is proposed, able to supply very high currents with excellent current-balancing feature, able to achieve very low driving loop-inductance, keeping low losses, small profile, and is low cost[34]. For the developed eGD, maximum driving current is 90 A (which will allow reaching target switching speeds of 100 V/ns according to initial research on XHV-6 SiC MOSFET presented in ref. [28]), driving loop inductance is less than 5 nH, and near-ideal gate current sharing between paralleled devices is achieved, avoiding thermal issues due to current imbalance.

To achieve fast short-circuit detection, high-bandwidth-and-accuracy Rogowski switch-current sensor (RSCS) for protection of the SiC MOSFET device is developed[34,35]. The PCB with embedded Rogowski coils is placed between the module and PCB planar busbar so that the current going through the spacer connecting the two is measured. Special attention in coil design is dedicated to satisfying the PD-free requirement under high-voltage operation, meanwhile preserving high power density[36–39]. Fast short-circuit protection is achieved with detection in under 80 ns, while safely protecting the device in less than 1.5 μs with two-level soft turn-off. Apart for protection, RSCS serves as a peak-current-mode control sensor in SCC, and as a phase-current sensor in ICBT, sampling the switch current with an analog-to-digital converter and sending it to the local FPGA, and later the controller, through a communication protocol. More information about current sensing system, it's performance, accuracy, and self-calibration are in refs. [35, 40].

As one of the main challenges, superb CMTI due to extremely fast commutations (> 100 V/ns) is required. This is further pronounced by requirement of fast digital communication and signal processing that can easily be disrupted. To overcome this issue and provide clean and stable voltages for signal processing and driving, avoiding false triggering/signal malfunction/communication loss, novel gate-driver architecture is proposed[34]. Impedance control technique is applied to create a mismatch between power and signal propagation paths of CM current (noise) created with fast commutation of device. Power path has higher admittance than signal path on higher frequencies (for over 80 dBS) for CM current. This redirects CM current to power path, bypassing the driving and processing signal path, thus protecting eGD from malfunction of logic. Additionally, active Miller clamping circuitry is employed to increase the cross-talk immunity designed according to ref. [41].

To further bolster CMTI, novel current transformer-based power supply (CT-based PS) is developed. More on the CT-based PS in Section 3. Developed eGD with RSCS, powered by novel CT-based PS mounted on an XHV-6 SiC MOSFET module is shown on Figure 3. Enhanced GD operation verification can be found in refs. [35, 40, 42].

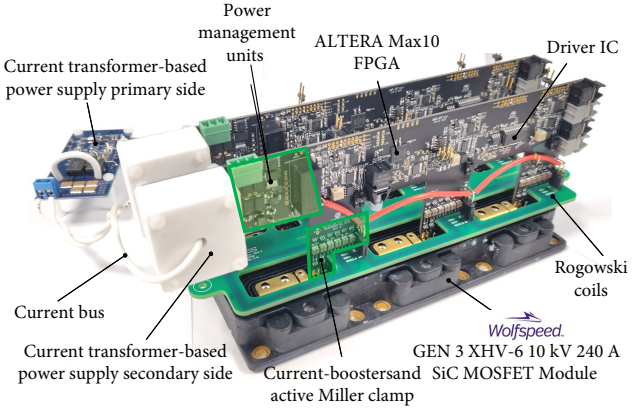

Fig. 3 Two eGD boards with CT-based PS assembled with a Rogowski coil board on an XHV-6 SiC MOSFET.

3 Auxiliary electronics

3.1 Auxiliary network architecture

The design of auxiliary power supply (APS) for gate-drivers, controllers, and sensors is critical, due to influence of high dv/dt which bringing challenges in insulation design and EMI mitigation. APS needs to ensure high-reliability, high-efficiency and power density, high-insulation capability, and low EMI susceptibility. For internally powered APS solutions[43,44], APS is fed from internal dc-caps of power-cell. Even though this type of solution provides scalability, drawbacks are high-step down ration converter design, and dependency of power with power-cell which can potentially present issue during start-up or power-cell failure. For externally powered methods, APS is powered from outside the main power system, from low-voltage earthed source. These usually utilize transformers with high-voltage isolation capabilities[45], or wireless power transfer[46]. Benefits are reflected in power independence (attaining higher reliability by making sure the gate-driver and controller are powered and not related to state of power-cell), high-insulation capabilities, and flexible mechanical structure. Consequently, it may not be practical to have an earthed APS network in HVDC applications, but this approach is still manageable and beneficial for MV applications.

As proposed in ref. [47], Figure 1 show the two-stage auxiliary power network architecture for a SiC MOSFET-based HB-PEBB. The black components in Figure 1 show the main power components of the HB-PEBB. The green part shows all the possible loads including controller, eGDs, voltage senor, and temperature sensor that require power from the auxiliary system. The blue part shows the auxiliary network components of the two-stage solution. Architecture of the auxiliary power supply network is quite

intricate. The first-stage is the wireless power transfer converter (WPT), getting power from a 48 V dc power supply with reference point connected to the earth. The second-stage is the current-transformer based power supply (CT-based PS) fed from the WPT. The reference point of the auxiliary power supply (APS) bus, which is the output of WPT and input of CT-based PS, is connected to the mid-point of the dc-link capacitors. Each HB-PEBB has 6 kV dc-link voltage and the mid-point of the dc-link is connected to APS bus as shown in Figure 1, the second-stage CT-based PS only needs to hold half of the bus voltage which is a bipolar 3 kV square wave voltage excitation. In this case, the first-stage needs to hold $3+6(N-1)$ kV, where N is the number of HB-PEBBs. With this two-stage solution, the first-stage can focus on high insulation design and the second-stage can focus more on voltage regulation. Also, the constant voltage bus of the first-stage makes it easier to add a UPS backup system. With the constant current bus on the second-stage, short-circuit failure on certain loads will not interfere with other loads' operation. Hardware prototypes of the CT-based PS and WPT are shown in Figure 3 and Figure 4(a), respectively. Performance for both WPT and CT-based PS are listed in Table 2. Power ratings for the CT-based PS and WPT are defined according to the requirement of load consumption when they are utilized in full-bridge power-cell which contains four gate-drivers, three sensors, while rest of auxiliary components are same as in half-bridge power-cell in Figure 1. Other components of the system include pre-charge, discharge, and mini-UPS circuits with design and test results shown in ref. [48]. Hardware prototypes of the pre-charge, discharge, and mini-UPS circuits are presented in Figure 4.

3.2 Wireless power transfer converter

For the WPT designed specifically as an medium-voltage APS, three design requirements should be met simultaneously. First, the efficiency η of the converter should be high. Compared to losses of the megawatt power rating medium voltage converter, losses from APS contributed to the total system are negligible. However,

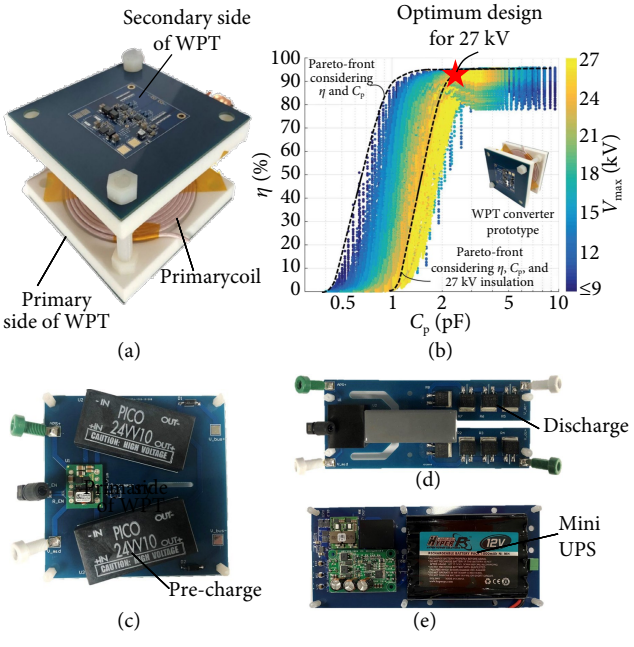

Fig. 4 **(a)** Hardware prototypes of the WPT. **(b)** Multiobjective optimization result of coils for WPT. The optimum design for 27 kV is marked with red star. **(c)** Hardware prototype of pre-charge. **(d)** Hardware prototype of discharge. **(e)** Hardware prototype of mini-UPS circuits.

Table 2 Performance of WPT and CT-based PS

	WPT	CT-based PS
Efficiency (%)	93	85
Isolation capacitance (pF)	2.78	1.86
Insulation rating (kV)	30	5
Power rating (W)	160	120
Closed-loop control	No	Yes

the space of the HB-PEBB is very limited due to the highly compact design requirements. Therefore, the high efficiency can help APS shrink the size without having thermal dissipation issues. Second, the coil pair should have low isolation capacitance C_p between transmitter and receiver. For SiC-based HB-PEBB, the switching node of the half-bridge can have dv/dt as high as 100 V/ns. The coupling capacitance should be minimized to reduce the induced common-mode current since this EMI problem can ruin the performance of controllers and sensors. Third, the coil should have adequate insulation capability considering medium voltage converter applications. Therefore, a multi-objective optimization process taking all the requirements into consideration is necessary. In order to meet these requirements, a GaN-device-based resonant converter using Litz wire as coil winding is implemented. The result of multiobjective optimization is in Figure 4(b), with indicated optimum design for 27 kV. More detailed design, optimization, and testing results can be found in the following papers including the series-series-CL resonant circuit topology[49], multi-objective optimization[50], and insulation design[51].

3.3 Multi-channel current-transformer based power supply

Ideally, ultra-high isolation capability, with negligible coupling capacitance can be achieved with power over fiber[52]. However, it exhibits low efficiency, limited power, and impractical bulky laser transmitter. Other recent solutions are offered in refs. [32, 53], but offer only single load solution, with relatively bulky transformer designs. This paper expands solution originally proposed in ref. [54] by optimizing size, insulation capabilities, efficiency, and coupling capacitance.

As shown in Figure 1, the CT-based PS serves as the main power supply for gate drivers and sensors in PEBBs. To supply distributed loads simultaneously, a load-independent current bus achieved by resonant topology is designed for the CT-based PS. In this case, all loads are linked in series and are thus immune to short-load conditions. However, to regulate the output voltages for different load conditions and prevent open-circuit failure, an additional feedback loop is necessary. Thus, on each secondary side of the CT-based PS, a current-fed switching network is designed with a hysteresis controller. Besides multi-load driving and regulation capability, a medium insulation level with a compact form factor is another design consideration for CT-based PS to realize integration with gate drivers and sensors. To achieve so, a single-turn transformer using insulating wire with an operating frequency of 1 MHz is developed as shown in Figure 3. Air is used as medium between insulated wire and transformer core. Finally, minimization of the common-mode coupling capacitance (C_{cpl}) between the input and output of the transformer is required because the CT-based PS will experience high dv/dt during converter operation, which potentially induces EMI problems. Figure 5(a) shows experimental results of CT-based PS regarding coupling capacitance and insulation capabilities. Impedance analyzer Agilent 4294A is used to measure the coupling capacitance. Coupling ca-

pacitance of complete receiving side together with transformer is measured to be 1.86 pF. For the insulation test, the secondary side of CT-based PS integrated on GD is excited by a 60 Hz high-voltage ac source, and the current bus wire is referenced to earth ground, as shown in Figure 5(b). Both high-frequency current transformer (HFCT) and Omicron MPD-600 PD detector are used to measure the PD signals. Phase resolved partial discharge (PRPD) pattern (Figure 5(c)) shows voltage excitation represented with green sinusoidal waveform while each individual discharge event is plotted against the phase in which it occurred. PRPD pattern represents collections of these discharge events over time (in our case close to 5 minutes). Blue color indicates less events occurring, and red indicates higher repetition rate at particular magnitude and phase. Device under test is considered PD-free until magnitude of discharge is bellow of threshold 10 pC, according to IEC 60664-1 standard. In the experimental insulation test for air-insulated CT-based PS design, CT-based PS achieves PD-free operation until 5.8 kV, after which starts having discharges in the air-gap between primary side current bus wire and secondary side transformer core. The specific design process of the CT-based PS are discussed in refs. [55–57].

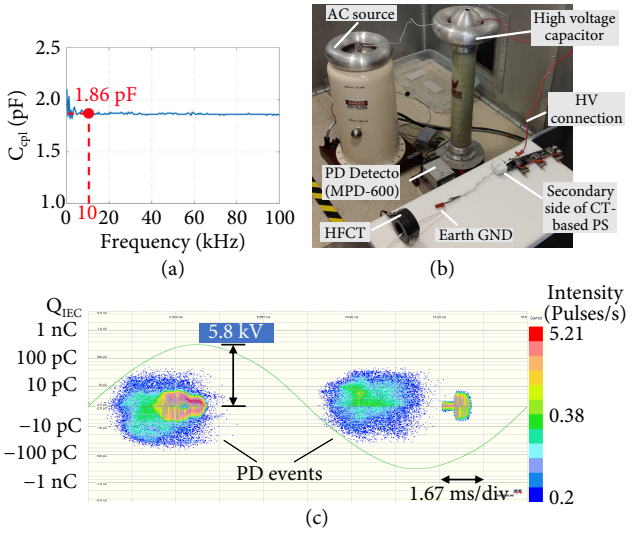

Fig. 5 **(a)** Coupling capacitance measurement results. **(b)** Setup for insulation test. **(c)** PD test result for design CT-based PS.

4 PCB-based dc-bus design

A dc-bus serves as an interconnect between components in the power loop such as SiC MOSFET power modules and bulk capacitors. To fully utilize the benefits offered by the fast switching nature of SiC MOSFET, a low inductance power loop is imperative. The planar laminated bus is a common solution that reduces the effective inductance, compared to the coplanar variant, through the cancellation of mutual inductance[58]. As mutual inductance is directly proportional to the distance between the layers, it is desired to make the layer thickness as small as possible[59]. However, the thickness must be carefully controlled for MV busses, as the average electric field (E-field) intensity is inversely proportional to the spacing between two layers.

A traditional planar laminated bus was previously constructed in ref. [20], with an overall thickness of 17.5 mm. GPO3 insulation plates are implemented between positive (+dc) and negative (-dc) layers with thickness of 5 mm, while a 2.5 mm insulation layer is between positive or negative and adjacent middle (mid) layers. Adhesive and encapsulating material are applied to attach layers together, as well as sealing the bus edges. Layer to layer insulation quality was tested via PD measurement and observing the phase resolved partial discharge (PRPD) pattern. According to ref. [60], this design failed initial PD testing. It exhibits around 1 nF discharges at only 4 kV rms between the positive and negative layers, where the general requirement allows less than 10 pC discharge at designed operation voltage. After further analysis, this is likely due to defects in the thick insulation layers, adhesive layers, or even at conductor edges near terminals or the edge of the bus where E-field intensities are high. As a result, both fabrication and design must be improved[60].

PCB-based planar laminated bus is proposed to improve the fabrication and design since PCB manufacturing technologies are mature and readily available. A detailed method for controlling the peak E-field intensity was implemented[61] for each of the various terminals, cutouts, and the board edge. Here, as an example, the 2D section view of the PCB based bus along one of its interconnection regions is shown in Figure 6(a). With adjusting insulation thickness between different layers and offsets, the E-field intensities in and out of the board can precisely be controlled. Via FEA simulation it is confirmed that the maximum E-field intensity inside the PCB is lower than 20 kV/mm with no more than 2 kV/mm in air around it. After fabrication, the new PCB based laminated bus (shown in Figure 6(b)) is only about 5 mm thick. The multi-layer PCB planar bus has only 12.1 nH power-loop inductance. Insulation tests were performed with same equipment as described before on Figure 5. When measuring between +dc and -dc layers, the PD inception voltage (PDIV) was increased to 11.36 kV, as seen in Figure 6(c). The dc-link capacitors are mounted directly on the bus which, in combination with the low inductance bus, eliminated the need for decoupling capacitors.

Apart from planar PCB-bus for HB-PEBB, developed design procedure can be utilized to develop the converter-level dc-bus, still ensuring low parasitic inductance and high PDIV. However, approach will slightly be changed compared to HB-PEBB dc-bus. Example dc-bus will be constructed based on the 24 kV PCB-based motherboard, where eight 3 kV PCB daughtercards carrying dc-bus capacitance will be inserted in series to achieve desired capacitance and to reach desired voltage[62]. The full bus voltage is split between 9 potentials (including earth GND - 0 V) so that the maximum differential between any two adjacent layers is still 3 kV. To increase flexibility with the converter assembly, the 0 V layers were placed as the outer most planes with the 24 kV layer in the middle. In total, the final board is 22 layers and 10.8 mm thick. Regarding the 3 kV capacitor daughtercards, two 6 μF, 1.5 kV Kemet capacitors were placed in series and three sets in parallel for total of 9 μF. Additionally, surface mount resistors were integrated in each capacitor daughtercard for voltage balancing. Same approach for insulation testing was performed for converter dc-bus assembly (shown in Figure 6(d)), and final PDIV is 27.3 kV. Additionally, a dc hipot test was performed for 1 h at 26.4 kV without any flashovers or breakdown issues.

5 Power-cell integrated magnetics

This section aims to develop a high-power high-density inductor integrated in the HB-PEBB. The specifications were derived from the SCC principle (inductance, rated current, and maximum current).

Generally, the passive components in MV applications have bulky and over-designed insulation[63,64] resulting in large overall size; however, the space for passive components in the HB-PEBB

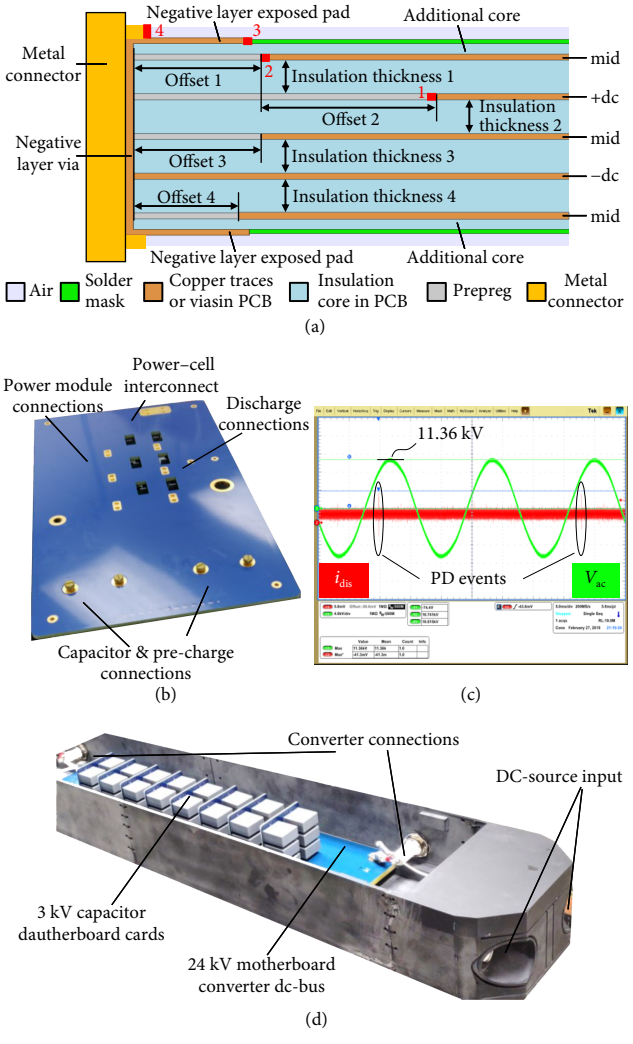

Fig. 6 **(a)** 2D section view of multi-layer PCB bus for MV converters. **(b)** Developed 6 kV PCB-based bus. **(c)** PDIV assessment of PCB-based dc-bus prototype. **(d)** Converter-level PCB-based dc-bus assembly.

is extremely limited due to its high power density requirement. The proposed SCC approach for MMC enables a significant size reduction for passive component[13,20], but a compact and reliable physical design is still in need. The magnetic design for MV applications regarding insulation designs of inductors, transformers, electric machines, and cables has been widely studied over years, proposing many solutions[65–67]. However, combining the magnetic design with insulation design is a comprehensive task for such high density requirement[39,68,69].

The inductor design starts with a comparative study among air-core, single-turn magnetic core and multi-turn magnetic core solutions in terms of volume and power loss, and result shows that the single-turn magnetic core structure is the most suitable solution[70]. After comparing different insulation strategies, the solid insulation with locally grounded shielding layer (HB-PEBB capacitor midpoint) is selected due to its compactness and reliability. Once the general structure was selected, multi-objective optimization (cf. Figure 7(a)) was done to find out the best trade-off in terms of power loss, volume and parasitic capacitance (between the conductor and shield). Figure 7(b) shows the selected structure with optimized dimensions.

The shielding layer facilitates the insulation design, but it brings side-effects (cf. Figure 7(c)), one of which is the loss on the shield

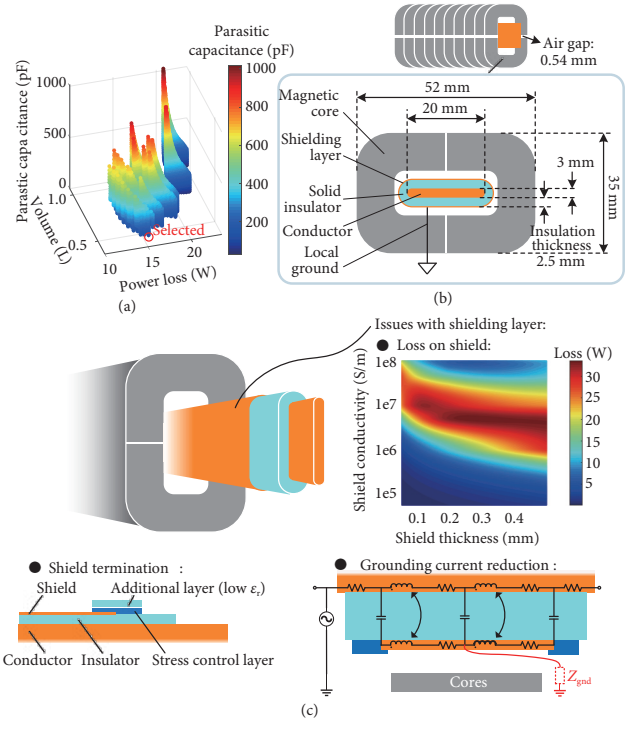

Fig. 7 **(a)** Multi-objective optimization and **(b)** the selected inductor structure. **(c)** Shield overview and its related issues addressed in ref. [70].

due to the leakage magnetic field near the air gap. This loss is a function of frequency, distance to the air gap, shield thickness, and permeability and conductivity of the shield. A conductive shield forms an equipotential surface but has relatively higher loss than a highly resistive shield. A conductive coating material ($\sigma = 4.6 \times 10^5$ S/m) was used and the thickness must be small enough to ensure the loss is acceptable. In addition, the sharp shield fringes would cause equipotential lines to concentrate and result in high electric field in air. The high permittivity material was utilized to cover the shield edges to smooth out the equipotential lines. To further minimize the electric field in air, the double layer termination structure was proposed and studied quantitatively. Finally, a layer with $\varepsilon_r \approx 3.6$ and thickness 1 to 1.5 mm was selected. Another issue is the parasitic capacitance between the conductor and the shield. Displacement current can be induced due to the high dv/dt rate and contributes to the overall CM noise. After evaluating the grounding performance of several configurations (damping resistor with series capacitor), a 50 Ω grounding resistor and a 5 pF capacitor were inserted between shield and local ground (HB-PEBB capacitor midpoint).

Inductor prototypes (Figure 8(a)) were fabricated in lab using resin rich or epoxy encapsulation process. The PDIV is above 7 kV which meets the insulation requirement. To confirm effectiveness of ground network, the prototype was tested with dv/dt up to 98 V/ns. The current through the grounding network and the loss on the damping resistor all increase with dv/dt, and the worst case gives 3 A peak current and less than 0.2 W loss on the damping resistor, as observable from Figure 8.

6 High-speed, High-performance communication network

The high switching frequency and modularity jointly result in a significant challenge to the communication and control systems implemented in modular converters. For these converters, dis-

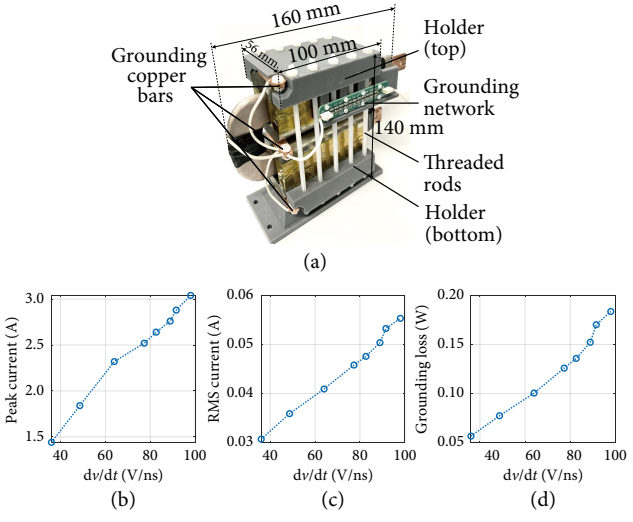

Fig. 8 **(a)** Inductor prototype. **(b)(c)(d)** Test results under various dv/dt values.

tributed control with high scalability is preferred[71]. Emerging large-scale modular converters are pursuing high-performance distributed control systems (DCSs) that feature minimal synchronization accuracy (SA), high data rate, and advanced control schemes[72,73]. State-of-the-art communication networks with high SA are: (1) ±5 ns SA field bus protocol[74], (2) ±4 ns SA Synchronous-Converter-Control-Bus (SyCCo-Bus) based on 1 GBit Ethernet standard[75], (3) ±1.5 ns SA fully customized protocol with RealSync technology[76]. Notwithstanding remarkable SA performance, these communication networks cannot suffice in ICBT converter due to strict requirement for synchronous operation of cells, where several nanosecond mismatch in synchronization can lead to enormous arm current peaks, especially at high voltage. The following discussion presents the effective synchronization techniques that tackle this challenge, particularly the CPES PESNet, which has evolved from its first generation in 1999 to PESNet 3.0 today. PESNet 3.0 achieves a ±0.5 ns SA, 300 ns node-to-node latency, and reinforced resilience with a novel network topology. More details about distribution, control layer partition and its mapping with physical control hardware, synchronization and temporal sequencing can be found in ref. [77].

6.1 Inter-PEBB layer

Power electronics system network (PESNet) 3.0 is a next-generation communication network designed and optimized for DCSs[78]. Accompanied by the growing availability of MV wide-bandgap devices, fast-switching-enabled novel control schemes raise a high SA requirement for PESNet 3.0[15,17]. PESNet 3.0 contains an inter-PEBB layer and an inner-PEBB layer. Custom-made controller supporting PESNet 3.0 is shown in Figure 9(a). The White Rabbit technology, originally developed for the Large Hadron Collider accelerator chain at the European Organization for Nuclear Research[79,80], has been embedded in PESNet 3.0 inter-PEBB layer to achieve a sub-nanosecond (sub-ns) SA for distributed power conversion systems for the first time. PESNet 3.0 inter-PEBB layer contains the main controller and HB-PEBB controllers. They share the same hardware using the high-end Xilinx 7000 as the control device, and are communicated in a tree topology with 5 Gbps data rate. Sub-ns SA is achieved by utilizing a PLL on the controllers to lock both the frequency and phase of the local time with each other.

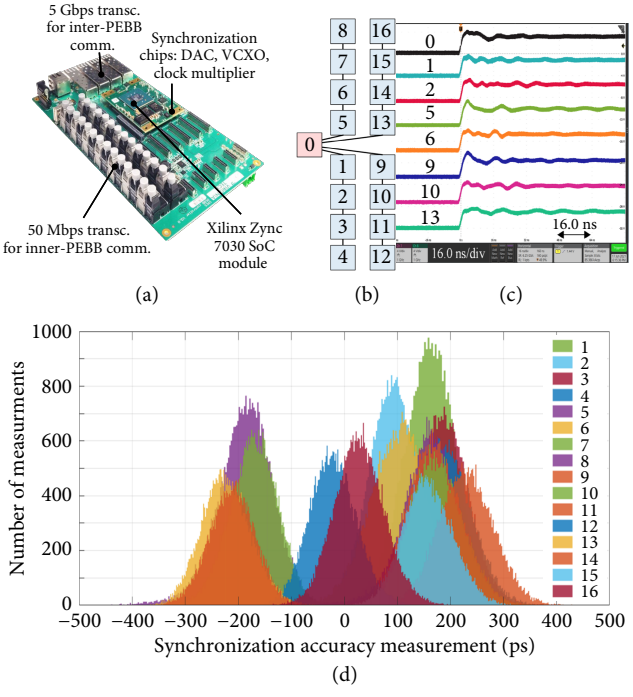

Fig. 9 **(a)** Controller prototype. **(b)** PESNet 3.0 inter-PEBB layer with 17 controllers in a tree topology. Controller 0 is the main, and 1 to 16 are the HB-PEBB controllers. **(c)** Synchronization test waveform for the main and 7 HB-PEBB controllers. This test is repeated with the other 9 HB-PEBB controllers. **(d)** Synchronization accuracy distribution referred to the benchmark main controller for all the 16 HB-PEBB controllers.

To evaluate the PESNet 3.0 inter-PEBB layer synchronization performance, a communication network shown in Figure 9(b) is built. A local time counter is generated based on each controller's own clock. A square wave based on the local time counter is utilized to measure the SA, as shown in Figure 9(c). The channel-to-channel delay measurement data is further extracted from the oscilloscope as shown in Figure 9(d). Setting the main controller as the benchmark, all the measurement data for the 16 HB-PEBB controllers are within ±0.5 ns, which verifies the sub-ns SA.

6.2 Inside-PEBB layer

Apart from communicating with other controllers in inter-PEBB layer, HP-PEBB controller is simultaneously communicating with digital voltage and temperature sensor and two eGDs forming an Inside-PEBB layer, as shown in Figure 10(a). Clock for synchronization purposes is physically distributed between the controller and eGDs using an additional fiber optic transceiver, achieving excellent synchronization using relatively inexpensive communication hardware. Regarding communication protocol, it is heavily influenced by 10BASE-T Ethernet and EtherCAT[81–83]. By reducing minimum payload size (12 octets) and doubling the speed (25 Mbps), the communication is improved in order for required data to be exchanged within one control cycle (switching cycle). Research[73,84] heavily influenced communication and synchronization development as well. Developed communication protocol is utilized for both sending (duty cycle, current reference, dynamic dead-time, phase shift, etc.) and receiving information (current, voltage, temperature, short-circuit faults, communication errors, etc.). To bolster the data transmission between local controller and GD, and prevent data corruption during power-cell switching in-

stances due to high conductive and radiated EMI noise caused by high dv/dt and di/dt, data packets transmission pauses during the switching transitions (implemented pauses are ≈ 2 μs).

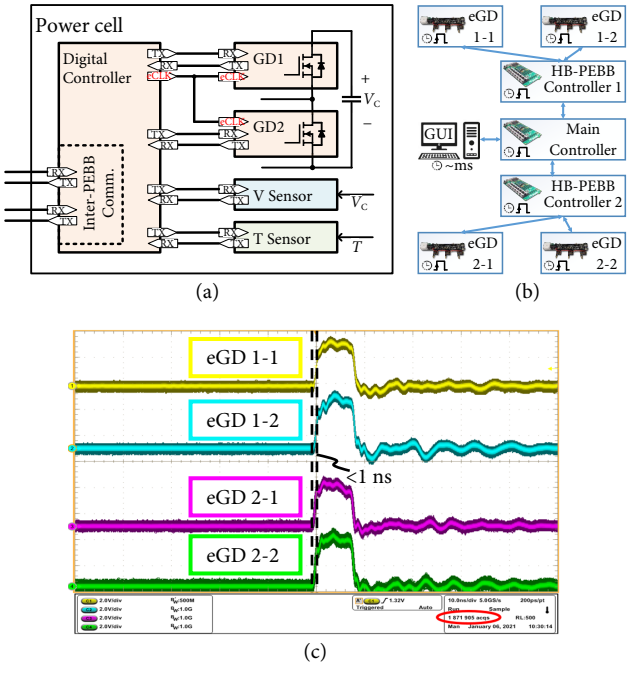

Fig. 10 **(a)** Inside-PEBB communication layer. **(b)** Testbed for synchronization verification. **(c)** Synchronization test waveform for four eGDs.

To verify communication and synchronization, a testbed, shown in Figure 10(b), is built consisting of main controller communicating with two HB-PEBB controllers, and each is communicating with two eGDs. The eGD's task is to generate synchronization pulse at a defining moment if communication and synchronization is successful. Figure 10(c) shows that synchronization pulses are within ±1 ns, which further verifies the sub-ns SA. Consequently, all actions at any moment will happen synchronously across all communication network.

7 High-bandwidth control

7.1 Switching-cycle control (SCC)

To possibly overcome MMC conventional control drawbacks of large capacitor voltage ripple, existing attenuation approaches such as the second order or high-frequency harmonic injections are designed based on average models limiting the achievable performance[85,86]. The proposed switching-cycle control (SCC)[15] aims to greatly increase the control time resolution and form the control in the timescale of a switching-cycle. This critical alternation equips the MMC with the capability to achieve voltage balancing in a single switching-cycle, shifting the MMC from a long-deemed ' line-cycle balancing' converter to a ' switching-cycle balancing' converter.

The key reason for the large capacitor voltage deviation in the conventional control is that the arm currents have the same value in one switching period, accumulating voltage deviations in the same direction. To prevent this, it is necessary to meaningfully reassign arm currents within one switching period instead of keeping the same value. With that, the capacitor voltages can be balanced in a single switching period with the derived arm current patterns, preventing capacitor voltage deviations, as shown in Figure 11 for two-cell-per-arm converter. To achieve this arm current pattern, the switching actions between the upper and lower arm cells are not complimentary as in the conventional control. Instead, a delay is applied on cell output voltages to create 'shoot-through' periods inducing high di/dt, instantly shaping the arm current. By adjusting the duration of the 'shoot-through' periods, arm currents can be arbitrarily shaped. Current boundaries can be derived from closed loop control based on phase current and capacitor voltage disbalance. Peak current mode (PCM) modulation is used to determine the duration of the shoot-through periods. It is worth mentioning that due to the inserted 'shoot-through' periods, an additional voltage level is observed on the output voltage. In contrast to the conventional control, since there is no capacitor voltage deviation by the end of the switching period, this makes the dc-dc operation of the MMC possible. Furthermore, due to the zero-voltage switching the turn-on loss is nearly eliminated, reducing the total losses compared to the classic control methodologies. More details about the control can be found in ref. [15].

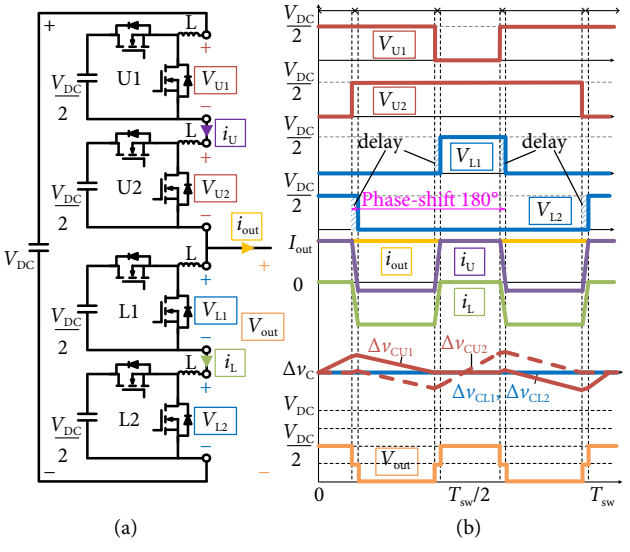

Fig. 11 **(a)** Two-cell-per-arm SCC configuration. **(b)** Representative waveforms for duty cycle of D = 0.25.

7.2 Integrated capacitor-blocked transistor (ICBT)

ICBT converter[16] provides another solution to achieve modular MV converters with high power density. An ICBT-based converter arm consists of multiple series-connected ICBT cells, also similar as a converter arm in MMCs, except that the arm inductor is eliminated. ICBT-based converters have the modularity and scalability features like MMCs. Configuration of an ICBT cell is same as the HB-PEBB of MMCs proposed in Figure 1, except the inductor will be bypassed.

Unlike the control for MMCs, the ICBT-based converters have simple control principle. The HB-PEBBs in the same arm operate synchronously and the HB-PEBBs in the opposite arms operate complementary. As shown in Figure 12(a) for two-cell-per-arm configuration, when the bottom switch is on, the HB-PEBB is in the on-state, and can conduct a bidirectional current. When the top switch is on, the HB-PEBB capacitor is connected in series with the other HB-PEBB capacitors in the same arm, and together to the converter dc bus. Due to only parasitic inductance in the arm, the arm current reduces rapidly to zero and the cells block the converter dc-bus voltage, as shown in Figure 12(b). This is the

off-state of the HB-PEBB and consecutively converter arm. As a result of low HB-PEBB capacitor currents, HB-PEBB capacitor voltages have low ripples, largely reducing the requirement of capacitances, in both dc and ac applications.

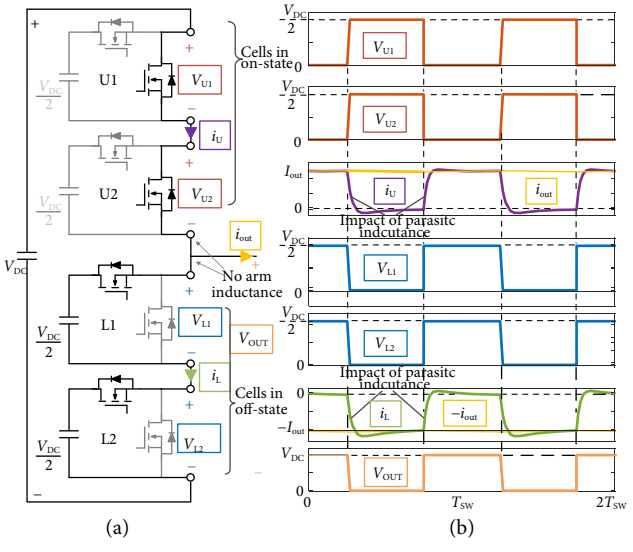

Fig. 12 **(a)** Two-cell-per-arm ICBT configuration. **(b)** Representative waveforms.

The capacitor voltage balance is critical, ensuring the safe operation of all switching devices and HB-PEBB capacitors. Existence of parasitic capacitance between device terminals and the corresponding heatsinks can compromise the HB-PEBB voltage balance[18]. During the fast switching transients, the parasitic capacitors are subjected to fast voltage change, resulting in charging or discharging currents through them. Although the magnitudes of those currents are small, they cause the HB-PEBBs with synchronous control signals to operate with different switching speeds, leading to capacitor voltage difference. The voltage difference develops slowly but will accumulate over time and thus have to be controlled. The HB-PEBB capacitor voltage control[17] can be achieved by applying delays to gate signals to some of the series-connected ICBT cells, forcing different cell capacitor currents for short periods of time during switching transitions. The closed-loop control requires sensing of cell capacitors and phase leg output current.

8 Converter-level verification

After validation of the constitutive parts, HB-PEBB is assembled and the prototype is shown in Figure 13. Based on the dimensions and the maximum input values, power density is 11.9 kW/L (195 W/in3). Systematic assessment methodology of the developed HB-PEBB is presented in refs. [42, 87]. The PD-free operation for both internal and external insulation systems of the HB-PEBB are confirmed at 6 kV differential-mode voltage, and maintains PD-free condition until 33.2 kV common-mode voltage. Given that, 4 of these HB-PEBB units can safely be put in series without PD or insulation breakdowns between earth potential cabinet and HB-PEBB on high voltage. Additional research about utilization of heatsink guard rings to maintain PD-free operation meanwhile increasing power density is described in ref. [88]. The HB-PEBB achieved measured peak efficiency of $\eta = 99.6\%$ @ 5 kHz and $\eta = 99.3\%$ @ 10 kHz. The power cell successfully operated at $V_{dc} = 6$ kV, $I = 84$ A, $f_{sw} \geq 5$ kHz, $T_j \leq 150$ °C, in both dc-dc and dc-ac mode, and had high switching speeds up to 100 V/ns, exhibiting excellent CMTI.

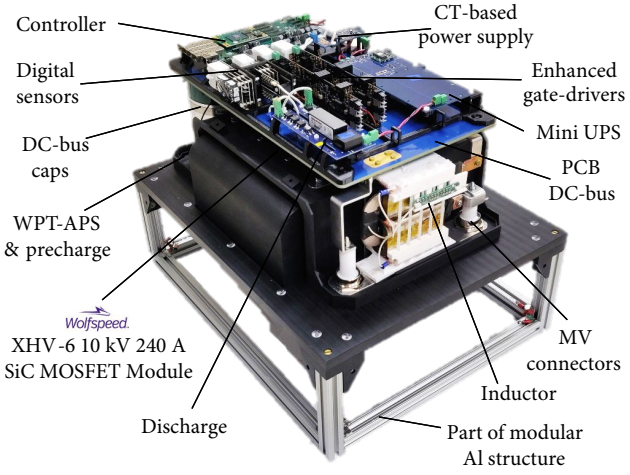

Fig. 13 **10 kV SiC MOSFET-based power-cell with indicated constitutive parts outside enclosure.**

Two-cell-per-arm, modular, scalable converter prototype is custom-built to validate proposed control methodologies at MV. Schematic of the setup and prototype is shown on Figure 14. Described distributed control system is adopted. Each HB-PEBB contains a designated controller, which are connected in a tree topology with one primary main controller and 8 secondary controllers. Experimental setup is capable of operating at maximum 12 kV dc-bus. Two phase legs will be operated in a pumpback configuration to relax the required active power drawn from the dc source[42]. The arm inductance is designed as 160 μH. Unlike for the SCC, arm inductor components are not required in ICBT based converters, and will be bypassed. In that case remaining arm inductance will be parasitic from HB-PEBBs and dc-bus interconnections, which is estimated to be around $L_{para} = 2$ μH per converter arm. Through aid of simulation, cell capacitance is selected to be 32.5 μF. Even with capacitance this small, the SCC balancing only exhibits a 1% voltage ripple, and the ripple is completely independent of the output frequency. If the same capacitance were to be used for conventional MMC control, the capacitor voltage ripple would be 26.5% at 50 Hz and 66% at 20 Hz, which is clearly too large for a safe operation. Key specifications are summarized in Table 3. Due to load and arminductance limit-

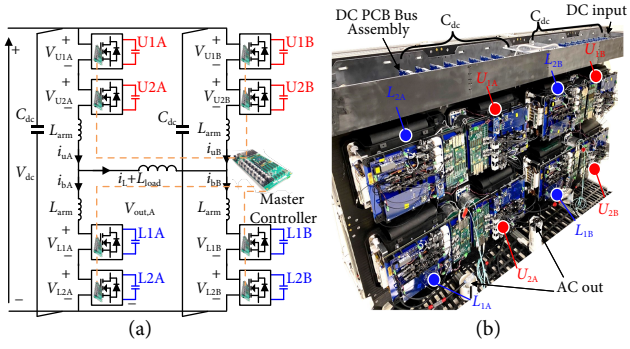

Fig. 14 **(a)** The modular converter pump-back test configuration schematic diagram. **(b)** Prototype of 10 kV SiC MOSFET-based two-cell-per-arm converter in pump-back test configuration.

Table 3 Parameters of the MV converter in pumpback

Parameter	Symbol	Value
Cell capacitance	C_{cell}	32.5 μF
DC-link capacitance	C_{dc}	2.2 μF
DC-link voltage	V_{dc}	12 kV
Arm inductance	$L_{arm,scc}$; $L_{para,icbt}$	160 μH; 2 μH
Load inductance	L_{load}	3 mH
Switching frequency	F_{sw}	10 kHz
Ambient temperature	T_a	23 °C

ations, for now setup can only be tested up to 28 Arms. Converter continuous operation will be demonstrated in the ICBT dc-ac conversion mode, and in the SCC dc-dc conversion mode.

Inherent attribute of novel converter to operate at zero Hz line output frequency can potentially be highly desired operation mode in applications such as MVDC shipboard distribution and dc microgrids which previously was unattainable with conventional MMC. Dc-dc SCC operation mode is shown in Figure 15(a), at 12 kV dc-link voltage with $V_{out} = 6$ kV ($D = 0.5$) and $i_L = 24$ A verifying the converter operation at rated voltage for two-cell-per-arm. According to theoretical analysis presented in ref. [15], for duty cycles between 0.375 and 0.625, 90° carrier phase-shift is used (alternating every 10 switching cycles between 90° and 270°) to prevent cell voltage diverging, and the test results also corroborate with the theoretical waveform. Additionally, Figure 15(b) shows very well balanced HB-PEBBs of the phase legs A, with differences of around 200 V, which is superb considering that each HB-PEBB has only 32.5 μF capacitance. Voltage balancing data is collected through the developed digital sensors which send the data to GUI through communication network. Since pump-back testing approach is utilized, efficiency can be measured with high accuracy. Even though it is zero voltage switching topology, efficiency is not as high as expected and it is measured to be $\eta = 98.65\%$, due to excessive losses in arm inductors. Inductor losses being higher than originally estimated is due to increased core losses, since inductor value had to be increased from original design values of only $L_{arm,scc} = 4$ μH to $L_{arm,scc} = 160$ μH. Reason for this increase is due to existence of delays in GD integrated RSCS and driving network ($T_{dly} \approx 250$ ns) combined with the high di/dt, which hindered peak-current-mode control accuracy. In the next iterations of converter and GD design, sensing and driving delays should be reduced as much as possible, and these delays should as well be taken into account when designing a power-cell inductor. Due to multilevel output voltage, total harmonic distortion (THD) is favorable compared to ICBT and dv/dt will be smaller. Maximum output voltage dv/dt in SCC is 40 V/ns.

ICBT testing results at 60 Hz line frequency under 12 kV dc-link with output current reference of $i_L = 26$ A are shown in Figure 16(a), demonstrating successful operation at rated voltage for two-cell-per-arm. Regarding voltage balancing in this case, shown in Figure 16(b), HB-PEBBs are extremely well balanced exhibiting only minor ripple of ≤ 40 V. All tests results in ICBT have a good agreement with the theoretical waveforms. Additionally, during zero-crossing of the current, minimal spikes in phase leg A arm currents are observed showing that sub-ns SA between the cells is achieved. The distributed communication network PESNet 3.0 with sub-ns SA is thus successfully demonstrated on the modular converter. Efficiency in ICBT configuration at shown conditions is measured to be $\eta = 99.2\%$, surpassing SCC. Major concern for ICBT is regarding the extremely high output voltage dv/dt that can impact adversely insulation of inverter-driven ac machines and accelerate its degradation. Since ICBT is basically 2 level converter, output HB-PEBB voltages are added together, resulting in maximum dv/dt to reach almost 200 V/ns (4–5 times higher than in SCC), which will continue to increase with adding more cells. If for ICBT converter high output voltage dv/dt is potentially detrimental in certain applications, it is of utmost importance to maintain the dv/dt below recommended values. One way to reduce the converter output voltage is by reducing the device dv/dt through increase of the resistance of the gate loop. However, a higher value of resistance increases switching losses of the semiconductor, thus

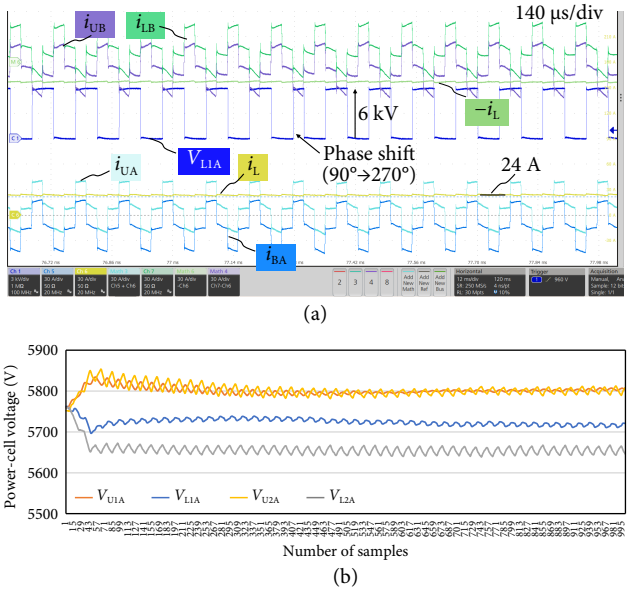

Fig. 15 SCC dc-dc operation mode at $V_{dc} = 12$ kV and $i_L = 24$ A at $D = 0.5$, phase shift (PH) = 90° and PH = 270°: (a) waveforms, **(b)** power-cell voltages collected through communication network.

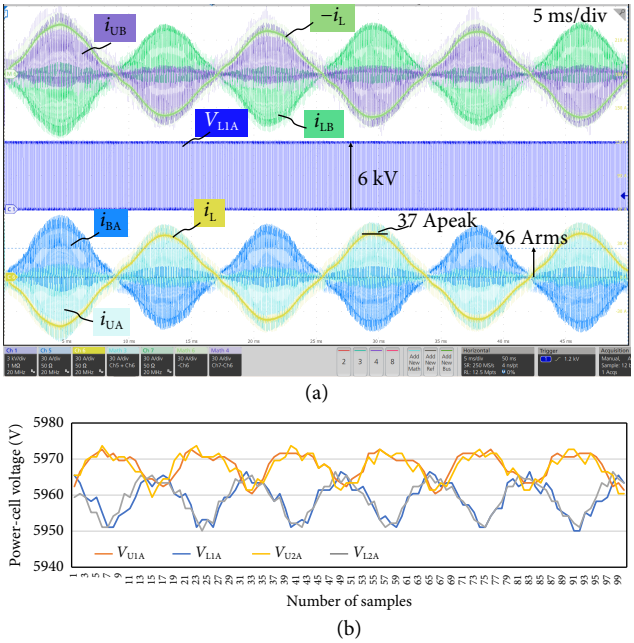

Fig. 16 (a) ICBT dc-ac operation mode having 12 kV dc-link with variable duty cycle, $i_L = 26$ A. **(b)** Power-cell voltages collected through communication network and displayed on GUI.

sacrificing the efficiency[89]. Different passive and active methods of increasing the Miller capacitor value or injecting additional current through it can be used as well[90–92], however they share a similar problem in reducing the efficiency. Another dv/dt control method adds RC snubbers in parallel to the switches for both high side and low side[90], with penalty of increased losses in snubber and device. Additionally, controlling the dv/dt could potentially be solved with using different converter-level dv/dt filtering techniques. Even though filtering techniques do not have an impact on the switching losses on the device, they will introduce additional loss in the filters, increase the cost of the system, and reduce power-density[89,93].

9 Conclusions

Medium-voltage (MV) applications such as grid-tied inverters, dc-dc converters for MVDC microgrids, and motor drives would immensely benefit from high-efficiency, high-density, and high-frequency converter. This paper presents summary of unique key technological solutions to enable 10 kV SiC MOSFET-based modular MV power conversion. Novel technologies such as high-performance enhanced gate-driver maximizing the utilization of SiC MOSFET characteristics, auxiliary power supply network having wireless power transfer as a centerpiece minimizing common-mode current propagation, high-voltage printed circuit board (PCB) planar dc-bus with minimized loop inductances and weight, and high-density integrated power-cell magnetics are presented. At the core of the proposed approach and innovation, are the switching-cycle control (SCC), integrated capacitor-blocked transistor (ICBT) converter control, and required high-performance/high-bandwidth communication network with synchronization accuracy of < 1 ns enabling proposed controls. All technologies are combined in 6 kV SiC-based power-cell with power-density of 11.9 kW/L and $\eta = 99.3\%$ (@ 10 kHz, 6 kV, 84 A) which is finally embedded in the 12 kV modular MV converter prototype. Converter operates successfully in both SCC and ICBT in dc-dc and dc-ac mode without necessity for outside passives, having switching speeds (up to 100 V/ns per power-cell) and high-switching frequency (10 kHz), meanwhile exhibiting high common-mode transient immunity and high-efficiency ($\eta_{ICBT} = 99.2\%$ and $\eta_{SCC} = 98.65\%$). Converter designed in this way successfully overcomes challenges of high-voltage insulation, high dv/dt and electromagnetic interference (EMI), and high-switching frequency, providing the system with benefits of high power density, high-efficiency, fast dynamic response, unrestricted line frequency operation, and improved power quality. Developed hardware and software technologies are not strictly limited to modular converters and can be broadly utilized for MV converters.

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Additional information

Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

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