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Analysis and synchronization controller design of dual-port grid-forming voltage-source converters for different operation modes

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ABSTRACT

Grid-tie voltage source converters (VSCs) can operate in three distinct modes: AC-dominant, DC-dominant, and balanced, depending on the placement of the stiff voltage sources. The distinct operation modes of the VSCs traditionally demand different synchronization control techniques, leading to heterogeneous VSCs. It is challenging for the power system to accommodate and coordinate heterogeneous VSCs. A promising universal synchronization control technique for VSCs is the DC-link voltage synchronization control (DVSC) based on a lead compensator (LC). The LC DVSC stabilizes both the DC and AC voltages of a VSC while achieving synchronization with the AC grid. This results in a dual-port grid-forming (DGFM) characteristic for the VSC. However, there has been very limited study on the stability and synchronization controller design of the VSCs with the LC DVSC operating in various modes. To bridge this gap, the paper presents a quantitative analysis on the stability and steady-state performance of the LC DVSC in all three operation modes of the DGFM VSC. Based on the analysis, the paper provides step-by-step design guidelines for the LC DVSC. Furthermore, the paper uncovers an instability issue related to the LC DVSC when the DGFM VSC operates in the balanced mode. To tackle the instability issue, a virtual resistance control is proposed and integrated with the LC DVSC. Simulation results validate the analysis and demonstrate the effectiveness of the DGFM VSC with the LC DVSC designed using the proposed guidelines in all three operation modes. Overall, the paper demonstrates the feasibility of employing the DGFM VSC with the LC DVSC for all three possible operation modes, which can help overcome the challenges associated with accommodating and coordinating heterogeneous VSCs in the power system.

KEYWORDS

DC-link voltage synchronization control (DVSC), dual-port grid-forming (DGFM) control, grid forming (GFM), synchronization stability, voltage-source converter (VSC).

The modern power system is envisioned to integrate more and more voltage source converters (VSCs) to provide various critical services[1–6]. As illustrated in Figure 1, a grid-tie VSC can operate in an AC-dominant, a DC-dominant, or a balanced mode when an external stiff voltage source is applied on the AC bus, DC bus, or both, respectively[4,5]. A voltage source is defined to be "stiff" when it has a low series impedance internally, meaning that when the current flowing into or out of it changes, the voltage will change very little[4]. In the AC-dominant mode, the VSC must impose a stiff DC voltage for the devices connected to the DC bus. This operation mode is frequently employed for integrating renewable generation into an AC power grid[6,7]. In the DC-dominant mode, the VSC must maintain a stiff AC voltage that can be used as a reference voltage for the devices connected to the AC bus. A common application is using the VSC to impose a stiff AC grid voltage in offshore wind farm clusters for exporting the generated power, which is typically transmitted to the mainland grid through high-voltage direct-current (HVDC) transmission[2]. In the balanced mode, VSCs serve as interlinking converters that link a stiff DC voltage and a stiff AC voltage to provide mutual power support[3–5].

Traditionally, different operation modes of grid-tie VSCs require different synchronization control techniques to fulfill their functions. Two prevailing grid synchronization techniques have been extensively researched[7]:

(1) AC-voltage-based synchronization control. Also known as grid-following (GFL) control, this method employs a phase-locked loop (PLL) to track the AC grid phase and frequency[7,8]. Consequently, the GFL control is not applicable in the DC-dominant mode.

(2) Power-based synchronization control (PSC). It generates the operating frequency and phase of the VSC based on an active power-frequency droop control with certain modifications, also known as grid-forming (GFM) control[7]. The prevalent methods in this category include power synchronization control[1], (inertial) droop control[9], virtual synchronous generator control[10], and dispatchable virtual oscillator control[11]. However, the GFM control necessitates the VSC to be connected to a stiff DC voltage source, making it unsuitable for operating in the AC-dominant mode.

In modern power systems, the VSCs are anticipated to function in different modes to accommodate different applications. However, neither GFM control nor GFL control can serve as a universal synchronization control technique for VSCs to operate in all of the three modes. While the combination of the GFL VSCs and the GFM VSCs can handle different applications that require the VSCs to operate in all of the three modes, effectively accommodating and coordinating the heterogeneous GFL and GFM VSCs remains challenges for power systems[12]. To address these challenges, a universal synchronization control technique for VSCs to operate in all of the three modes is desirable, which motivated the development of the following third category of synchronization control methods.

(3) DC-link voltage synchronization control (DVSC). Uniquely integrating DC-link voltage control (DVC) with AC synchro-

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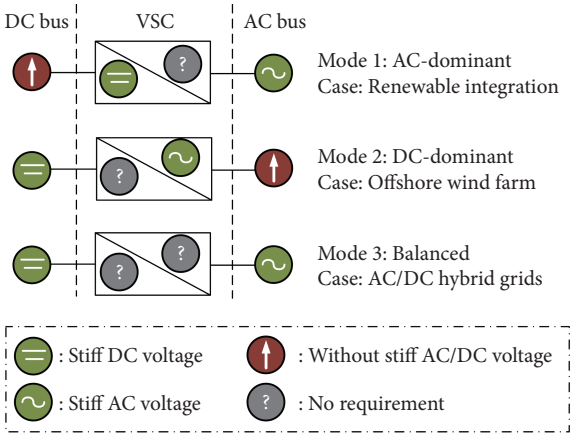

Figure 1 Operation modes of a grid-tie VSC with typical application cases.

nization control, the DVSC can effectively stabilize both DC- and AC-side voltages of the VSC simultaneously[5,13–25]. This exceptional feature grants the VSC a dual-port grid-forming (DGFM) terminal characteristic, making the VSC possibly operate in any of the three modes[21,22]. A conventional type of DVSC is formed by cascading or paralleling a proportional-integral (PI) DVC with a PSC[23–25], called PI+PSC DVSC. Another type of DVSC directly processes the DC voltage error using a proportional regulator[5,13], a low-pass filter (LPF)[14], a proportional-derivative (PD) regulator[15], or a lead compensator (LC)[16–20]. The DVSC with either a proportional regulator, an LPF, or a PD regulator can be viewed as a special case of the LC DVSC. As pointed out in Refs. [25] and [26], the proportional DVSC and the LPF-based DVSC exhibit instability issues when the DC-bus of the VSC only contains a constant power source or load. In Ref. [26], a small-signal-model-based comparison between the PI+PSC DVSC and the LC DVSC reveals that the LC DVSC features a simpler control structure. When using the LC DVSC, the DVC loop and synchronization control loop are integrated into a single control loop, while the PFF of the PI+PFF DVSC separates the DVC and the synchronization control into two distinct control loops[26].

However, the existing research on the LC DVSC has focused solely on the operation of VSCs in the AC-dominant mode, and none of these studies has offered a quantitative analysis on the synchronization stability or provided rigorous guidelines for the parameter design of the LC DVSC, while considering the effects of external disturbances[16–20]. Moreover, the potential applications of the DGFM VSC with the LC DVSC in the three operation modes are still underexplored, and the feasibility of operating the DGFM VSC with the LC DVSC in the DC-dominant mode and the balanced mode is yet to be demonstrated.

To address the research gaps, this paper provides a quantitative analysis of the stability and steady-state performance of the LC DVSC, considering the impact of external disturbances in the three operation modes, respectively. Based on the analysis, design guidelines for the LC DVSC are provided for the DGFM VSC in each of the three operation modes. Moreover, the paper uncovers a potential instability issue with the LC DVSC when the DGFM VSC operates in the balanced mode. To solve the problem, a virtual resistance (VR) control is proposed and integrated with the LC DVSC to not only enhance the system stability but also play a crucial role in regulating the output power of the VSC in the balanced mode.

The remainder of the paper is organized as follows. In Section 1, the system setup and modeling preparation for the DGFM VSC with the LC DVSC is outlined, including the system configuration, essential assumptions for modeling the system, and the shared small-signal power dynamics modeling among the three operation modes. Sections 2, 3, and 4 analyze the stability and steady-state performance of the LC DVSC in the AC-dominant, DC-dominant, and balanced modes, followed by the design guidelines for the LC DVSC, respectively. Simulation results are provided in Section 5. Section 6 presents concluding remarks.

1 System setup and modeling preparation

This section describes the system configuration of the DGFM VSC with the LC DVSC, applicable to all three operation modes, followed by three assumptions to simplify the modeling process and the shared small-signal models of the DC-link and AC-bus power dynamics of the DGFM VSC in the three operation modes.

1.1 System configuration

The single-line diagram of a three-phase DGFM VSC is illustrated in Figure 2. The power stage of the system includes a three-phase VSC, a lumped DC-link capacitor C_d, and an inductor-capacitor filter. The power transferred from the DC bus to the DC link of the VSC power stage, named DC bus power hereafter, is represented as P_{dc}. Similarly, the power flowing from the point of common coupling (PCC) into the AC bus, named as AC-bus power hereafter, is denoted as P_{ac}. Additionally, the AC bus, which is represented by an AC source cascaded with an equivalent line inductance L_g and resistance R_g, is connected to the PCC of the VSC power stage. The AC-bus voltage is denoted as v_{gabc}, with its angular frequency represented as ω_g. The controller of the VSC samples the DC-link voltage v_{dc}, the current through the filtering inductor i_{fabc}, the PCC voltage v_{abc}, and the current from the VSC power stage to the AC bus i_{gabc}. The LC DVSC consists of a PD regulator and an LPF. The angular frequency of the PCC voltage ω is generated by the LC DVSC[16–20] as

$$\omega = \omega_{ref} + (K_p + sK_d) \cdot \frac{\omega_c}{s+\omega_c} \cdot (v_{dc} - V_{dcref}) \tag{1}$$

where ω_{ref} denotes the nominal angular frequency of the AC-bus voltage; K_p and K_d denote the proportional and derivative gains, respectively; ω_c is the cutoff frequency of the LPF; and V_{dcref} denotes the reference DC-link voltage.

The LC DVSC produces the angular frequency ω and phase θ required for the amplitude-invariant Park and reverse Park transformations. Given that the paper focuses on the examination of the synchronization control loop, which is typically associated with the active power and DC-link voltage, the study omits the reactive power control from the VSC controller. Therefore, the d-axis reference voltage V_{dref} is set to the amplitude of rated AC-bus phase-ground voltage V_m, while the q-axis reference voltage V_{qref} is set to 0. Consequently, the amplitude of the PCC voltage is maintained as a constant V_m, achieved through the inner PCC voltage and current control loops.

1.2 Model assumptions

To gain a better understanding of the primary behavior of a system, certain small yet intricate phenomena within the system can be disregarded using assumptions. The assumptions employed to simplify the modeling process of the system in Figure 2 are outlined below.

Assumption 1: The losses of the DGFM VSC power stage are neglected, implying that the power flowing from the DC link into

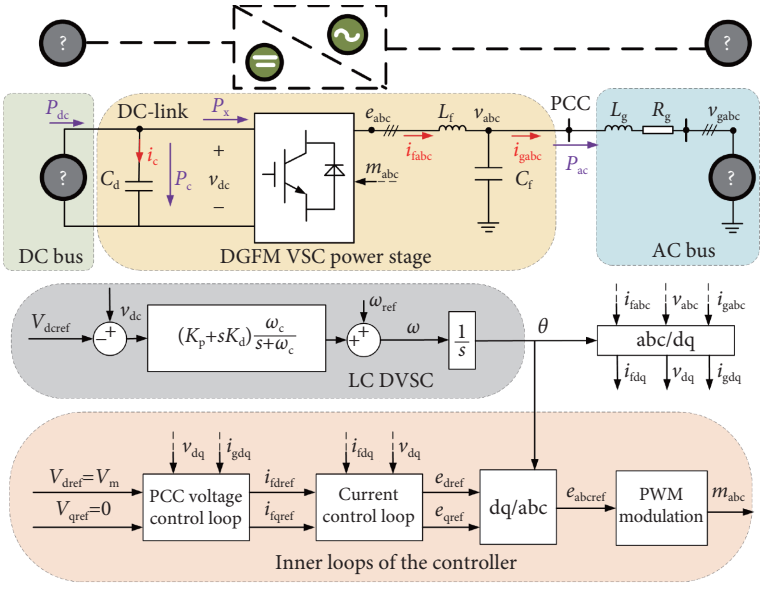

Figure 2 Single-line diagram of a three-phase DGFM VSC with the LC DVSC operating in any of the three operation modes.

the VSC power modules, P_x, is assumed to be equal to the power flowing from the PCC into the AC bus P_{ac}.

Assumption 2: Assuming that the dynamics of the inner loops of the VSC controller are much faster than that of the outer-loop LC DVSC, the gain of the inner PCC voltage and current loops can be regarded as 1 with a zero phase delay.

Assumption 3: Assuming that the AC-bus line reactance $X_g = \omega_g L_g$ is much greater than the line resistance R_g and disregarding the dynamics of the power flow through the line connected to the AC bus, the AC-bus power can be approximated as[9,17,19,26]

$$P_{ac} = \frac{3}{2}\frac{V_m V_g}{X_g}\sin\delta = P_{max}\sin\delta \tag{2}$$

where V_g represents the amplitude of the AC-bus voltage v_{gabc}, δ signifies the phase difference between the PCC voltage v_{abc} and the AC-bus voltage v_{gabc}, and $P_{max} = 3V_m V_g/(2X_g)$ denotes the maximum capacity of active power delivery, which can be treated as a constant by assuming V_g and V_m are constant.

Overall, the Assumptions 1–3 can considerably simplify the analysis of the dominant dynamics of the system.

1.3 Small-signal models of DC-link and AC-bus power dynamics

By employing Assumption 1, the power dynamics of the lumped DC-link capacitor follows

$$P_{dc} - P_{ac} \approx P_{dc} - P_x = P_c = v_{dc} i_c \tag{3}$$

where P_c denotes the power absorbed by the DC-link capacitor, and i_c denotes the capacitor charging current.

Then, the small-signal expression of Eq. (3) is derived as

$$\begin{aligned}\Delta P_{dc} - \Delta P_{ac} &= \Delta v_{dc} I_c + V_{dc}\Delta i_c \\ &= \Delta v_{dc} I_c + V_{dc}\left(s \cdot C_d \Delta v_{dc}\right) = s V_{dc} C_d \Delta v_{dc}\end{aligned} \tag{4}$$

where the small-signal variables are denoted by the symbol "Δ" in front; I_c denotes the steady-state value of capacitor charging current that should be 0; and V_{dc} denotes the steady-state value of DC-link voltage.

Referring to Eq. (2), the small-signal dynamics of the AC-bus power can be derived as follows by utilizing Assumption 3.

$$\Delta P_{ac} = P_{max}\cos(\delta_0)\Delta\delta \approx P_{max}\Delta\delta \tag{5}$$

where δ_0 signifies the steady-state value of the phase difference between the AC-bus voltage v_{gabc} and the PCC voltage v_{abc}. A step-by-step derivation of the small-signal dynamics of the power flow through the line connected to the AC bus is provided in the Appendix, accompanied by an assessment of the impact of Assumption 3.

The phase angle difference $\Delta\delta$ in Eq. (5) can be calculated by

$$\Delta\delta = (\Delta\omega - \Delta\omega_g)/s \tag{6}$$

In summary, the small-signal model of the DC-link power dynamics is derived as Eq. (4), and the small-signal model of the AC-bus power dynamics is derived as Eq. (5) and Eq. (6). These models are universally applicable for the DGFM VSC operating in any of the three modes.

2 DGFM VSC operating in AC-dominant mode

This section first presents the application scenarios of the DGFM VSC operating in the AC-dominant mode. Then, the small-signal model of the synchronization control loop is established, followed by an analysis of the synchronization stability, disturbance rejection, and steady-state performance of the LC DVSC. Based on the analysis, step-by-step design guidelines for the LC DVSC are presented.

2.1 Application scenarios and modeling of DC-bus power

According to the type of the device connected to the DC bus, there are primarily four application scenarios of the DGFM VSC operating in the AC-dominant mode, which are depicted in Figure 3. In the first scenario, an adjustable AC source (e.g., wind turbine) or load (e.g., AC motor drive) is connected to the DC bus through an AC/DC converter to supply or draw active power to or from the DC link of the VSC power stage, respectively. This AC/DC converter regulates the active power of the AC source or load but relies on the DGFM VSC to stabilize the DC-bus voltage. In the second scenario, an adjustable DC source (e.g., PV panels) or load is connected to the DC bus via a DC/DC converter to supply or draw power to or from the DC link of the VSC power

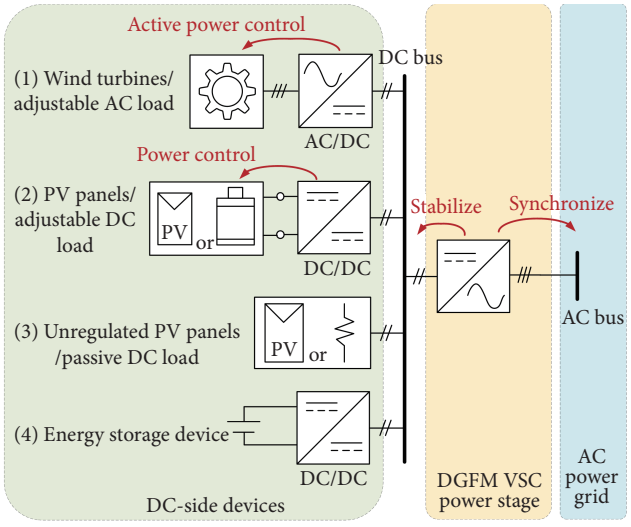

Figure 3 Application scenarios of the DGFM VSC operating in AC-dominant mode.

stage, respectively. This DC/DC converter regulates the power generated by the DC source or consumed by the DC load but depends on the DGFM VSC to ensure the stability of the DC-bus voltage. In the third scenario, a DC source (e.g., PV panels) or passive DC load directly provides or consumes unregulated power to or from the DC link of the VSC power stage, respectively. In the fourth scenario, an energy storage device (ESD), such as battery packs, is connected to the DC bus via a bidirectional DC/DC converter, which can utilize a P_{dc}/v_{dc} droop control to support the DC-bus voltage[14], whose effects will be discussed later. It should be noted that a DGFM VSC can be used in a single application scenario or multiple application scenarios simultaneously. Furthermore, the DGFM VSC with the LC DVSC can seamlessly transition between the GFM inverter mode and the GFM rectifier mode, which is also known as GFM load mode[27].

In the AC-dominant mode, the DC bus of the DGFM VSC is modeled as a current source with an output power P_{dc}, and the AC bus is modeled as an AC voltage source with a line impedance, as shown in Figure 4. The DC-bus power P_{dc} may contain one or multiple of the three distinct components according to the power of the devices connected to the DC bus in different application scenarios: a regulated constant power P_{dc1} ($\Delta P_{dc1} = 0$) in the application scenarios 1 and 2, an unregulated power P_{dc2} in the third application scenario, and a regulated droop power P_{dc3} in the fourth application scenario and possibly in the application scenarios 1 and 2, which is controlled as[14]

$$P_{dc3} - P_{dc3ref} = k_{dc}\left(V_{dcref} - v_{dc}\right) \tag{7}$$

where P_{dc3ref} denotes the nominal power exchanged between the ESD and the DC bus, and k_{dc} denotes the P_{dc3}/V_{dc} droop gain.

Then, the small-signal expression of ΔP_{dc} can be derived by

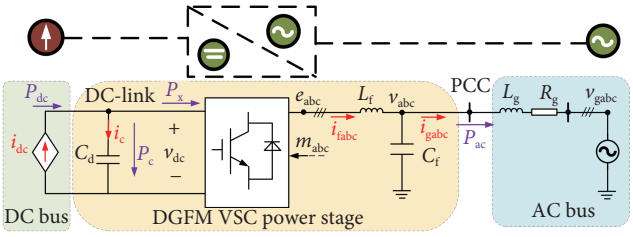

Figure 4 DGFM VSC operating in AC-dominant mode where the LC DVSC is the same as that in Figure 2 and, thus, is omitted.

considering the three components in a unified manner:

$$\begin{aligned}\Delta P_{dc} &= \Delta P_{dc1} + \Delta P_{dc2} + \Delta P_{dc3} \\ &= \underbrace{\Delta P_{dc2}}_{\text{unregulated}} + \underbrace{\left(-k_{dc}\Delta v_{dc}\right)}_{\text{droop}}\end{aligned} \tag{8}$$

2.2 Stability analysis in AC-dominant mode

For simplicity, by disregarding changes in inner references ΔV_{dcref} and $\Delta\omega_{ref}$ of the controller, the small-signal model of the synchronization control loop can be deduced and depicted in Figure 5, where the open-loop transfer function $G_{ol}(s)$ from $\Delta\omega_g$ to $\Delta\omega$ without the feedback loop is derived as follows:

$$G_{ol}(s) = G_1(s)\,G_2(s) = \frac{P_{max}\omega_c}{\left(C_d V_{dc} s + k_{dc}\right)} \cdot \frac{K_p + sK_d}{s\left(s+\omega_c\right)} \tag{9}$$

where

$$\begin{cases} G_1(s) = \dfrac{P_{max}}{s} \\ G_2(s) = \dfrac{\omega_c}{\left(C_d V_{dc} s + k_{dc}\right)} \cdot \dfrac{K_p + sK_d}{\left(s+\omega_c\right)} \end{cases} \tag{10}$$

In the case of $k_{dc} = 0$, the open-loop transfer function $G_{ol}(s)$ in Eq. (9) shows three poles and one zero, where two poles $\omega_{p1} = \omega_{p2} = 0$ are inherently included in the AC-bus model and the DC-bus model, respectively; the third pole $\omega_{p3} = -\omega_c$ and the zero $\omega_z = -K_p/K_d$ are dominated by the parameters of the LC DVSC. In this case, the open-loop transfer function $G_{ol}(s)$ closely resembles that of a node-to-node PLL in Ref. [28]. To have a positive phase margin, the necessary stability condition has been demonstrated to be $|\omega_z| < |\omega_{p3}|$[28], or written as

$$K_p / K_d < \omega_c \tag{11}$$

Furthermore, the closed-loop expression of $\Delta\omega$ can be derived with the following two terms:

$$\Delta\omega(s) = \underbrace{\frac{G_{ol}(s)}{1+G_{ol}(s)}\Delta\omega_g(s)}_{\text{synchronization stability}} + \underbrace{\frac{G_2(s)}{1+G_1(s)\,G_2(s)}\Delta P_{dc2}(s)}_{\text{disturbance rejection}} \tag{12}$$

The first term on the right-hand side of Eq. (12) represents the

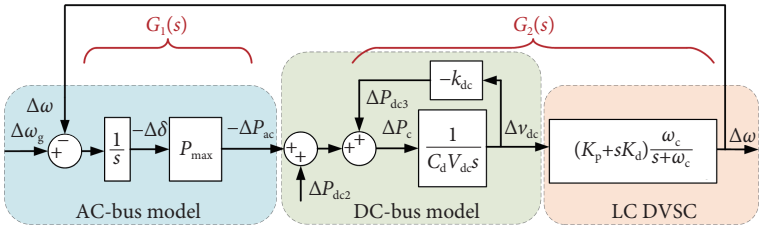

Figure 5 Small-signal model of synchronization control loop in AC-dominant mode.

synchronization stability, while the second term represents the rejection of the disturbance originated from the unregulated power ΔP_{dc2}. Assume the cutoff frequency of $G_{ol}(s)$ is ω_{sync}. For the low frequency range where $|s| << \omega_{sync}$, $|G_{ol}(s)| = |G_1(s)G_2(s)| >> 1$, and the magnitudes of the first and second terms become $|\Delta\omega_g|$ and $|\Delta P_{dc2}|/|G_1(s)|$, respectively. In contrast, for the high frequency range where $|s| >> \omega_{sync}$, $|G_{ol}(s)| = |G_1(s)G_2(s)| << 1$, and the magnitudes of the first and second terms become $|G_{ol}(s)|\cdot|\Delta\omega_g|$ and $|G_2(s)|\cdot|\Delta P_{dc2}|$, respectively. Thus, to enhance synchronization stability, it is desired to increase the cutoff frequency of $G_{ol}(s)$; to have a more robust disturbance rejection capability, it is desired to have a larger $|G_1(s)|$ (by having a larger P_{max}) in the low frequency range and a smaller $|G_2(s)|$ (by having a larger C_d, a larger k_{dc}, and a smaller K_d) in the high frequency range.

Because of the presence of the regulated droop power ΔP_{dc3}, the DC-link power model expressed by Eq. (4) changes from an integrator to an LPF through the combination of the integrator and the feedback loop in Figure 5, resulting in a higher phase margin. Moreover, with an increased k_{dc}, the disturbance rejection capability can be improved. However, as k_{dc} increases, the gain of $G_{ol}(s)$ diminishes, leading to a slower synchronization transient.

2.3 Steady-state analysis in AC-dominant mode

Assuming synchronization is achieved in the steady state (i.e., $\omega = \omega_g$), the relationship between the deviation of the DC-link voltage and the variation of angular frequency of the AC-bus voltage using the LC DVSC can be determined using Eq. (1) as

$$V_{dc} - V_{dcref} = (\omega_g - \omega_{ref}) / K_p \tag{13}$$

This suggests that a deviation in DC-link voltage occurs in the steady state when the AC-bus frequency differs from the reference frequency. The approach to choosing K_p involves maintaining the deviation of the DC-link voltage within an acceptable range (e.g., ±5%) to accommodate typical variations in AC-bus frequency (e.g., ±1%)[18]. This results in the limitation of K_p:

$$K_p \geqslant \frac{1\% \cdot \omega_{ref}}{5\% \cdot V_{dcref}} = 0.2 \text{ p.u.} \tag{14}$$

It is essential to recognize that when the AC-bus frequency surpasses the predefined range in Eq. (14), the deviation of the DC-link voltage can exceed the designed acceptable range. However, the deviation of the DC-link voltage can be effectively constrained by adjusting ω_{ref} or V_{dcref} in the LC DVSC, based on Eq. (13). As an example in Ref. [17], an auxiliary PLL can be used to adjust ω_{ref} to track the changes in ω_g and reduce the difference between v_{dc} and V_{dcref}. Since the paper focuses on the nominal operation of the VSC, the controller does not include the adjustment to ω_{ref} or V_{dcref}.

The benefit of permitting a variance in DC-link voltage lies in the fact that the devices connected to the DC bus can extract AC grid frequency information concurrently by monitoring the DC-link voltage according to Eq. (13). Furthermore, due to the v_{dc}/P_{dc} droop characteristic of the ESD outlined in Eq. (7), a ω_g/P_{ac} droop characteristic can be obtained at the PCC in the steady state as

$$P_{dc3} - P_{dcref3} = P_{ac} - P_{dcref} = -k_{dc}(\omega_g - \omega_{ref}) / K_p \tag{15}$$

where P_{dc1} and P_{dc2} are assumed to be stabilized at their references P_{dcref1} and P_{dcref2}, respectively, in the steady state; and P_{dcref} denotes the sum of P_{dcref1}, P_{dcref2} and P_{dcref3}.

Eq. (15) indicates that the DGFM VSC, when equipped with a droop-controlled ESD, can offer a frequency support for the AC grid similar to a conventional GFM VSC[8], but without the need for a stiff DC bus.

2.4 LC DVSC design guidelines in AC-dominant mode

The control parameters of the LC DVSC can be designed using the following guidelines based on Eqs. (9)–(15). (1) The P_{dc3}/V_{dc} droop gain, k_{dc}, can be determined by considering the capacity of the available ESD and the requirement for AC grid frequency support based on Eq. (15). (2) K_p and the phase margin of $G_{ol}(s)$ should be co-designed to maintain the deviation of the DC-link voltage within an acceptable range in both steady states and transients. (3) The cutoff frequency of $G_{ol}(s)$, ω_{sync}, should be set significantly lower than (e.g., one fifth) the cutoff frequency of the inner control loops to adhere to Assumption 2. Possible changes in the AC-line inductance L_g during operation can affect P_{max} and further influence the cutoff frequency and phase margin of $G_{ol}(s)$. Therefore, in a specific application scenario, it is essential to consider the potential range of L_g during the design process. It is recommended to use the medium value of L_g in the design to achieve overall optimal performance. (4) K_d and ω_c can be determined using the phase margin and ω_{sync} found in previous steps. (5) The disturbance rejection needs to be evaluated to maintain the deviation of the DC-link voltage within an acceptable range, considering the dynamics of the unregulated power P_{dc2}. If necessary, the DC-link capacitance C_d can be augmented. (6) Conduct simulations to ensure all requirements are satisfied within the potential range of L_g. (7) Revise the design by tuning the selected cutoff frequency/phase margin of $G_{ol}(s)$ if needed.

3 DGFM VSC operating in DC-dominant mode

In the DC-dominant mode, the VSCs need to uphold an AC voltage to serve as a frequency reference for the devices connected to the AC bus. This section begins with the derivation of DC-link voltage dynamics. Then, an assessment of both steady-state and transient performance of the DGFM VSC operating in the DC-dominant mode is provided. Lastly, design guidelines for the LC DVSC are provided.

3.1 DC-link voltage dynamics

In the DC-dominant mode, the DC bus of the DGFM VSC is modeled as a DC voltage source (denoted as v_d) connected in series with a resistance R_{dc}, and the AC bus is represented as an AC current source with an equivalent line inductance and resistance, as shown in Figure 6.

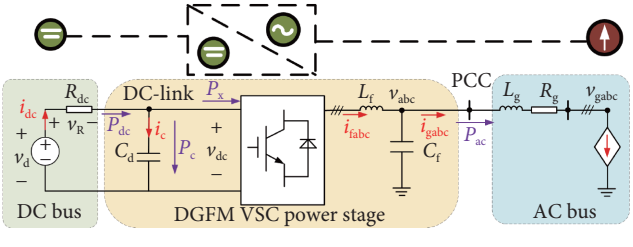

Figure 6 DGFM VSC operating in DC-dominant mode, where the LC DVSC is the same as that in Figure 2 and, thus, is omitted.

The small-signal perturbation of the DC-bus output current Δi_{dc} is derived as

$$\Delta i_{dc} = (\Delta v_d - \Delta v_{dc}) / R_{dc} \tag{16}$$

According to Eq. (16), ΔP_{dc} can be derived as

$$\begin{aligned}\Delta P_{dc} &= \Delta i_{dc} V_{dc} + I_{dc} \Delta v_{dc} \\ &= V_{dc} / R_{dc} \cdot \Delta v_d - \left(V_{dc} / R_{dc} - I_{dc}\right) \cdot \Delta v_{dc} \\ &\approx V_{dc} / R_{dc} \left(\Delta v_d - \Delta v_{dc}\right)\end{aligned} \tag{17}$$

where I_{dc} denotes the steady-state value of i_{dc}, which is assumed to be much smaller than the DC short circuit current V_{dc}/R_{dc}.

According to Eq. (4) and Eq. (17), the DC-link voltage dynamics can be derived as

$$\Delta v_{dc} = \frac{1}{C_d V_{dc} s + V_{dc} / R_{dc}} \left(-\Delta P_{ac}\right) + \frac{V_{dc} / R_{dc}}{C_d V_{dc} s + V_{dc} / R_{dc}} \Delta v_d \tag{18}$$

where $C_d V_{dc}$ denotes the charge stored in the DC-link capacitor at the steady-state operating point, while V_{dc}/R_{dc} can be considered equivalent to the charge generated by the DC short circuit current over one second, which is much larger than $C_d V_{dc}$. Thus, in a low frequency range where $|s| << 1/(C_d R_{dc})$, V_{dc}/R_{dc} significantly exceeds $|C_d V_{dc} s|$ and, therefore, Eq. (18) is simplified as

$$\Delta v_{dc} = R_{dc} / V_{dc} \cdot \left(-\Delta P_{ac}\right) + \Delta v_d \tag{19}$$

According to Eq. (16) and Eq. (19), Δi_{dc} can be derived as

$$\Delta i_{dc} = \Delta P_{ac} / V_{dc} \tag{20}$$

Then, the voltage drop on R_{dc}, Δv_R, can be obtained as

$$\Delta v_R = \Delta i_{dc} R_{dc} = \Delta P_{ac} \cdot R_{dc} / V_{dc} \tag{21}$$

3.2 Steady-state and transient performance analysis

In this mode, VSCs are primarily employed to maintain a stable AC-bus voltage for renewable energy sources, such as wind farms, or islanded AC loads connected to their AC side. The AC-bus power P_{ac} is exclusively determined by the renewable generation or the power demand of the AC loads, making ΔP_{ac} unaffected by the VSC frequency deviation $\Delta\omega$. Hence, in this mode, the LC DVSC operates in an open-loop control manner, as depicted by its small-signal model in Figure 7. Since the AC-bus voltage and frequency are maintained by the VSC, there is no synchronization issue. Thus, the following analysis will focus on the steady-state and transient performance of the VSC frequency.

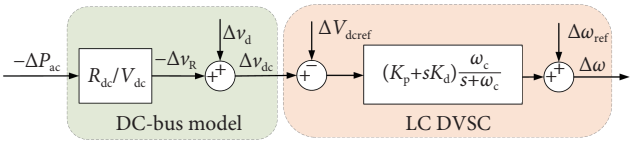

Figure 7 Small-signal model of the DGFM VSC in DC-dominant mode.

In the steady state where $s = 0$, there are two basic equations:

$$P_{ac} = P_{dc} = V_{dc} I_{dc} \tag{22}$$

$$V_d - V_{dc} = R_{dc} I_{dc} \tag{23}$$

where V_d denotes the steady-state value of the DC-bus voltage. Based on Eqs. (13), (22) and (23), the steady-state VSC frequency can be derived as

$$\omega = K_p \left(V_d - V_{dcref} - R_{dc} P_{ac} / V_{dc}\right) + \omega_{ref} \tag{24}$$

In contrast, in a high frequency range where $|s|$ is much larger than $1/(C_d R_{dc})$, K_p/K_d, and ω_c, the influence of the disturbances ΔP_{ac} and Δv_d on $\Delta\omega$ is derived as

$$\Delta\omega = \omega_c K_d \cdot \left[\left(-\Delta P_{ac}\right) / \left(C_d V_{dc} s\right) + \Delta v_d / \left(C_d R_{dc} s\right)\right] \tag{25}$$

The steady-state and transient performances of the VSC frequency are revealed in Eq. (24) and Eq. (25), respectively. It should be noted that the impact of the change in the DC-bus voltage Δv_d on the VSC frequency variation $\Delta\omega$ is significant in both steady states and high-frequency transients. Thus, devices connected to the AC bus can obtain the DC-bus voltage information by gauging the AC-bus frequency. This opens the possibility for the AC-side devices to contribute to stabilizing the DC-link voltage across the DGFM VSC power stage, a prospect that merits further investigation. For example, when a decrease in the DC-bus voltage Δv_d occurs, it leads to a drop in the DC-link voltage Δv_{dc}, as indicated in Figure 7. Then, the LC DVSC responds by decreasing the VSC frequency $\Delta\omega$. When a decrease in $\Delta\omega$ is detected, the AC-side devices can be controlled to output more active power, i.e., $-\Delta P_{ac}$ increases. As a result, the impact of the decrease of Δv_d on Δv_{dc} can be mitigated by the increase of $-\Delta P_{ac}$, as indicated in Eq. (19).

3.3 LC DVSC design guidelines in DC-dominant mode

Considering the steady-state deviation of the DC-bus voltage V_d and the AC-bus power P_{ac}, K_p can be established using Eq. (24) to limit the steady-state deviation of the VSC frequency ω from its reference ω_{ref}. Regarding the transient performance, reducing K_d and ω_c can mitigate the transient VSC frequency change caused by ΔP_{ac} and Δv_d, as indicated in Eq. (25). If necessary, increasing the DC-link capacitance C_d can additionally restrict the high-frequency fluctuation of the VSC frequency. Finally, simulations can confirm whether the VSC frequency variation $\Delta\omega$ is within an acceptable range, and if not, the LC DVSC parameters can be adjusted based on Eq. (24) and Eq. (25).

4 DGFM VSC operating in balanced mode

As illustrated in Figure 8, the DGFM VSCs operating in the balanced mode should facilitate energy sharing and reciprocal power support between the DC bus and the AC bus. Possible applications include using the DGFM VSC to interlink a DC grid and an AC grid within a hybrid microgrid system or an HVDC-based AC/DC system. This section discusses a possible instability problem related to the operation of the DGFM VSC in the balanced mode. To address this issue, a virtual resistance (VR) control is introduced. Subsequently, the steady-state analysis considering the effect of VR is outlined, followed by LC DVSC design guidelines.

4.1 Potential instability issue in balanced mode

The small-signal model of the synchronization control loop in the balanced mode is shown in Figure 9(a). The DC-bus model includes an extremely small gain, R_{dc}/V_{dc}, resulting in a low bandwidth of the synchronization control loop, which may lead to

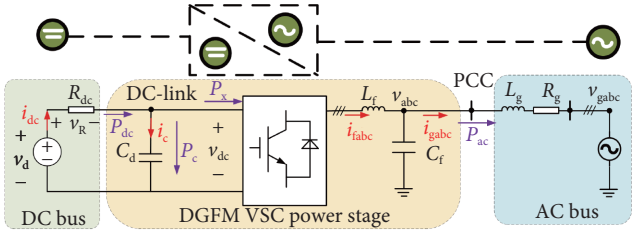

Figure 8 DGFM VSC operating in balanced mode, where the LC DVSC is the same as that in Figure 2 and, thus, is omitted.

instability of the synchronization control and a compromised disturbance rejection capability. This issue is even accentuated when the DC-bus voltage is stiff (indicating a small R_{dc}).

4.2 Proposed virtual resistance control and stability analysis

One approach to address the issue of a limited bandwidth of the synchronization control loop is to increase the gains of the LC DVSC, specifically K_p and K_d. While this approach can enhance synchronization stability, it also amplifies the disturbance caused by Δv_d, leading to inferior disturbance rejection performance.

Since the limited bandwidth of the synchronization control loop is caused by a small R_{dc}, an intuitive strategy to solve this problem is to add a VR into the LC DVSC. This is achieved by configuring the reference of the DC-link voltage as follows:

$$V_{dcref} = V_{dcnom} + R_V i_{dc} \tag{26}$$

where V_{dcnom} denotes the nominal value for the DC-link voltage, and R_V denotes the VR, which is a parameter of the LC DVSC.

Recalling Eq. (20), the small-signal expression of Eq. (26) can be derived as

$$\Delta V_{dcref} = R_V \Delta i_{dc} = \Delta P_{ac} \cdot R_V / V_{dc} \tag{27}$$

The small-signal model of the synchronization control loop with the VR is depicted in Figure 9(b), where the open-loop transfer function $T_{ol}(s)$ from $\Delta\omega_g$ to $\Delta\omega$ without the feedback loop is expressed as follows:

$$T_{ol}(s) = T_1(s)\,T_2(s) = \frac{P_{max}(R_{dc}+R_V)}{V_{dc}} \cdot \frac{\omega_c(K_p+sK_d)}{s(s+\omega_c)} \tag{28}$$

where

$$\begin{cases} T_1(s) = P_{max} \cdot \dfrac{(R_{dc}+R_V)}{V_{dc}} \cdot \dfrac{1}{s} \\ T_2(s) = \dfrac{\omega_c(K_p+sK_d)}{s+\omega_c} \end{cases} \tag{29}$$

Then, the closed-loop expression of $\Delta\omega(s)$ is derived with two parts:

$$\Delta\omega(s) = \underbrace{\frac{T_{ol}(s)}{1+T_{ol}(s)}\Delta\omega_g(s)}_{\text{synchronization stability}} + \underbrace{\frac{T_2(s)}{1+T_1(s)\,T_2(s)}\Delta v_d(s)}_{\text{disturbance rejection}} \tag{30}$$

As indicated in Eq. (29), R_V holds a position comparable to R_{dc} in $T_1(s)$, indicating that the VR serves a similar function as the DC-bus resistance in terms of synchronization stability and disturbance rejection shown in Eq. (30). Since R_V can be set much larger than R_{dc}, the integration of the VR can significantly boost the gain of $T_1(s)$, resulting in improved synchronization stability and enhanced disturbance rejection against Δv_d.

4.3 Steady-state analysis considering virtual resistance

By assuming that synchronization can be attained in the steady state (i.e., $\omega = \omega_g$), the steady-state AC-bus power P_{ac} can be derived through Eq. (22), (24), and (26) as follows:

$$P_{ac} = \frac{V_{dc}}{R_{dc}+R_V}\left[(V_d - V_{dcnom}) - \frac{1}{K_p}(\omega_g - \omega_{ref})\right] \tag{31}$$

Eq. (31) reveals P_{ac} is subjected to the deviations of the DC-bus voltage from its nominal value V_{dcnom} and the AC-bus frequency from its reference ω_{ref}, which are essential for the dynamic energy sharing between the DC bus and the AC bus. For instance, if the DC-bus voltage increases (i.e., $V_d > V_{dcnom}$), indicating an energy surplus in the DC bus, the DGFM will consequently supply more power to the AC bus (i.e., $P_{ac} > 0$), and vice versa. Likewise, if the AC-bus frequency increases (i.e., $\omega_g > \omega_{ref}$), signifying an excess energy in the AC bus, the DGFM will reduce the power output to the AC bus (i.e., $P_{ac} < 0$), and vice versa. It is noteworthy that K_p functions as a weighting factor in determining the importance between the variations of the DC-bus voltage and the AC-bus frequency, while the VR serves to regulate P_{ac} more precisely.

4.4 LC DVSC design guidelines in balanced mode

In the balanced mode, the parameter design for the LC DVSC is contingent upon Eqs. (26)–(31) and can be performed using the following guidelines. (1) The weighting factor K_p can be determined by assessing the relative significance of supporting the DC-bus voltage versus the AC-bus frequency. (2) R_V can be determined by considering the trade-off between the stability governed by Eqs. (28)–(30) and the adjustment range of P_{ac} in Eq. (31). For example, a larger R_V can improve the stability, but leads to a smaller P_{ac} and, therefore, a weaker power sharing capability between the DC and AC buses of the VSC for the same perturbations in v_d or ω_g. (3) The cutoff frequency of $T_{ol}(s)$ should be selected substantially lower than (e.g., one fifth) the cutoff frequency of the inner control loops to satisfy Assumption 2. Additionally, the phase margin of $T_{ol}(s)$ should be determined to balance the dynamic response

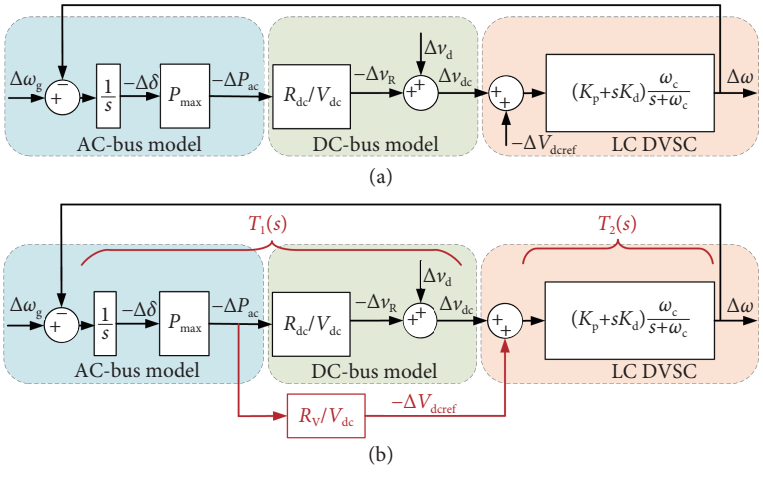

Figure 9 Small-signal model of synchronization control loop in balanced mode: (a) without VR; (b) with VR.

speed and the overshoots during transients. Possible changes in the AC-line inductance L_g during operation can affect P_{max} and further influence the cutoff frequency and phase margin of $T_{ol}(s)$. Therefore, in a specific application scenario, it is essential to consider the potential range of L_g during the design process. It is recommended to use the medium value of L_g in the design to achieve overall optimal performance. (4) The parameters K_d and ω_c can be computed using the selected cutoff frequency and phase margin of $T_{ol}(s)$. (5) The impact of the disturbance in the DC-bus voltage Δv_d on the VSC frequency dynamics $\Delta\omega$ expressed by Eq. (30) should be evaluated according to possible dynamics of $\Delta v_d(s)$ to ensure that the VSC does not lose synchronization with the AC bus. (6) Perform simulations to verify the stability and the steady-state performance of the DGFM VSC within the potential range of L_g. (7) Revise the design if necessary by adjusting the selected cutoff frequency/phase margin of $T_{ol}(s)$.

5 Simulation verification

The DGFM VSC with the LC DVSC shown in Figure 2 is tested in the three operation modes using high-fidelity large-signal simulations with discrete controllers conducted in the PLECS software. Table 1 presents the key parameters employed for the simulations. For each of the three distinct operation modes of the DGFM VSC, the MATLAB codes for calculating control parameters and the corresponding PLECS simulation files are accessible online[29].

For the PLECS simulations, the sampling frequency of analog signals generated by voltage and current sensors is set to be twice the VSC switching frequency of 10 kHz to minimize the discrete control delay of the controller; namely, the sampling interval T_s is set as 50 μs. The Forward–Euler method is utilized to convert the LC in Eq. (1) from s domain to z domain, yielding the following discrete LC, $LC(z)$.

$$LC(z) = K_p \frac{\omega_c T_s}{z + \omega_c T_s - 1} + K_d \frac{\omega_c}{1 + \omega_c \frac{T_s}{z-1}} \tag{32}$$

The cutoff frequencies of the inner voltage and current control are designed as 1 kHz and 100 Hz, respectively. The inner PI controllers for both the voltage control and the current control are discretized by the Trapezoidal method.

5.1 Simulation of DGFM VSC in AC-dominant mode

To validate the derived small-signal open-loop transfer function (9), a comparison is made between the modeled loop gains of the LC DVSC operating in the AC-dominant mode and their corresponding simulated counterparts. Specifically, the modeled loop gains are derived using $G_{ol}(s)$ of Eq. (9), whereas the simulated loop gains are obtained from a higher-fidelity simulation model in PLECS that accurately represents the dynamics of the synchronization control without relying on the Assumptions 1–3. This comparison considers different droop gains of the ESD, k_{dc}, as illustrated in Figure 10. The magnitude of the modeled $G_{ol}(s)$ closely aligns with the simulated result for various k_{dc} values. Moreover, with an increase in k_{dc} value, the magnitude of $G_{ol}(s)$ decreases, which confirms the analysis on the impact of k_{dc} presented in Section 2.2. Regarding the phase plot in Figure 10, the difference between the modeled and simulated results is negligible at low frequency but escalates as the frequency increases. Notably, at 20 Hz, a divergence of about 12° is observed consistently across

Table 1 Key parameters of simulation tests

Common parameters for three modes	
Rated AC-bus phase-ground voltage	110V RMS, 60 Hz
Rated DC-link voltage	380 V
Inductor-capacitor filters	L_f = 10 mH (ESR = 0.1Ω), C_f = 200 μF
DC-link capacitor	C_d = 1.5 mF
Switching frequency	10 kHz
Sampling frequency	20 kHz (double-rate sampling)
Inner voltage control	Cutoff frequency: 100 Hz
Inner current control	Cutoff frequency: 1 kHz
AC bus line impedance	L_g = 10 mH, R_g = 1 Ω
DGFM VSC operating in AC-dominant mode	
LC DVSC controller	K_p = 0.248 (0.25 p.u.); K_d = 0.0073, ω_c = 724.03 rad/s
Open-loop transfer function $G_{ol}(s)$	Cutoff frequency 20 Hz; Phase margin: 65°
DGFM VSC operating in DC-dominant mode	
LC DVSC controller	K_p = 0.248 (0.25 p.u.); K_d = 0, ω_c = 10π rad/s
DC line Resistance	R_{dc}= 1Ω
AC bus load Z_{load}	10Ω + 10mH for each phase
DGFM VSC operating in balanced mode	
LC DVSC controller	K_p = 0.1984 (0.2 p.u.); K_d = 0.0237, ω_c = 6.8766 rad/s
Virtual resistance	R_V = 2.688 Ω (for large-signal simulations)
Open-loop transfer function $T_{ol}(s)$	Cutoff frequency 2 Hz; Phase margin: 85°
VSC power rating	±5 kW
DC bus resistance	R_{dc} = 0.2 Ω

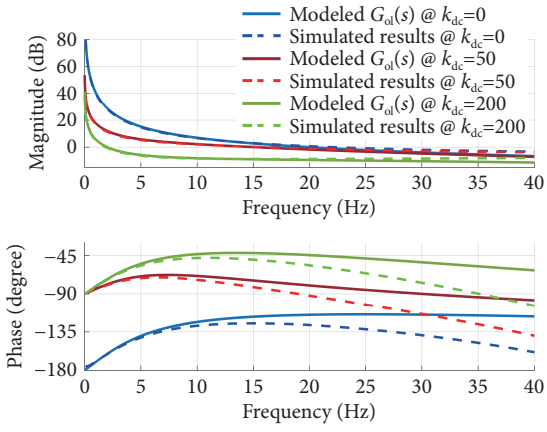

Figure 10 Modeled loop gains of the LC DVSC using $G_{ol}(s)$ in AC-dominant mode and its simulated counterparts with different droop gains of the ESD.

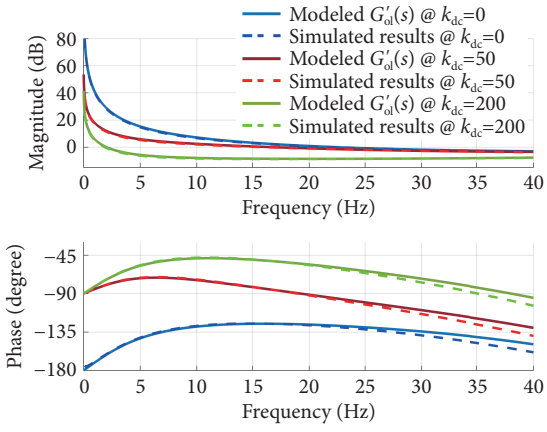

Figure 11 Modeled loop gains of the LC DVSC using $G_{ol}'(s)$ in AC-dominant mode considering the dynamics of the power flow through the line connected to the AC bus and its simulated counterparts with different droop gains of the ESD.

all cases with different k_{dc} values.

By replacing P_{max} in $G_{ol}(s)$ of Eq. (9) with the transfer function from $\Delta\delta$ to ΔP_{ac} in Eq. (A9), the dynamics of the power flow through the line connected to the AC bus is added to the new open-loop transfer function $G_{ol}'(s)$ as follows.

$$G_{ol}'(s)=\frac{3}{2}\left(\frac{V_m V_g X_g}{L_g^2 s^2+2R_g L_g s+X_g^2}\right)\frac{\omega_c}{(C_d V_{dc} s+k_{dc})}\cdot\frac{K_p+sK_d}{s(s+\omega_c)} \tag{33}$$

The modeled loop gains using $G_{ol}'(s)$ of Eq. (33) are compared with the simulated results in Figure 11. The simulated results in Figures 10 and 11 are the same. A comparison of Figures 10 and 11 clearly shows that the phase difference between the modeled and simulated results in Figure 10 is primarily attributed to the impact of the dynamics of the power flow through the line connected to the AC bus, which is neglected in the modeled results using $G_{ol}(s)$ with Assumption 3. Despite this, the phase deviation in Figure 10 remains acceptable in the low frequency range (e.g., < 20 Hz), and the potential negative impact introduced by the unmodeled phase delay can be mitigated by properly designing the parameters of the LC DVSC K_p, K_d, and ω_c and the droop gain k_{dc} of the ESD so that the $G_{ol}(s)$ has an adequately large phase margin. For instance, as confirmed in Figure 10, a higher k_{dc} value can increase the phase margin.

In Figure 11, the difference between the modeled and simulated results becomes pronounced in the high-frequency range (e.g., > 40 Hz). This discrepancy is attributed to the delay introduced by the inner PCC voltage control and current control, which is neglected with Assumption 2. However, the phase delay induced by the inner control loops is negligible in the low-frequency range (e.g., < 25 Hz). This observation supports the validity of Assumption 2 when designing a synchronization controller with a bandwidth within a low-frequency range.

To validate the dynamic and steady-state characteristics of the designed LC DVSC and assess the impact of the droop-controlled ESD, large-signal simulation tests consisting of three consecutive stages are carried out, as shown in Figure 12.

(1) In the first stage, a trapezoidal disturbance is imposed into the DC-bus power P_{dc} with a rate of change of 10 kW/s. During the slope periods, P_{dc} can be treated as unregulated power, transitioning into a constant power source/load once it is stabilized at 2kW/−2kW. To examine the disturbance rejection capability of the system under the most challenging conditions, the regulated droop power is excluded from P_{dc} in this stage by setting k_{dc} = 0.

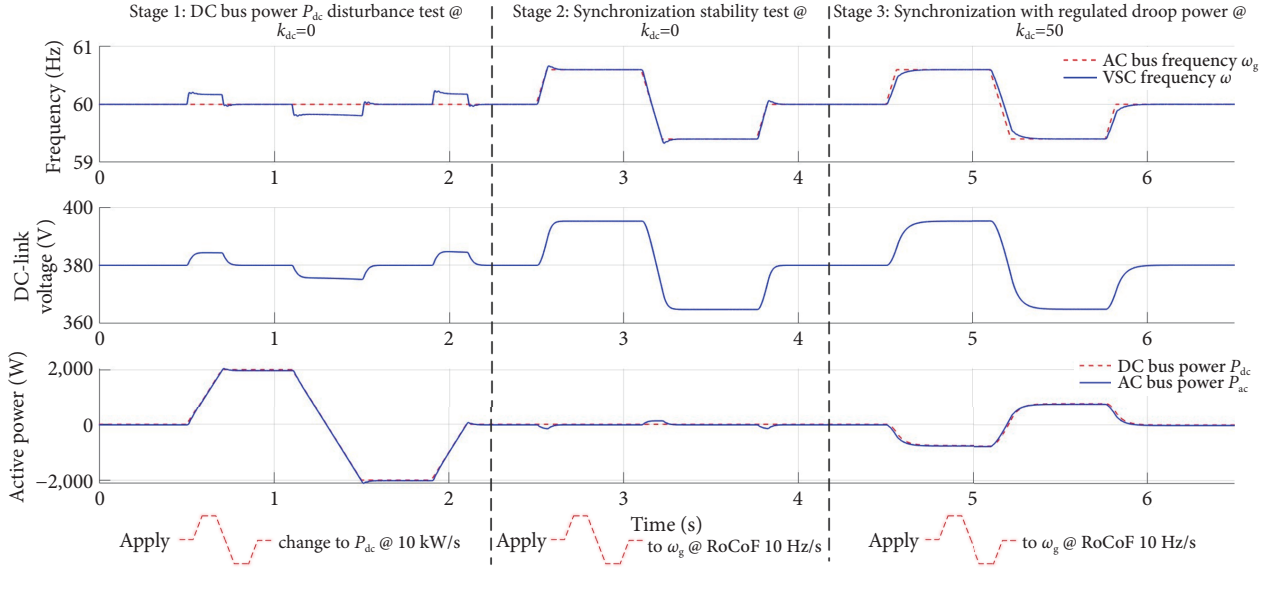

Figure 12 Large-signal simulation tests for DGFM VSC power stage in AC-dominant mode with disturbance from P_{dc} or ω_g.

As P_{dc} changes, three oscillations manifest in the VSC frequency. These oscillations cause a progressive/regressive phase angle difference between the PCC voltage and the AC bus voltage, corresponding to the rising/falling P_{dc} to be transferred to the AC bus. Moreover, when P_{dc} is stabilized, the frequency of the VSC power stage resumes synchronized with the AC bus, and the DC-link voltage is stabilized at its nominal value of 380 V.

(2) In the second stage, a trapezoidal disturbance is imposed into the AC-bus frequency ω_g, with a rate of change of frequency (RoCoF) set at 10 Hz/s. This disturbance causes the AC-bus frequency to deviate from its rated value by a maximum of ±0.6 Hz. The DGFM VSC power stage effectively maintains synchronization with the AC bus throughout both transient and steady states. Additionally, the DC-link voltage v_{dc} is adjusted in response to VSC frequency variations, following the control law specified in Eq. (1). In the steady state, the DC-link voltage deviation is proportional to the VSC frequency deviation, aligning precisely with Eq. (13).

(3) In the third stage, the disturbance persists in the same manner as in the second stage, yet now a droop-controlled ESD is connected to the DC link. This ESD is characterized by a nominal power P_{dc3ref} of 0 and a droop gain k_{dc} set at 50. In contrast to the previous test, the synchronization transients exhibit a slower response. This is attributed to the influence of k_{dc}, which reduces the open-loop bandwidth while augmenting the phase margin, thereby causing a deceleration in the dynamics of the VSC frequency. Moreover, the ω_g/P_{ac} droop characteristic at the PCC is validated. In the steady state, the P_{ac} deviation is proportional to the AC-bus frequency deviation, as indicated by Eq. (15).

5.2 Simulation of DGFM VSC in DC-dominant mode

The simulation setup for the DGFM VSC operating in the DC-dominant mode is illustrated in Figure 13. In this configuration, the AC-bus load consists of the line impedance and a balanced three-phase load Z_{load} when the switch S_2 is open. The LC DVSC in this mode is set as an LPF DVSC to reject high frequency disturbances by setting K_d to be 0. As shown in Figure 14, there are three successive tests: (1) At 0.5 s, when S_1 is closed, the balanced three-phase load is connected. This connection induces a step increase in P_{ac}. As anticipated from the model in Figure 7, both the DC-link voltage and the VSC frequency exhibit a slight decrease in the steady state. (2) At 1 s, when S_2 is closed, the impedance of phase C drops to $Z_{load}/2$. This unbalanced AC-bus load induces a second-order harmonic component in both P_{ac} and v_{dc}, but the designed LPF DVSC can effectively mitigate the impact of the harmonic on the VSC frequency. (3) At 1.5 s, a step increase is applied to v_d. The designed LPF DVSC enables a smooth transient response in the VSC frequency.

5.3 Simulation of DGFM VSC in balanced mode

With the VSC power rating and K_p provided in Table 1, and considering a maximum v_d deviation of 5% and maximum ω_g deviation of 1%, the lowest limit of R_V is calculated as 2.688 Ω based on Eq. (31). To validate the derived small-signal open-loop transfer function $T_{ol}(s)$ in Eq. (28) of the LC DVSC operating in the balanced mode, a comparison is conducted between the modeled loop gains $T_{ol}(s)$ and their corresponding simulated counterparts, considering various VR values. As shown in Figure 15, the magnitude of the modeled $T_{ol}(s)$ closely matches that of the simulated results for different R_V values. Moreover, an increase in R_V value leads to a higher magnitude and, thus, a higher bandwidth of $T_{ol}(s)$. The phase plots of the modeled gains overlap with each other for different R_V values. Similar overlapping patterns are observed in the simulated phases with different R_V values. These results show negligible influence of R_V on the phase of $T_{ol}(s)$. The difference between the modeled and the simulated results is minor at low frequency, but grows as the frequency increases.

Similar to the discussion in Section 5.1, by replacing P_{max} in $T_{ol}(s)$ of Eq. (28) with the transfer function from $\Delta\delta$ to ΔP_{ac} in Eq. (A9), the dynamics of the power flow through the line connected to the AC bus is added to the new open-loop transfer function $T_{ol}'(s)$ as follows.

$$T_{ol}'(s) = \frac{3}{2}\left(\frac{V_m V_g X_g}{L_g^2 s^2 + 2R_g L_g s + X_g^2}\right)\frac{(R_{dc}+R_V)}{V_{dc}} \cdot \frac{\omega_c (K_p + sK_d)}{s(s+\omega_c)} \tag{34}$$

In Figure 16, the modelled loop gains using $T_{ol}'(s)$ of Eq. (34) are compared with the simulated results. A comparison of Figures 15 and 16 clearly indicates that the phase divergence of the modeled results using $T_{ol}(s)$ is primarily caused by the dynamics of the power flow through the line connected to the AC bus, which is neglected with Assumption 3. However, this phase divergence in Figure 15 remains within acceptable limits, as it results in only a 1° phase deviation at the designated cutoff frequency of 2 Hz.

To assess the least stable scenario for operating the DGFM VSC in the balanced mode, R_V is deliberately set to its lowest limit in the large-signal simulation, which consists of three consecutive stages as shown in Figure 17.

(1) In the first stage, a trapezoidal disturbance is imposed in the DC-bus voltage v_d with a rate of change of 320 V/s. During the transients, three spikes occur in the VSC frequency to adjust the AC-bus power. When v_d is stabilized within ±5% deviations from the rated DC-link voltage, the VSC resumes synchronized with the AC bus, and the PCC output power is stabilized at half of the VSC's power rating of ±2.5 kW, as per design. The slight difference between the DC-link voltage v_{dc} and v_d is caused by the voltage drop on the DC-bus resistor. (2) Then, a trapezoidal disturbance with an RoCoF of 10 Hz/s is imposed into the AC-bus frequency. This disturbance causes frequency deviations up to ±1% from the rated frequency. The VSC frequency shows a synchronization process without any noticeable overshoots, which is anticipated by designing a large phase margin of 85°. The PCC output power can also stabilize at ±2.5 kW, equivalent to half of the VSC power rating, owing to the designed weighting factor K_p. (3) In the third stage, when the trapezoidal deviations are simultaneously applied to ω_g and v_d with reverse polarities, the VSC shows robust synchronization dynamics during the transients. Furthermore, the

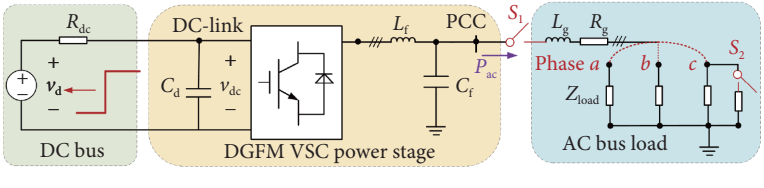

Figure 13 Simulation setup for DGFM VSC in DC-dominant mode.

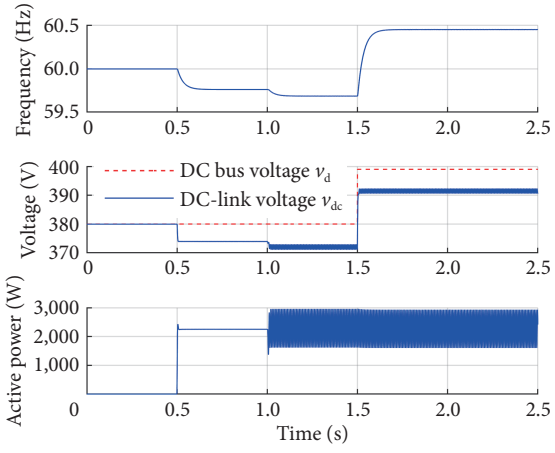

Figure 14 Large-signal simulation test for DGFM VSC in DC-dominant mode.

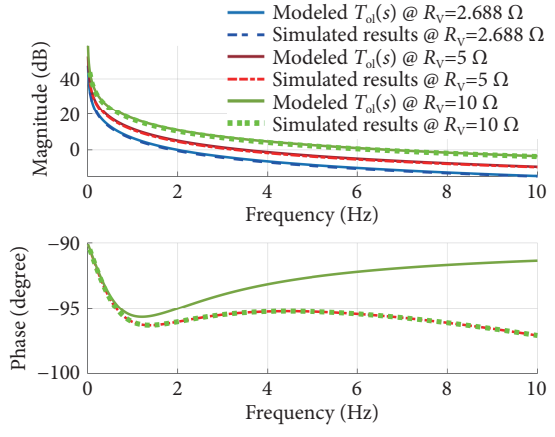

Figure 15 Modeled loop gains of the LC DVSC using $T_{ol}(s)$ in balanced mode and its simulated counterparts with different virtual resistance R_V.

PCC output power can be stabilized at the level of the VSC power rating of ±5 kW, accounting for the deviations in both v_d and ω_g based on Eq. (31).

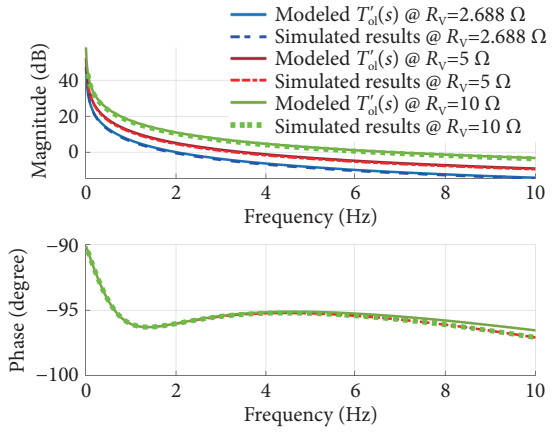

Figure 16 Modeled loop gains of the LC DVSC using $T_{ol}'(s)$ in balanced mode considering the dynamics of the power flow through the line connected to the AC bus and its simulated counterparts with different virtual resistance R_V.

6 Conclusions

This article established small-signal models for the DGFM VSC with the LC DVSC operating in all of three possible modes, respectively. Based on the models, the paper presented a quantitative analysis on the stability and steady-state performance of the LC DVSC. A potential instability issue is uncovered when the DGFM VSC is connected to a stiff DC-bus voltage in the balanced operation mode. To tackle this issue, a VR control is proposed and integrated with the LC DVSC to improve the synchronization stability and the disturbance rejection capability. Additionally, the VR assumes a pivotal function in regulating the VSC's output power. Based on the models and analysis, the paper provided step-by-step design guidelines for the LC DVSC in the three operation modes of the DGFM VSC. The simulation results validated the derived small-signal models, confirmed the analysis on the stability and steady-state performance, and verified the effectiveness of the design guidelines for the LC DVSC. In conclusion, this paper has demonstrated the practicability and effectiveness of employing the

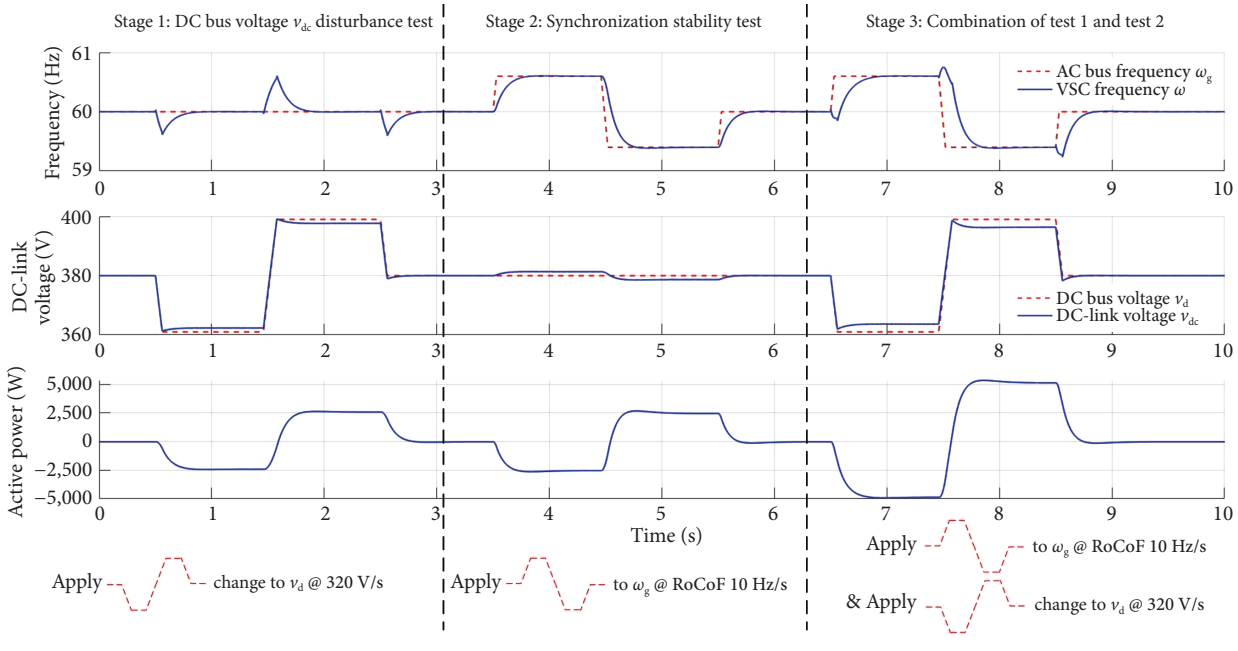

Figure 17 Large-signal simulation tests for DGFM VSC in balanced mode with disturbances from P_{dc} or/and ω_g @ R_V = 2.688 Ω.

DGFM VSC with the LC DVSC in all three operation modes. Moreover, by adopting the LC DVSC as the universal synchronization control technique for grid-tie VSCs, the challenges associated with accommodating and coordinating heterogeneous GFL and GFM VSCs in power systems can be mitigated.

Appendix

The small-signal dynamics of the power flow through the line connected to the AC bus is derived as follows. Near the equilibrium point, the amplitude of the AC-bus voltage stabilizes at V_g, and the amplitude of the PCC voltage stabilizes at V_m. In the amplitude-invariant dq reference frame, the relationship between the PCC voltage $\boldsymbol{v}_{dq}$ and the AC-bus voltage $\boldsymbol{v}_{gdq}$ can be derived as

$$\boldsymbol{v}_{gdq} = \boldsymbol{v}_{dq} - \boldsymbol{Z}_g \cdot \boldsymbol{i}_{gdq} \tag{A1}$$

where $\boldsymbol{Z}_g$ denotes the grid impedance matrix in the dq reference frame and $\boldsymbol{i}_{gdq}$ denotes the vector of the current flowing from the PCC to the AC bus. The voltage and current vectors and impedance matrix are defined as follows.

$$\boldsymbol{v}_{gdq} = \begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} = \begin{bmatrix} V_g \\ 0 \end{bmatrix}, \ \boldsymbol{v}_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} V_m \cos\delta \\ V_m \sin\delta \end{bmatrix} \tag{A2}$$

$$\boldsymbol{i}_{gdq} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}, \boldsymbol{Z}_g = \begin{bmatrix} sL_g + R_g & -X_g \\ X_g & sL_g + R_g \end{bmatrix} \tag{A3}$$

At the equilibrium point, by setting $s = 0$, the PCC voltage $\boldsymbol{V}_{dq}$ and the grid current $\boldsymbol{I}_{gdq}$ can be derived from (A1)–(A3) as follows

$$\boldsymbol{V}_{dq} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos\delta_0 \\ V_m \sin\delta_0 \end{bmatrix} \tag{A4}$$

$$\boldsymbol{I}_{gdq} = \begin{bmatrix} R_g & -X_g \\ X_g & R_g \end{bmatrix}^{-1} \cdot \begin{bmatrix} V_m \cos\delta_0 - V_g \\ V_m \sin\delta_0 \end{bmatrix} \tag{A5}$$

Also, the small-signal variables $\Delta\boldsymbol{i}_{gdq}$ and $\Delta\boldsymbol{v}_{dq}$ can be derived from (A1)–(A3) as

$$\Delta\boldsymbol{i}_{gdq} = \boldsymbol{Z}_g^{-1}\Delta\boldsymbol{v}_{dq} \tag{A6}$$

$$\Delta\boldsymbol{v}_{dq} = \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} = \begin{bmatrix} -V_m \sin\delta_0 \\ V_m \cos\delta_0 \end{bmatrix} \Delta\delta \tag{A7}$$

Then, based on the instantaneous power theory[30], the active power ΔP_{ac} flowing into the AC bus can be derived from (A4)–(A7) as

$$\begin{aligned} \Delta P_{ac} &= \frac{3}{2}\left(\Delta v_d I_{gd} + V_d \Delta i_{gd} + \Delta v_q I_{gq} + V_q \Delta i_{gq}\right) \\ &= \frac{3}{2}\left[-V_m \sin\delta_0 \cdot \frac{\left(V_m \cos\delta_0 - V_g\right)R_g + V_m \sin\delta_0 X_g}{R_g^{\,2} + X_g^{\,2}} + \right. \\ &\quad V_m \cos\delta_0 \cdot \frac{-V_m \sin\delta_0 \left(sL_g + R_g\right) + V_m \cos\delta_0 X_g}{\left(sL_g + R_g\right)^2 + X_g^{\,2}} + \\ &\quad V_m \cos\delta_0 \cdot \frac{V_m \sin\delta_0 R_g - \left(V_m \cos\delta_0 - V_g\right)X_g}{R_g^{\,2} + X_g^{\,2}} + \\ &\quad \left. V_m \sin\delta_0 \cdot \frac{V_m \cos\delta_0 \left(sL_g + R_g\right) + V_m \sin\delta_0 X_g}{\left(sL_g + R_g\right)^2 + X_g^{\,2}}\right]\Delta\delta \end{aligned} \tag{A7}$$

By assuming the steady-state phase angle difference $\delta_0 \approx 0$, $X_g >> R_g$, and $V_m \approx V_g$, the expression of (A8) can be simplified as

$$\Delta P_{ac} = \frac{3}{2}\left(\frac{V_m V_g X_g}{L_g^{\,2}s^2 + 2R_g L_g s + X_g^{\,2}}\right)\Delta\delta \tag{A9}$$

It should be noted that Eq. (5) is a special case of Eq. (A9) by setting both the variables s and R_g to be 0. This means that the power dynamics on the AC-bus line reactance in Eq. (A9) is neglected in Eq. (5) due to the utilization of Assumption 3. It is revealed in Eq. (A9) that the dynamics of the power flow through the line connected to the AC bus can lead to a progressively increasing phase delay of the transfer function from $\Delta\delta$ to ΔP_{ac} as the frequency of "s" increases. When the frequency of "s" reaches the nominal AC grid frequency (e.g., 50 or 60 Hz), the phase delay becomes a substantial 90°. However, when using Assumption 3, this phase delay is neglected to simplify the analysis and the design of the LC DVSC.

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Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

References

[1] Zhang, L., Harnefors, L., Nee, H. P. (2010). Power-synchronization control of grid-connected voltage-source converters. *IEEE Transactions on Power Systems*, 25: 809–820.

[2] Zhang, Z., Zhao, X. (2023). Coordinated power oscillation damping from a VSC-HVDC grid integrated with offshore wind farms: Using capacitors energy. *IEEE Transactions on Sustainable Energy*, 14: 751–762.

[3] Wang, J., Dong, C., Jin, C., Lin, P., Wang, P. (2022). Distributed uniform control for parallel bidirectional interlinking converters for resilient operation of hybrid AC/DC microgrid. *IEEE Transactions on Sustainable Energy*, 13: 3–13.

[4] Gu, Y., Li, Y., Yoo, H. J., Nguyen, T. T., Xiang, X., Kim, H. M., Junyent-Ferre, A., Green, T. C. (2019). Transfverter: Imbuing transformer-like properties in an interlink converter for robust control of a hybrid AC–DC microgrid. *IEEE Transactions on Power Electronics*, 34: 11332–11341.

[5] Shi, H., Sun, K., Hou, X., Li, Y., Jiang, H. (2022). Equilibrium mechanism between dc voltage and ac frequency for AC–DC interlinking converters. *iEnergy*, 1: 279–284.

[6] Mishra, P., Zhang, P. (2023). Physics-informed transient stability assessment of microgrids. *iEnergy*, 2: 231–239.

[7] Wang, X., Taul, M. G., Wu, H., Liao, Y., Blaabjerg, F., Harnefors, L. (2020). Grid-synchronization stability of converter-based resources—An overview. *IEEE Open Journal of Industry Applications*, 1: 115–134.

[8] Rocabert, J., Luna, A., Blaabjerg, F., Rodríguez, P. (2012). Control

of power converters in AC microgrids. *IEEE Transactions on Power Electronics*, 27: 4734–4749.

[9] Wu, H., Wang, X. (2023). Control of grid-forming VSCs: A perspective of adaptive fast/slow internal voltage source. *IEEE Transactions on Power Electronics*, 38: 10151–10169.

[10] Rathnayake, D. B., Razzaghi, R., Bahrani, B. (2022). Generalized virtual synchronous generator control design for renewable power systems. *IEEE Transactions on Sustainable Energy*, 13: 1021–1036.

[11] Gros, D., Colombino, M., Brouillon, J. S., Dorfler, F. (2019). The effect of transmission-line dynamics on grid-forming dispatchable virtual oscillator control. *IEEE Transactions on Control of Network Systems*, 6: 1148–1160.

[12] Singhal, A., Vu, T. L., Du, W. (2022). Consensus control for coordinating grid-forming and grid-following inverters in microgrids. *IEEE Transactions on Smart Grid*, 13: 4123–4133.

[13] Arghir, C., Dorfler, F. (2020). The electronic realization of synchronous machines: Model matching, angle tracking, and energy shaping techniques. *IEEE Transactions on Power Electronics*, 35: 4398–4410.

[14] Chen, D., Xu, Y., Huang, A. Q. (2017). Integration of DC microgrids as virtual synchronous machines into the AC grid. *IEEE Transactions on Industrial Electronics*, 64: 7455–7466.

[15] Li, G., Ma, F., Wang, Y., Weng, M., Chen, Z., Li, X. (2020). Design and operation analysis of virtual synchronous compensator. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8: 3835–3845.

[16] Cvetkovic, I., Boroyevich, D., Burgos, R., Li, C., Mattavelli, P. (2015). Modeling and control of grid-connected voltage-source converters emulating isotropic and anisotropic synchronous machines. In: Proceedings of the 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, Canada.

[17] Huang, L., Xin, H., Wang, Z., Wu, K., Wang, H., Hu, J., Lu, C. (2017). A virtual synchronous control for voltage-source converters utilizing dynamics of DC-link capacitor to realize self-synchronization. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5: 1565–1577.

[18] Lyu, X., Groß, D. (2024). Grid forming fast frequency response for PMSG-based wind turbines. *IEEE Transactions on Sustainable Energy*, 15: 23–38.

[19] Huang, L., Xin, H., Yang, H., Wang, Z., Xie, H. (2018). Interconnecting very weak AC systems by multiterminal VSC-HVDC links with a unified virtual synchronous control. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6: 1041–1053.

[20] Peng, Y., Shuai, Z., Shen, C., Hou, X., Shen, Z. J. (2023). Transient stabilization control of electric synchronous machine for preventing the collapse of DC-link voltage. *IEEE Transactions on Smart Grid*, 14: 82–93.

[21] Groß, D., Sánchez-Sánchez, E., Prieto-Araujo, E., Gomis-Bellmunt, O. (2022). Dual-port grid-forming control of MMCs and its applications to grids of grids. *IEEE Transactions on Power Delivery*, 37: 4721–4735.

[22] Subotic, I., Gros, D. (2022). Power-balancing dual-port grid-forming power converter control for renewable integration and hybrid AC/DC power systems. *IEEE Transactions on Control of Network Systems*, 9: 1949–1961.

[23] Zhao, L., Jin, Z., Wang, X. (2023). Small-signal synchronization stability of grid-forming converters with regulated DC-link dynamics. *IEEE Transactions on Industrial Electronics*, 70: 12399–12409.

[24] Zhao, L., Jin, Z., Wang, X. (2022). Transient stability of grid-forming converters with flexible DC-link voltage control. In: Proceedings of the 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan.

[25] Zhao, L., Jin, Z., Wang, X. (2023). Analysis and damping of low-frequency oscillation for DC-link voltage-synchronized VSCs. *IEEE Transactions on Power Electronics*, 38: 8177–8189.

[26] Zhang, S., Qiao, W., Qu, L., Wang, J. (2023). Comparative analysis on DC-link voltage synchronization controllers for dual-port grid-forming voltage-source converters. In: Proceedings of the 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA.

[27] Gomis-Bellmunt, O., Tavakoli, S. D., Lacerda, V. A., Prieto-Araujo, E. (2023). Grid-forming loads: Can the loads be in charge of forming the grid in modern power systems. *IEEE Transactions on Smart Grid*, 14: 1042–1055.

[28] Rong, Y., Shen, Z., Wang, J., Yu, J., Fan, B., Mocevic, S., Boroyevich, D., Burgos, R. (2023). PESNet 3.0: A WRN-based communication network with ±0.5 ns synchronization error for large-scale modular power converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11: 1827–1837.

[29] Zhang, S., Qiao, W., Qu, L., Wang, J., (2023). MATLAB codes for calculating control parameters of the lead-compensator-based DGFM VSC and PLECS simulation files for the three operation modes. Available at: https://github.com/ShuoZhang222/iEnergy_DGFM.git.

[30] Akagi, H., Watanabe, E. H., Aredes, M. (2017). *Instantaneous Power Theory and Applications to Power Conditioning, 2nd edn*. Hoboken, NJ, USA: John Wiley & Sons.