

A Novel ON-State Resistance Estimation Technique for Online Condition Monitoring of Semiconductor Devices Under Noisy Conditions

MOHSEN ASOODAR¹ (Student Member, IEEE), MEHRDAD NAHALPARVARI¹ (Student Member, IEEE), SIMON SCHNEIDER¹, IMAN SHAFIKHANI², GUNNAR INGESTRÖM³, AND HANS-PETER NEE¹ (Fellow, IEEE)

¹Department of Electrical Engineering, KTH Royal Institute of Technology, 114 28 Stockholm, Sweden

²Department of Electrical Engineering, Linköping University, 581 83 Linköping, Sweden

³Grid and Power Quality Solutions, Hitachi Energy Sweden AB, Västerås, Sweden

CORRESPONDING AUTHOR: M. ASOODAR (e-mail: asoodar@kth.se)

This work was supported by the Grid and Power Quality Solutions (GPQS) Unit of Hitachi Energy Sweden AB.

ABSTRACT This article presents a novel method for accurate online extraction of semiconductor ON-state resistance in the presence of measurement noise. In this method, the ON-state resistance value is extracted from the measured ON-state voltage of the semiconductors and the measured load current. The extracted ON-state resistance can be used for online condition monitoring of semiconductors. The proposed method is based on the extraction of selective harmonic content. The estimated values are further enhanced through an integral action that increases the signal-to-noise ratio, making the proposed method suitable in the presence of noisy measurements. The efficacy of the proposed method is verified through simulations in the MATLAB/Simulink environment, and experimentally. The estimated ON-state resistance values from the online setup are compared to offline measurements from an industrial curve tracer, where an overall estimation error of less than 1% is observed. The proposed solution maintains its estimation accuracy under variable load conditions and for different temperatures of the device under test.

INDEX TERMS Condition monitoring, health monitoring, online estimation, ON-state resistance, reliability, semiconductor devices, state of health.

I. INTRODUCTION

THE ON-STATE voltage of semiconductors is a key characteristic which can be used for online junction temperature estimation, thermal modeling of semiconductor modules, and online condition monitoring of semiconductor devices [1], [2], [3], [4], [5], [6], [7]. It is also a useful figure of merit for analyzing conduction losses and can help with accurate online loss calculations [8].

Semiconductor devices sustain temperature fluctuations, which result in thermo-mechanical degradation over time [9]. This, in turn, increases their ON-state resistance. Hence, tracking this resistance can help in identifying the current health state of semiconductor devices. Even though certain

standards, such as AQG 324, use the deviation in the ON-state voltage of semiconductor devices to identify their health state, changes in the ON-state voltage as a result of package degradation are mainly attributed to the changes in the ON-state resistance [10]. This is true for both unipolar devices [11], [12] and bipolar devices [4], [11], [13]. Hence, in online monitoring applications, regardless of the type of semiconductor device, it is beneficial to identify the ON-state resistance of semiconductors [1], [2], [3], [4].

For a fixed temperature and fixed gate voltage, an increase in the ON-state resistance larger than 20% of its initial value is reported as an end-of-life (EOL) criterion [14]. Consequently, in order to confidently detect aging, or to

precisely estimate the junction temperature, an accurate estimation of the ON-state resistance is required. The ON-state resistance is typically extracted from the ON-state voltage measurements and load current [8], [15], [16]. A multitude of considerations are needed for accurate measurement of the ON-state voltage. To begin with, the bandwidth of the measurement system must be sufficiently high in order to avoid measurement distortion. Moreover, the measurement circuit must be able to withstand the high voltage of the semiconductor device in the OFF state. The measurement circuit should not be sensitive to temperature variations, or distort the ON-state voltage measurement in any way (by imposing an offset or gain error). Many circuits have been suggested that provide high measurement bandwidths [8], [15], [16], [17]. In [8], [17], [18], [19], and [20], the use of a double-diode circuit is suggested, where the diodes help to block the OFF-state voltage, and the double-diode system allows for compensating the voltage offset created by the blocking diode's forward voltage. In [8], the double-diode solution is investigated thoroughly. This design is shown to have sufficient bandwidth, however, even with reasonable design considerations, in some cases, the temperatures of the two-voltage blocking diodes are stated to be 3 °C apart. Considering a typical temperature coefficient of 2 mV/°C for the blocking diodes, this temperature difference can cause an offset error of 6 mV [11]. Furthermore, parameter spreads are expected in all semiconductor components. In [8], a 10-mV difference in forward voltage is observed for two diodes with the same part numbers. For many semiconductor devices, these levels of offset are sufficiently high to distort the measurements, especially in the low-current operation of the converter. This kind of offset is especially concerning because it may change over time as a result of load variations or temperature variations in the device.

In [16], [21], [22], and [23], depletion mode MOSFETs (DM-MOSFETs) are used for protecting the measurement circuit from the OFF-state voltage. This design is shown to also have a high bandwidth when a small resistance is placed between the gate–source terminals of the DM-MOSFETs [16]. A significant advantage of these designs is that the DM-MOSFET of the measurement circuit is a resistive channel. Hence, unlike the double-diode solutions, the circuit with DM-MOSFETs does not cause variable offset errors. The ON-state resistance of the DM-MOSFETs is typically much lower than the input impedance of the measurement stage, resulting in a negligible gain error in the measurements. In this article, the solution based on DM-MOSFETs is used in order to avoid measurement errors caused by temperature variations and variable offsets.

Although the measurement circuit based on DM-MOSFETs is superior to the double-diode system in maintaining low measurement errors, it is shown in this article that measurement noise can cause large errors in the estimated ON-state resistance [23], [24]. Therefore, it is important to devise post-processing algorithms that allow accurate estimation of the ON-state resistance in noisy environments. The effects

of noise and measurement offsets on the estimated ON-state resistance have not been well addressed in the literature. Moreover, methods for minimizing these effects have not been thoroughly investigated. Furthermore, in many studies, the measurement data of the online ON-state resistance has not been compared with a reliable reference value. This has been considered in [16], where the online measurements are compared to offline measurements extracted by a curve tracer. However, even though the presence of noise and offsets is reported, no suitable methods for mitigating their effect in an online setup are suggested. In [16], an estimation error of 2.9% is reported; however, the estimations are conducted under constant load and under low-noise conditions. Similarly, in [24], online measurements of V – I curves have been compared to curve-traced measurements; however, they have shown that at nominal voltages and currents, the switching noise significantly distorts the ON-state voltage measurements. No solution was provided on how to overcome the issue of the recorded measurement noise in that study. In [8], estimation errors of $\pm 3\%$ are reported; however, the comparison is made with datasheet information, rather than offline measurements with curve tracers. A unique method of accurate ON-state resistance estimation is proposed in [23], where the effects of noise and offsets are considered. That method is only applicable to modular multilevel converters, where the existing redundancies are leveraged for achieving a high estimation accuracy. In [18], a circuit for online V_{CE} measurements is presented; however, the circuit is tested via injecting a smooth low-frequency current into the device. That is, there is no actual switching present in the verification hardware, and the procedure is similar to how offline measurement systems operate. A similar argument can be made for [25] and [26]. The issue with such experimental setups is that when hard-switching is eliminated, lower measurement noise and other measurement inaccuracies are present.

The main goal of this article is to propose a method for accurate online estimation of the ON-state resistance, especially when measurements are subject to high levels of measurement noise. The estimated data can then be used for many purposes, such as online condition monitoring of the semiconductor devices, junction temperature monitoring, etc. The relationship between ON-state resistance, device health, and junction temperature has been thoroughly investigated in the literature and is not repeated in this article [2], [7], [9], [10], [11], [12], [14], [19], [26], [27], [28]. The proposed method in this article is a frequency-based approach for online estimation of ON-state resistance. The efficacy of frequency-based estimations for offline measurements is shown in [29]. However, online estimations in practical power electronic setups where high levels of noise are present are not considered in that paper. In [30], another frequency-based method is proposed for online estimation of the ON-state resistance. That solution requires additional hardware for injecting current into the semiconductor under test (SUT). In this article, it is shown that no additional

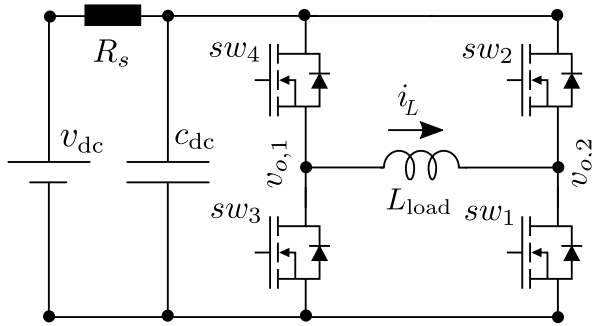


FIGURE 1. Single-phase full-bridge converter with inductive load.

hardware is needed for injecting auxiliary current into the SUT to achieve accurate and online frequency-based estimation of the ON-state resistance. The proposed solution is mainly designed for silicon-based and silicon-carbide-based (SiC) semiconductors, where no dynamic ON-state resistance variations are present [15], [16]. The main contributions of this article are as follows.

- 1) A novel estimation method that provides accurate estimations even in extremely noisy environments.
- 2) Experimental validation of the efficacy of the proposed solution under variable load conditions.
- 3) Experimental validation of estimation accuracy under variable temperatures of the SUT.
- 4) Detailed assessment of accuracy through comparison of online estimations and offline measurements from a commercial curve tracer.

The solution proposed in this article is demonstrated on a full-bridge converter; however, the proposed method is not application-specific and may be used in any power converter where the load current and ON-state voltage measurements are available. In converters operating at much higher switching frequencies than what is reported in this article, it is also important to ensure that the voltage and current measurement circuits possess sufficiently high measurement bandwidth. This article is organized as follows. Section II discusses the converter system on which the solution is studied, followed by a circuit diagram of the $v_{DS,ON}$ measurement circuit, and an explanation of its operation. Section III presents the proposed method for extracting $r_{DS,ON}$ from the ON-state voltage measurement of semiconductor devices. Simulation results of the proposed method are presented in Section IV, and experimental validations are shown in Section V. Finally, the conclusions of this article are provided in Section VI.

II. ON-STATE VOLTAGE MEASUREMENT

In this article, a single-phase full-bridge converter is chosen for simulations and experimental verification. The circuit diagram of the studied system is shown in Fig. 1. The converter is controlled in open loop and an inductive load is used to represent a typical load for power converters.

Accurate measurement of the ON-state voltage of semiconductors is needed for accurate estimation of the ON-state resistance. Moreover, an online measurement system must

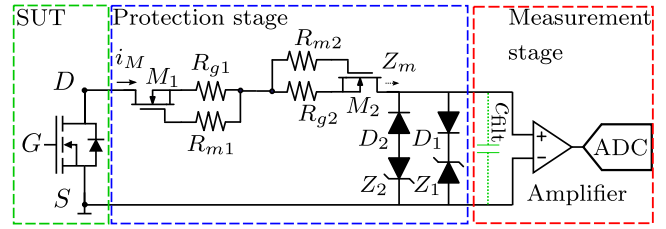


FIGURE 2. ON-state voltage measurement circuit using depletion-mode MOSFETs for protection against high voltages of the SUT [21].

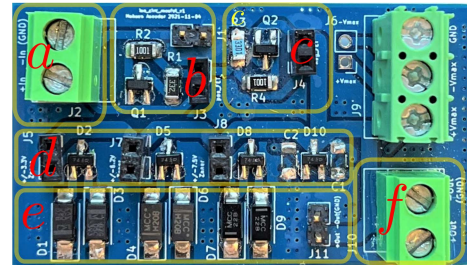


FIGURE 3. PCB of the protection stage for the ON-state voltage measurement circuit in Fig. 2. (a) Input connection to the drain–source terminals. (b) M_1 , R_{g1} , and R_{m1} . (c) M_2 , R_{g2} , and R_{m2} . (d) Protective diodes, including D_1 and D_2 . (e) Protective Zener diodes, including Z_1 and Z_2 . (f) Output connection to the measurement stage.

TABLE 1. Selected components for the ON-state voltage measurement circuit of Fig. 2.

Symbol	Part Number	Value
M_1, M_2	BSS126	–
R_{g1}, R_{g2}	–	3.3 k Ω
R_{m1}, R_{m2}	–	1.0 k Ω
D_1, D_2	BAS70-04	–
Z_1, Z_2	3SMAJ5920B	–
Filtering capacitor	C_{filt}	150 pF

be able to withstand the high voltages of the semiconductor device while it is in the OFF state. Several semiconductor ON-state voltage measurement circuits have been introduced in the literature that provide both protection against high voltages, and accurate voltage measurement while the semiconductor is ON [18], [21], [22], [23]. In this article, the isolation circuit based on self-triggering depletion-mode MOSFETs is used. A diagram of this solution is shown in Fig. 2, and the printed circuit board (PCB) of this design is shown in Fig. 3. In this article, a single-position design is considered for the DM-MOSFETs; however, the scalability of this circuit design for higher voltages has been demonstrated in [31]. A detailed explanation of the selected isolation circuit is presented in [23]. The main components used in the PCB of Fig. 3 are summarized in Table 1. In this design, when the voltage over the SUT is less than the breakdown voltage of the Zener diodes Z_1 and Z_2 , the MOSFETs M_1 and M_2 are in their ON state. Hence, the sensed voltage at the measurement stage is the same as the v_{DS} of the SUT. However, when v_{DS} is larger than the breakdown voltage of Z_1 , a small current passes through the

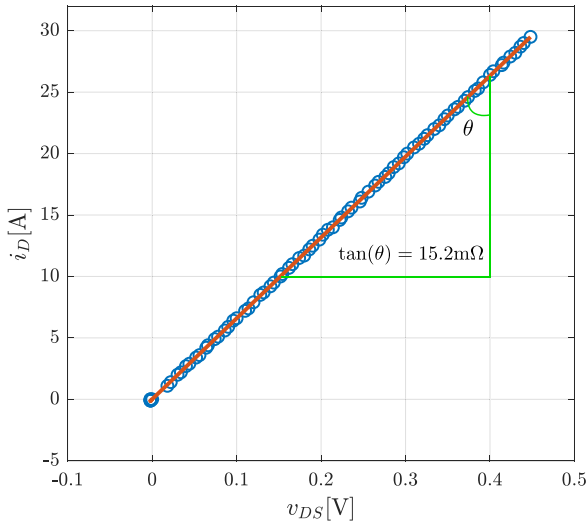


FIGURE 4. Measured v_{DS} - i_D curve (blue) of the IRFP4768 MOSFET using the Tektronix 371A curve tracer, and at $v_{GS} = 15$ V. The linear fit (red) of the measured data indicates an ON-state resistance of 15.2 m Ω .

protection stage creating a negative voltage over R_{g1} , which switches M_1 to its OFF state. The same can be said for Z_2 , R_{g2} , and M_2 for large negative voltages of v_{DS} ; however, in normal operating conditions, large negative voltages for v_{DS} are not expected. In the measurement stage, a filtering capacitor c_{filt} may optionally be placed. The resistors R_{m1} and R_{m2} can be used to change the switching time of M_1 and M_2 ; so, for larger values of R_{m1} and R_{m2} , slower transitions are expected for M_1 and M_2 , respectively.

III. EXTRACTING THE ON-STATE RESISTANCE

In this article, the IRFP4768 MOSFET is used for simulations and experimental results. The forward characteristic of this MOSFET has been measured using the Tektronix 371A curve tracer and shown as a v_{DS} - i_D curve in Fig. 4. The optimal linear fit to this curve is also calculated using the least-square method and shown in the same figure. The slope of the fitted curve represents the ON-state resistance of the device. This value is measured to be 15.20 m Ω . The measurements are conducted at room temperature of 20 $^{\circ}$ C and with a gate-source voltage (v_{GS}) of 15 V. The reverse characteristics of this device shows an ON-state resistance of 15.25 m Ω . Due to the similarity of the forward and reverse ON-state resistance, these two parameters are not separated in this article; however, methods for realizing this separation have been presented later in this section.

In an online setup, the circuit of Fig. 3 is connected to the SUT. The load current (i_L) as well as the ON-state voltage ($v_{DS,ON}$) are measured. Based on the switching function of the SUT, the current passing through each device can be estimated. For example, in the full-bridge converter of Fig. 1, i_{s1} which is the instantaneous current passing through the switch sw_1 can be estimated as

$$i_{s1} = s_1 i_L \quad (1)$$

TABLE 2. Parameters used for the full-bridge converter system shown in Fig. 1.

System parameter	Symbol	Value	Unit
Dc-bus voltage	v_{dc}	30	Vdc
Dc-link capacitor	c_{dc}	2.5	mF
Load inductance	L_{load}	3	mH
Stray resistance of power supply	R_s	30	m Ω
Switching frequency	f_{sw}	1.11	kHz
Forward ON-state resistance	$r_{DS,ON}$	15.2	m Ω
Voltage measurement noise	$v_{DS,n}$	$V_{DS,n} \sim \mathcal{N}(0, 0.015^2)$	V
Current measurement noise	$i_{L,n}$	$I_{L,n} \sim \mathcal{N}(0, 0.3^2)$	A

where s_1 represents the switching function of sw_1 , such that $s_i = 1$ and $s_i = 0$ correspond to the ON-state and OFF-state of the switch sw_i , respectively.

Theoretically, a single sample of $v_{DS,ON}$ and i_{s1} should provide an accurate estimation of the ON-state resistance. However, the presence of noise and other transients in an online circuit may distort the measurements [23], [24]. Hence, a multitude of data points are necessary for accurate estimation of the ON-state resistance. In practice, there are limitations on available memory, and also on computational power for conducting parameter estimations. Hence, in this article, a suitable method for ON-state resistance estimation is provided that:

- 1) requires a minimal amount of memory;
- 2) is computationally efficient and can be implemented easily in simple processors;
- 3) provides high estimation accuracies making it suitable for condition monitoring purposes.

The parameters of the converter system of Fig. 1 are summarized in Table 2. For these parameters, and considering a modulation index of $M = 0.7$, the ON-state voltage and current of sw_1 are simulated and depicted in Fig. 5(a). When processing the data, any measured voltage that is clamped to the breakdown voltages of Z_1 and Z_2 is set to zero. This is why the voltage measurements of Fig. 5(a) are shown to be zero when the SUT is in the OFF state. The voltage and current noise levels in the simulation are chosen to be of Gaussian distribution with a standard deviation of $\sigma_v = 15$ mV and $\sigma_i = 300$ mA, respectively. These values are in the range of what has been measured in the experimental setup explained in Section V. The estimated values of ON-state resistance $r_{DS,ON}$ using the sampled $v_{DS,ON}$ and $i_{s,1}$ data are plotted in Fig. 5(b), where it is shown that single-point estimations are not suitable for accurately estimating the ON-state resistance. Hence, post processing of the measured $v_{DS,ON}$ and $i_{s,1}$ data is required. In the following sections, a description of the state-of-the-art solution as well as a description of the proposed estimation algorithm are provided.

A. RLS-BASED ESTIMATION

Due to the piecewise linearity of the v_{DS} - i_D curve, a recursive least-square (RLS) estimation may be used to

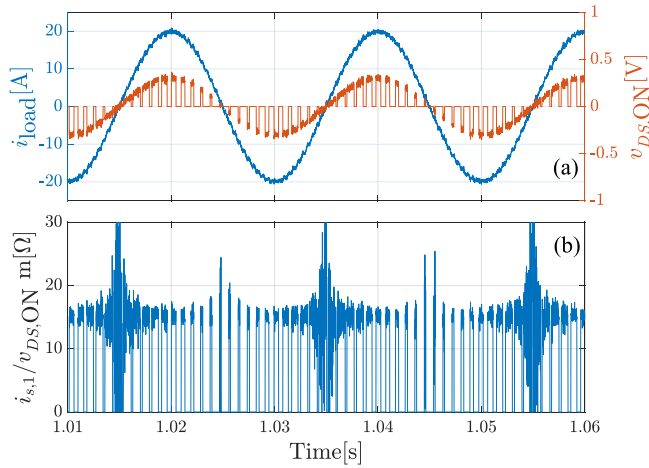


FIGURE 5. (a) Simulated load current (blue) and ON-state voltage of sw_1 (red) using the parameters of Table 2. (b) Estimated ON-state resistance by dividing the measured ON-state voltages and currents.

identify the linear relation between $v_{DS,ON}$ and i_D , i.e., the ON-state resistance. This method is currently regarded as the state-of-the-art solution [23], [27].

The ON-state model of a MOSFET can be described as

$$\hat{v}_{DS} = X^T A \quad (2)$$

where $X = [i_{DS} \ 1]^T$, and $A = [\hat{r}_{DS,ON} \ \hat{v}_0]^T$. v_0 represents the voltage offset, including the forward voltage of IGBTs and diodes at low currents. The parameters \hat{v}_{DS} , \hat{r}_{DS} , and \hat{v}_0 represent the estimated values of v_{DS} , r_{DS} , and v_0 , respectively. After each sampling instance, the error between the measured and estimated value of v_{DS} is calculated as

$$e = v_{DS} - \hat{v}_{DS} = v_{DS} - X^T A. \quad (3)$$

The Kalman gain K , covariance matrix P , and estimated parameter matrix A are updated as described in Algorithm 1 [23]. The forgetting factor λ is set to 1 (disabled) since the RLS estimator is reset each time an estimation is recorded. The RLS estimation method is implemented in the simulation model with the parameters of Table 2. It is evident from Fig. 6 that after only 0.04 s (two fundamental cycles) of estimation, the estimated resistance is within $\pm 0.5\%$ of the reference value. The total estimation error of the RLS method with the conditions of Table 2 is 0.2%.

A similar estimation method has been proposed in [27] and [28]; however, the accuracy of the proposed solutions has not been compared with accurate references, and the sensitivity of the solutions has not been investigated in different operational conditions.

B. PROPOSED ESTIMATION METHOD

The ON-state voltage and current of a semiconductor contain specific harmonic content. Through isolation and extraction of selected harmonic contents, accurate estimation of the ON-state resistance can be achieved. This selective harmonic-based estimation (SHE) method is performed

Algorithm 1 RLS Estimation Algorithm for the Estimation of $r_{DS,ON}$

0. Define $X = [i_D \ 1]^T$ and $A = [\hat{r}_{DS,ON} \ \hat{v}_0]^T$, and initiate matrices A and P :

$$A[1] = [0 \ 0]^T, \text{ and } P[1] = \begin{bmatrix} 10 & 0 \\ 0 & 10 \end{bmatrix}.$$

1. Sample $v_{DS}[n]$ and $i_D[n]$.

2. Calculate the estimation error:

$$e[n] = v_{DS}[n] - \hat{v}_{DS}[n] = v_{DS}[n] - X[n]^T A[n-1].$$

3. Update the Kalman gain $K[n]$:

$$K[n] = \frac{P[n-1]X[n]}{(\lambda + X^T[n]P[n-1]X[n])}.$$

4. Update the covariance matrix $P[n]$:

$$P[n] = \frac{1}{\lambda(P[n-1] - K[n]X^T[n]P[n-1])}.$$

5. Update the estimated values of $A[n]$:

$$A[n] = A[n-1] + K[n]e[n]$$

6. $n = n + 1$, and repeat.

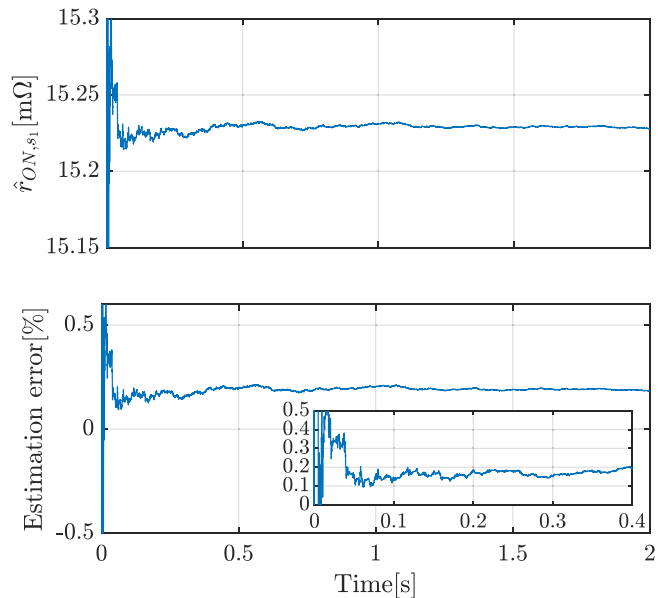


FIGURE 6. Estimated $\hat{r}_{ON,s1}$ using the RLS method and considering the parameters of Table 2.

on a full-bridge converter using carrier-based modulation. However, the method can be applied to other modulation schemes as well. For simplicity, a triangular carrier with natural sampling is considered. For a sinusoidal output voltage of $M \cos(\omega_0 t + \theta_0)$ p.u., the reference signal for switches sw_1 and sw_2 is defined as

$$\begin{aligned} v_{ref,sw_1} &= 0.5 - 0.5M \cos(\omega_0 t + \theta_0) \\ v_{ref,sw_2} &= 0.5 + 0.5M \cos(\omega_0 t + \theta_0) \end{aligned} \quad (4)$$

where M is the modulation index, and θ_0 is the phase angle of the fundamental frequency component of the reference voltage. Replacing θ_0 with $\theta_0 + \pi$ in (4) provides the reference signals for $v_{ref,s3}$ and $v_{ref,s4}$, respectively.

The modulated signal of each reference provides the corresponding switching function. For sw_1 , s_1 can be described as

$$s_1 = 0.5 + 0.5M \cos(\omega_0 t + \theta_0) + h_{s_1} \quad (5)$$

where h_{s_1} represents all other harmonics of s_1 aside from the dc and fundamental frequency components [32]. The output voltage of the full-bridge converter in Fig. 1 can be described as

$$\begin{aligned} v_{\text{out}} &= v_{\text{dc}}[s_4 - s_2] \\ &= v_{\text{dc}}[s_1 - s_3] \\ &= Mv_{\text{dc}} \cos(\omega_0 t + \theta_0) + v_{\text{dc}}[h_{s_1} - h_{s_3}]. \end{aligned} \quad (6)$$

Hence, for a linear load, the load current will contain a fundamental harmonic component as well as the switching harmonics that are not canceled in $h_{s_1} - h_{s_3}$. Therefore, the load current can be described as

$$i_L = i_m \cos(\omega_0 t + \theta_{i_L}) + h_{i_L}. \quad (7)$$

Substituting s_1 and i_L in (1) with (5) and (7) yields

$$\begin{aligned} i_{s_1} &= [0.5 + 0.5M \cos(\omega_0 t + \theta_0) + h_{s_1}] \\ &\times [i_m \cos(\omega_0 t + \theta_{i_L}) + h_{i_L}] \\ &= \underbrace{0.5i_m \cos(\omega_0 t + \theta_{i_L})}_{I_1} \\ &+ \underbrace{i_m \cos(\omega_0 t + \theta_{i_L})[0.5M \cos(\omega_0 t + \theta_0) + h_{s_1}]}_{I_2} \\ &+ \underbrace{h_{i_L}[0.5 + 0.5M \cos(\omega_0 t + \theta_0) + h_{s_1}]}_{I_3}. \end{aligned} \quad (8)$$

The term I_1 in (8) indicates that there is a significant fundamental frequency component in i_{s_1} . Given the presence of ON-state resistance in MOSFETs, the ON-state voltage of sw_1 can be simply modeled as

$$v_{s_1} = i_{s_1} r_{\text{ON},s_1}. \quad (9)$$

Consequently, v_{s_1} must also contain a significant fundamental frequency component. Extracting the fundamental frequency component of v_{s_1} and i_{s_1} can therefore be used to estimate the ON-state resistance r_{ON,s_1} . Under the condition of choosing a carrier frequency that is not an integer multiple of the fundamental frequency, only I_1 in (8) contains a fundamental frequency component [32], [33]. The proposed method of extracting the fundamental frequency components from v_{s_1} and i_{s_1} is to first mirror these components onto a direct-quadratic dq reference frame as

$$\begin{aligned} i_{s_1,d} &= i_{s_1} \cos(\omega_0 t) \\ i_{s_1,q} &= i_{s_1} \sin(\omega_0 t). \end{aligned} \quad (10)$$

Substituting i_{s_1} in (10) with (8) yields

$$\begin{aligned} i_{s_1,d} &= [I_1 + I_2 + I_3] \cos(\omega_0 t) \\ i_{s_1,q} &= [I_1 + I_2 + I_3] \sin(\omega_0 t). \end{aligned} \quad (11)$$

The terms $I_1 \cos(\omega_0 t)$ and $I_1 \sin(\omega_0 t)$ create a dc component and a second-order harmonic. It is these dc terms that are of interest for extracting r_{ON,s_1} . The terms $I_2 \cos(\omega_0 t)$ and $I_2 \sin(\omega_0 t)$ create a fundamental harmonic, a second-order harmonic, a third-order harmonic, and multiple components of higher-order harmonics. $I_3 \cos(\omega_0 t)$ and $I_3 \sin(\omega_0 t)$ may also contain harmonics of orders that are noninteger multiples of the fundamental. In order to increase the magnitude of the dc components compared to the other harmonics and noise, each mirrored component in the dq -frame is integrated over time by

$$\begin{aligned} I_{s_1,d} &= \int_{t_0}^{t_{\text{end}}} i_{s_1,d} dt \\ I_{s_1,q} &= \int_{t_0}^{t_{\text{end}}} i_{s_1,q} dt. \end{aligned} \quad (12)$$

Since the time integrals of non-dc harmonics remain oscillatory, they become less significant as the integrated dc terms in $i_{s_1,d}$ and $i_{s_1,q}$ grow. Since $I_{s_1,d}$ and $I_{s_1,q}$ contain harmonics of fundamental order as well as its integer multiples, it is advisable—but not necessary—to define t_{end} as an integer multiple of the fundamental period. This selection of the time period results in zeroing of the integrated harmonics that are an integer multiple of the fundamental frequency. Hence, the estimation error is lowest with such a selection of integration windows.

Similarly, v_{s_1} can be mirrored onto the dq -frame, and integrated over time. This results in

$$\begin{aligned} V_{s_1,d} &= \int_{t_0}^{t_{\text{end}}} v_{s_1} \cos(\omega_0 t) dt \\ V_{s_1,q} &= \int_{t_0}^{t_{\text{end}}} v_{s_1} \sin(\omega_0 t) dt. \end{aligned} \quad (13)$$

Using (13) and (12), the ON-state resistance r_{ON,s_1} can be estimated as

$$\hat{r}_{\text{ON},s_1} \approx \frac{\sqrt{V_{s_1,d}^2 + V_{s_1,q}^2}}{\sqrt{I_{s_1,d}^2 + I_{s_1,q}^2}} = \frac{V_{s_1}}{I_{s_1}}. \quad (14)$$

For the system parameters shown in Table 2, the proposed solution is verified through simulation studies. Fig. 7 shows the values of V_{s_1} , I_{s_1} , and \hat{r}_{ON,s_1} over time. It is evident that after three fundamental cycles, the estimation error becomes less than 0.1%. Hence, for the noise levels of Table 2, the SHE method provides a higher accuracy than the RLS estimation technique.

The results depicted in Fig. 7 are obtained under constant load conditions; however, the proposed solution can robustly estimate the ON-state resistance under variable load conditions as well. This is illustrated in Fig. 8 where the load is changed every 400 ms, while the estimated resistance and estimation error remain within the $\pm 1\%$ of their expected value.

Thus far, the forward and reverse conduction paths of the SUT are assumed to have the same ON-state resistance. In order to separately identify the ON-state resistance in the

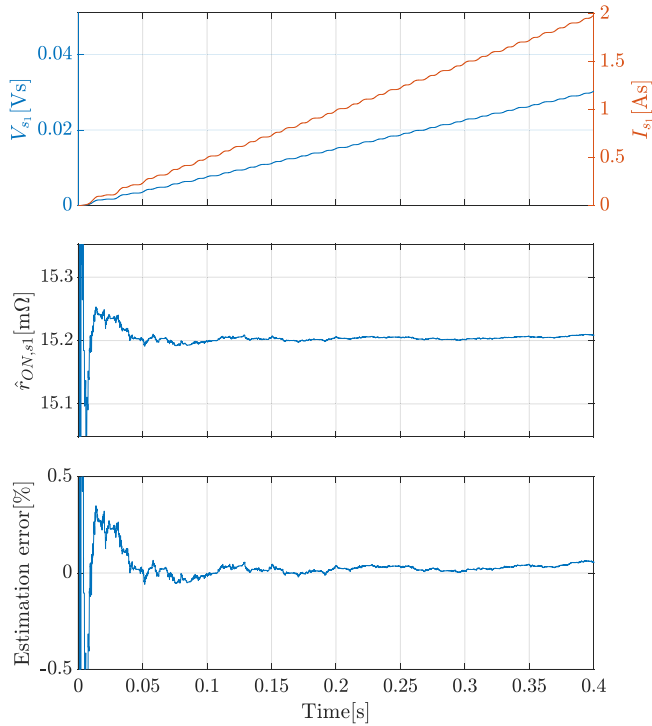


FIGURE 7. Estimated \hat{r}_{ON,s_1} using the SHE method and considering the parameters of Table 2. The integrated ON-state voltage V_{s_1} and integrated ON-state current I_{s_1} of sw_1 are calculated according to (14).

forward and reverse conduction paths, (10) and (13) can be modified to

$$\begin{aligned} i_{ps1,d} &= i_{s1} \frac{1 + \text{sgn}[i_{s1}]}{2} \cos(\omega_0 t) \\ i_{ps1,q} &= i_{s1} \frac{1 + \text{sgn}[i_{s1}]}{2} \sin(\omega_0 t) \\ i_{ns1,d} &= i_{s1} \frac{1 - \text{sgn}[i_{s1}]}{2} \cos(\omega_0 t) \\ i_{ns1,q} &= i_{s1} \frac{1 - \text{sgn}[i_{s1}]}{2} \sin(\omega_0 t) \end{aligned} \quad (15)$$

and

$$\begin{aligned} v_{ps1,d} &= v_{s1} \frac{1 + \text{sgn}[i_{s1}]}{2} \cos(\omega_0 t) \\ v_{ps1,q} &= v_{s1} \frac{1 + \text{sgn}[i_{s1}]}{2} \sin(\omega_0 t) \\ v_{ns1,d} &= v_{s1} \frac{1 - \text{sgn}[i_{s1}]}{2} \cos(\omega_0 t) \\ v_{ns1,q} &= v_{s1} \frac{1 - \text{sgn}[i_{s1}]}{2} \sin(\omega_0 t) \end{aligned} \quad (16)$$

where $\text{sgn}(x)$ represents the sign function of parameter x . In (15) and (16), the nonpositive (non-negative) SUT current samples—and their corresponding ON-state voltage samples—are zeroed when estimating the forward (reverse) ON-state resistance. As seen in Fig. 5, despite zeroing the nonpositive or non-negative SUT current samples, the measured waveforms still contain a dominant fundamental

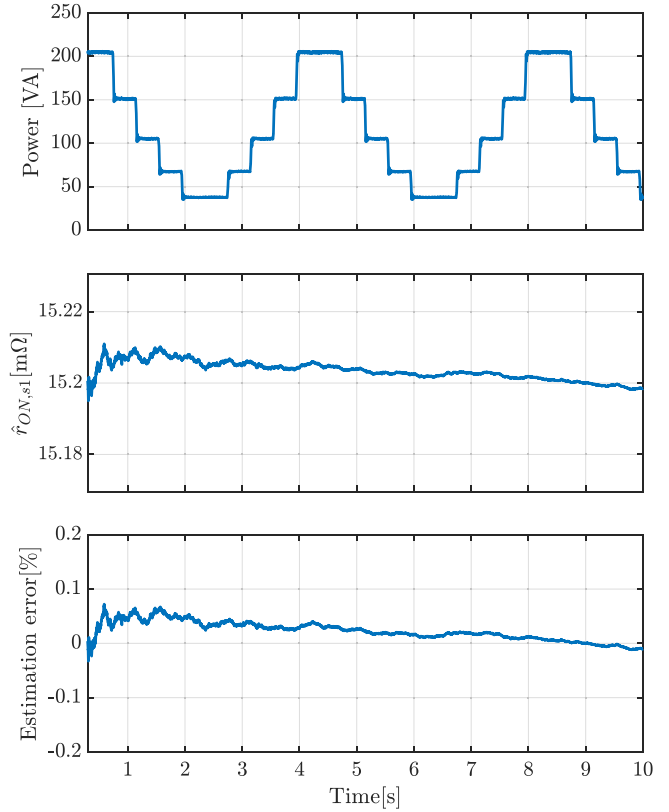


FIGURE 8. Estimated \hat{r}_{ON,s_1} using the SHE method and considering the parameters of Table 2. The output power of the converter is changed every 400 ms of operation.

frequency component. Hence, the forward and reverse ON-state resistance can be separately measured by extracting their fundamental frequency components, similar to what is described in (12) and (13). That is, r_{xON,s_1} can be calculated as

$$\hat{r}_{xON,s_1} \approx \frac{\sqrt{V_{xs1,d}^2 + V_{xs1,q}^2}}{\sqrt{I_{xs1,d}^2 + I_{xs1,q}^2}} = \frac{V_{xs1}}{I_{xs1}} \quad (17)$$

where

$$\begin{aligned} V_{xs1,d} &= \int_{t_0}^{t_{\text{end}}} v_{xs1,d} dt \\ V_{xs1,q} &= \int_{t_0}^{t_{\text{end}}} v_{xs1,q} dt \\ I_{xs1,d} &= \int_{t_0}^{t_{\text{end}}} i_{xs1,d} dt \\ I_{xs1,q} &= \int_{t_0}^{t_{\text{end}}} i_{xs1,q} dt \end{aligned} \quad (18)$$

and x denotes p for forward current conduction, and n for reverse current conduction.

IV. COMPARATIVE STUDIES

Both the RLS and SHE techniques provide accurate estimations of ON-state resistance for normal operation and typical

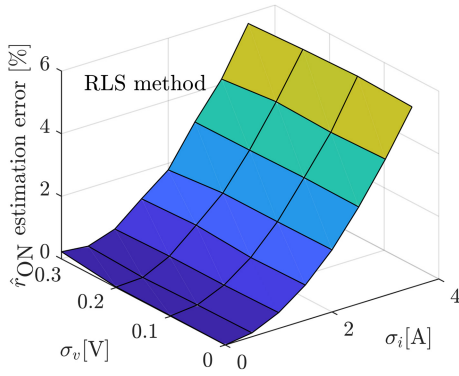


FIGURE 9. Effect of measurement noise on the RLS estimation method for extracting the ON-state resistance. The parameters used for this study are summarized in Table 2. The measurement noise for both the voltage and current measurements are assumed to be Gaussian with standard deviations of σ_v and σ_i , respectively.

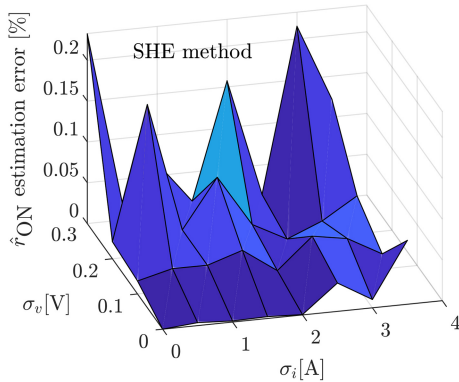


FIGURE 10. Effect of measurement noise on the SHE method for extracting the ON-state resistance. The parameters used for this study are summarized in Table 2. The measurement noise for both the voltage and current measurements are assumed to be Gaussian with standard deviations of σ_v and σ_i , respectively.

measurement conditions. However, under very noisy conditions, larger errors may be observed. The two estimation methods are compared when the measurement noise of the ON-state voltage and semiconductor current is artificially increased. Both voltage and current noises are assumed to be Gaussian, with standard deviations of σ_v and σ_i , respectively. The estimation errors under different levels of noise in voltage and current measurements are shown in Fig. 9 for the RLS method and in Fig. 10 for the SHE method. In both figures, the estimated values are recorded after 3 s of estimation. The results show the efficacy of the SHE method even under extreme levels of noise. This is because the SHE extracts information of selected low-frequency harmonic content. Hence, presence of any other harmonic content, which is typically of higher orders of frequency, has a smaller effect on the outcome of the SHE. A prominent feature of the proposed estimation technique is that there is no need to redesign the measurement circuit for different loads or environments. The proposed estimation technique automatically mitigates any uncertainties that may be caused by noise.

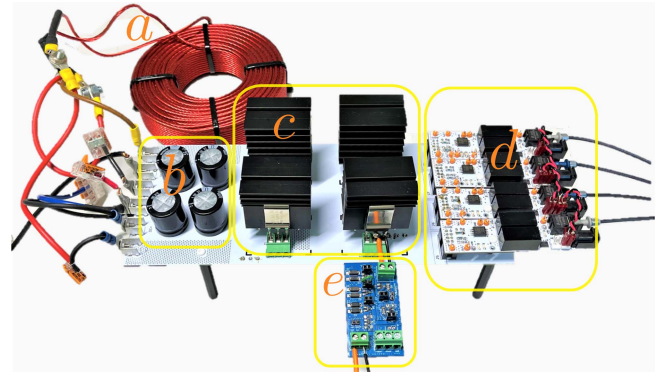


FIGURE 11. Experimental setup for the system shown in Fig. 1 and with the parameters of Table 2. (a) Load inductor, (b) dc-link capacitor, (c) semiconductors and their heat sink, (d) isolated gate drivers, and (e) protection stage of the ON-state voltage measurement circuit shown in Fig. 3.

V. EXPERIMENTAL VALIDATION

The proposed method of ON-state resistance extraction is demonstrated on an experimental setup with the parameters of Table 2. The efficacy of the proposed estimation technique is experimentally verified under varying load conditions, under three different switching frequencies, and under various temperatures of the SUT.

A. EXPERIMENTAL SETUP

The experimental setup is shown in Fig. 11. Each semiconductor of the full bridge is equipped with a separate isolated gate driver. The turn-ON voltage of the gate drivers is controlled to 15 V. For the control system, a Xilinx Zynq-7000 SoC module is used. Fig. 12 shows the recorded load current and ON-state voltage waveforms, as well as the direct estimation of the ON-state resistance. In the ON-state voltage waveform, the measurement data are digitally zeroed during the breakdown of the protective Zener diodes. This is carried out for better visibility, and to avoid erroneous estimations. It can be seen in Fig. 12(c) that even for the small levels of noise present in this hardware setup, high estimation errors are expected when using direct estimation techniques. Even though the estimation error reduces at higher currents, it is not sufficiently low for the high estimation accuracies required for condition monitoring purposes. This is more clearly depicted in Fig. 13 where the measured range of ON-state voltages for every current is illustrated. Fig. 13 shows that even at peak load current of 18 A, the ON-state voltage varies between 0.22 and 0.33 V, resulting in direct ON-state resistance estimations ranging from 12.2 to 18.3 m Ω . The recordings show the presence of Gaussian noise with $V_{DS,n} \sim \mathcal{N}(0, 0.01^2)$ V for the ON-state voltage measurements, and with $I_{L,n} \sim \mathcal{N}(0.08, 0.63^2)$ A for the load current measurements. The probability density function (PDF) of the measured noise as well as the Gaussian fit to these measurements are shown in Fig. 14. Hence, for the experimental setup of Fig. 11, under various operation modes, the measurement noise in both voltage and current measurements was naturally of Gaussian nature. No other

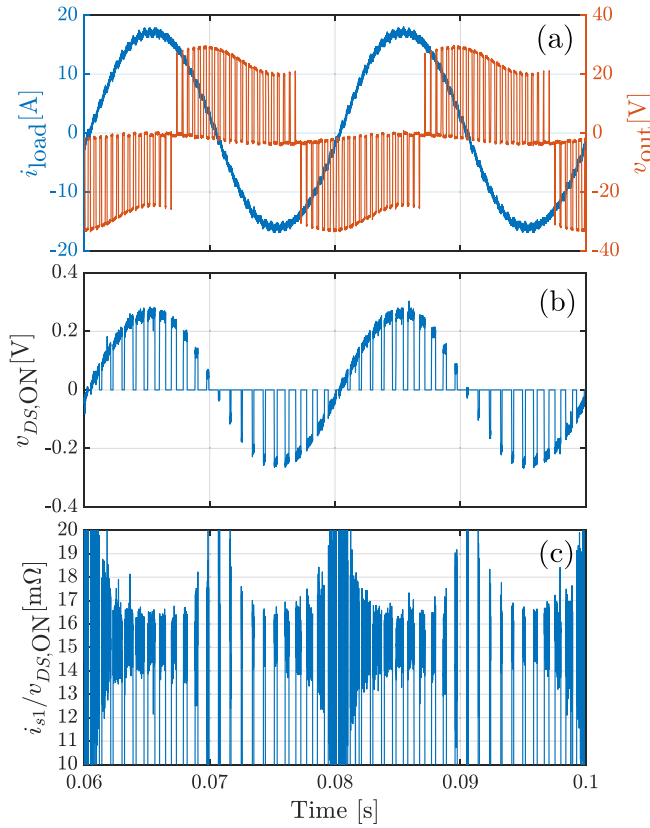


FIGURE 12. Recorded waveforms of (a) load current and output voltage, (b) ON-state voltage, and (c) direct estimation of the ON-state resistance of the converter system in Fig. 11 when operated with the parameters of Table 2.

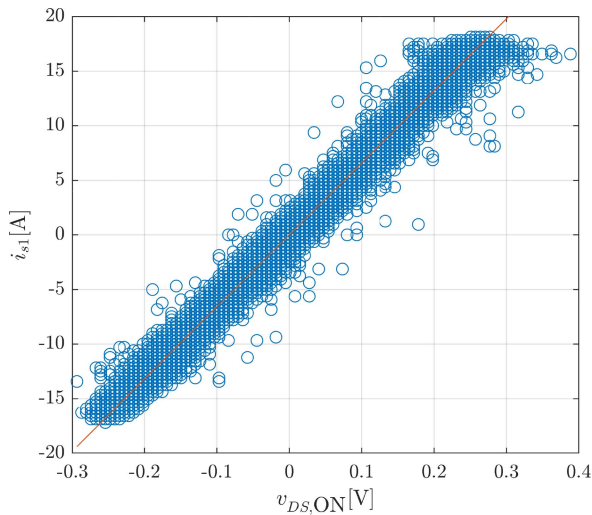


FIGURE 13. Measured ON-state voltage at different levels of the SUT's current when the converter is operated with the parameters of Table 2. The red line shows the linear fit to the measured data.

type of noise has been observed in the measurements. This noise includes the noise generated through hard-switching, as well as conducted and radiated noise from external circuits.

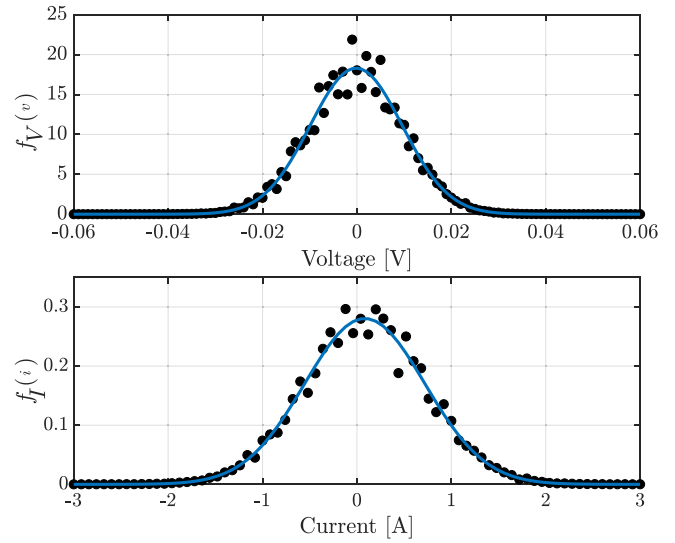


FIGURE 14. PDF of measurement noise (black ●) and its Gaussian fit (blue) for recorded load current and ON-state voltage of the converter system in Fig. 11 when operated with the parameters of Table 2. The fitted Gaussian curves suggest a distribution of $V_{DS,n} \sim \mathcal{N}(0, 0.01^2)$ V for the ON-state voltage measurements, and $I_{L,n} \sim \mathcal{N}(0.08, 0.63^2)$ A for the load current measurements.

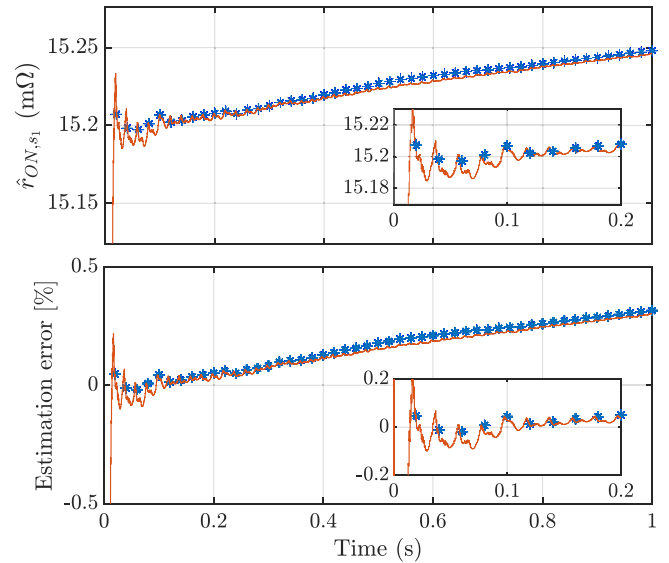


FIGURE 15. Estimated ON-state resistance of the IRFP4768 MOSFET in the experimental setup, and using the RLS (red), and SHE (blue ×) estimation methods.

B. EXPERIMENTAL RESULTS

For the parameters of Table 2, the ON-state resistance of the IRFP4768 MOSFET is extracted from the experimental setup using the proposed estimation method and the RLS estimation method. The results are depicted in Fig. 15. Compared to the curve-traced results of Fig. 4, both methods show an estimation error of less than 0.5% after 0.1 s of estimation. The gradual increase of resistance seen in the experimental results is due to the internal heating of the semiconductor under operation. For consistency, prior to

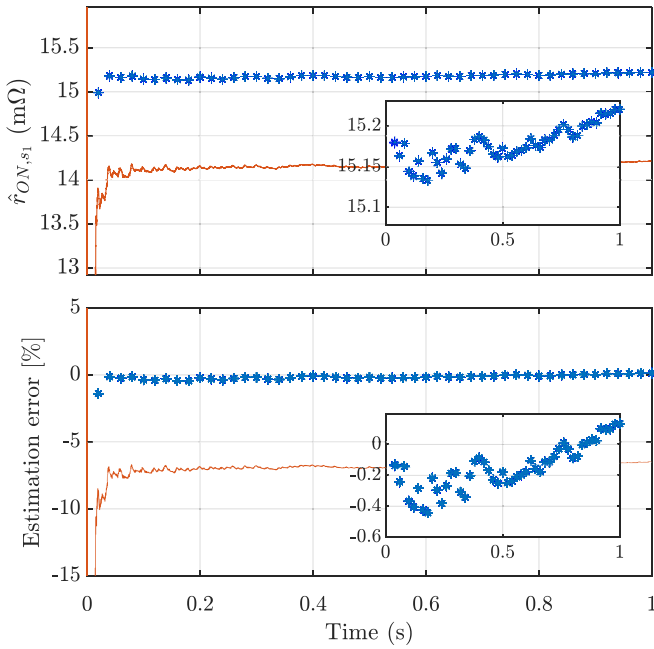


FIGURE 16. Estimated ON-state resistance of the IRFP4768 MOSFET in the experimental setup using RLS (red), and SHE (blue \star) estimation methods when Gaussian noise with standard deviations of $\sigma_v = 0.3$ V and $\sigma_i = 3$ A is artificially added to the measurements.

the online estimation, the SUT is first brought back to the same temperature at which the curve tracing was conducted. The estimation technique is also conducted immediately after starting the converter's operation in order to minimize the effect of internal heating on the estimated values. The experiment is repeated by introducing additional noise to the measurements. That is, the voltage and load current measurements are distorted with a Gaussian noise of $V_{DS,n} \sim \mathcal{N}(0, 0.3^2)$ V and $I_{L,n} \sim \mathcal{N}(0.0, 3.5^2)$ A, respectively. The estimation results under these conditions are shown in Fig. 16, where the RLS method has over 6% error, while the proposed SHE method remains accurate and provides estimations with less than 1% error. In the following sections, the robustness of the proposed SHE method is verified under different foreseeable conditions of operation. That is, the efficacy of the proposed solution is verified under dynamic load conditions, different switching frequencies, and different temperatures of the SUT.

1) EFFECT OF DIFFERENT SWITCHING FREQUENCIES

The estimation results are repeated for different switching frequencies of 5.11 and 10.11 kHz and plotted in Figs. 17 and 18, respectively. In all cases, the SHE method is accurate to an error of less than 1%. Hence, the proposed estimation algorithm is not sensitive to the presented range of switching frequencies. Although the suitability of DM-MOSFET-based measurement circuits is verified for much higher switching frequencies [16], the bandwidth of the measurement circuit used in this study has been deliberately limited. This is because the measurement circuit of this study

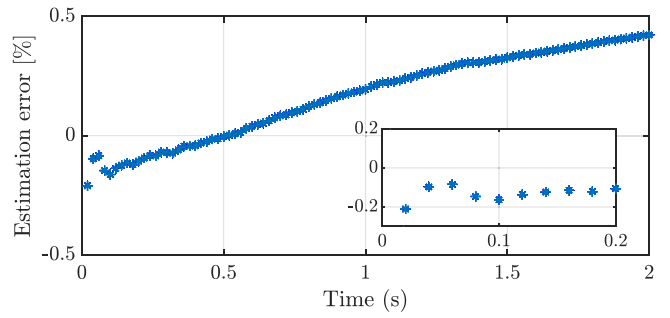


FIGURE 17. Estimated ON-state resistance of the IRFP4768 MOSFET at $f_{sw} = 5.11$ kHz, and using the SHE method.

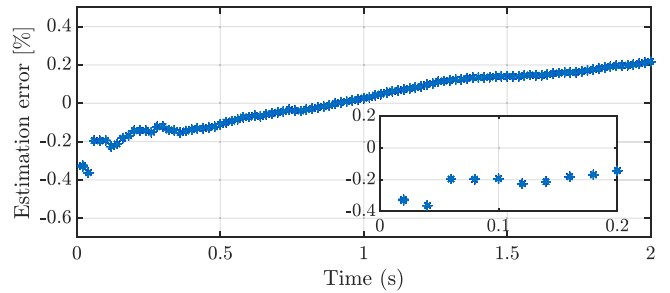


FIGURE 18. Estimated ON-state resistance of the IRFP4768 MOSFET at $f_{sw} = 10.11$ kHz, and using the SHE method.

has been designed for modular multilevel converter cells where switching frequencies much lower than 10 kHz are needed. Hence, although the proposed estimation algorithms are suitable for a wide range of switching frequencies, for very high switching frequencies, bandwidth limitations of the protection stage in Fig. 3 as well as the analog-to-digital converter must be considered.

2) EFFECT OF VARIABLE LOAD

So far, the proposed estimation technique has been verified for constant load conditions. However, this is not a requirement for accurate estimations. In Fig. 19, the estimation technique has been applied to a semiconductor under variable load conditions. Even though the load changes every 100 ms, the SHE method is able to identify the ON-state resistance accurately. Hence, the proposed method is also suitable for converters under variable load conditions. In many converter applications, the load is constantly changing. For example, in STATCOMs used for flicker mitigation caused by industrial loads such as electric arc furnaces, the load is constantly varying [34]. Hence, even if fast updates of the condition monitoring data are not needed, it is important to show that the estimations are not negatively affected by the load. This experiment also proves that the estimation method remains accurate during low-load conditions when the signal-to-noise ratio is relatively lower.

3) MEASUREMENT UNDER DIFFERENT TEMPERATURES

It is shown thus far that the estimation method presented in this article can successfully identify the ON-state resistance

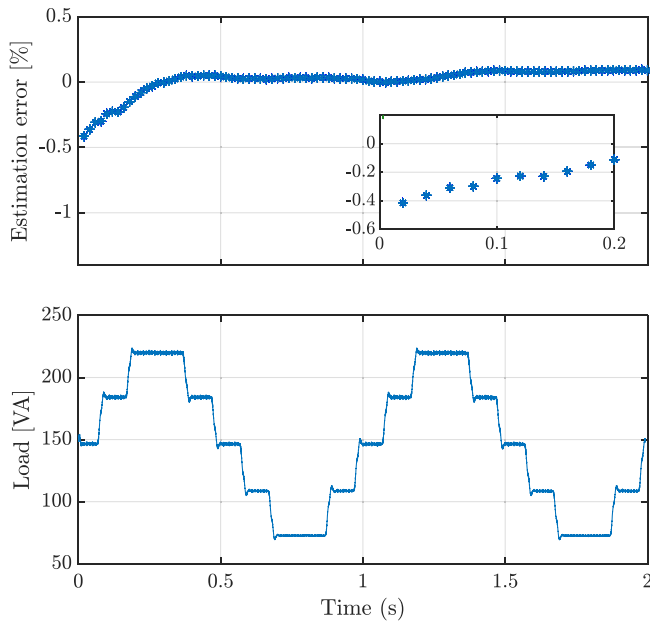


FIGURE 19. Estimated ON-state resistance of the IRFP4768 MOSFET under variable load conditions, and using the SHE method.

TABLE 3. Estimation errors at different temperatures of the SUT and when the system is operated with the parameters of Table 2. The results are sampled after 0.5 s of estimation.

Temperature of SUT [°C]	Offline measurement [mΩ]	SHE Error [%]
30	16.1	0.62
40	17.6	0.06
50	19.3	0.31
60	20.9	0.67
70	22.9	0.04
80	24.8	0.40
90	27.0	0.55

under various operations of the converter. In online operation, the temperature of the semiconductors is expected to vary. This, in turn, changes the value of the ON-state resistance. Since the ON-state resistance is typically used for temperature estimations and health indication of the device, it is important to accurately track it at different temperatures. The SUT is curve traced under seven different temperatures using the Tektronix 371A. The curves are plotted in Fig. 20, and the extracted ON-state resistance from these offline measurements is summarized in Table 3. The heating is conducted using a thermal plate, and the temperature recordings are made using a T-type thermocouple placed between the SUT and its heat sink. The thermocouple and the SUT are galvanically isolated using a thin thermally conductive electrical insulator. The temperature monitoring and logging are carried out using the Picolog TC-08. The accuracy of the thermocouple used for temperature logging is ± 0.5 °C.

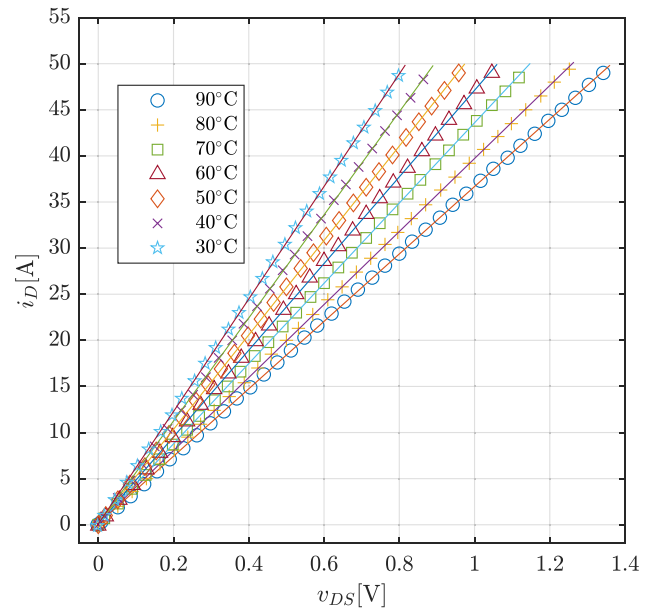


FIGURE 20. Measured $v_{DS}-i_D$ curve of the IRFP4768 MOSFET using the Tektronix 371A curve tracer at different temperatures of the SUT, and while $v_{GS} = 15$ V. The slopes of the linear fits, which indicate the ON-state resistance, are summarized in Table 3.

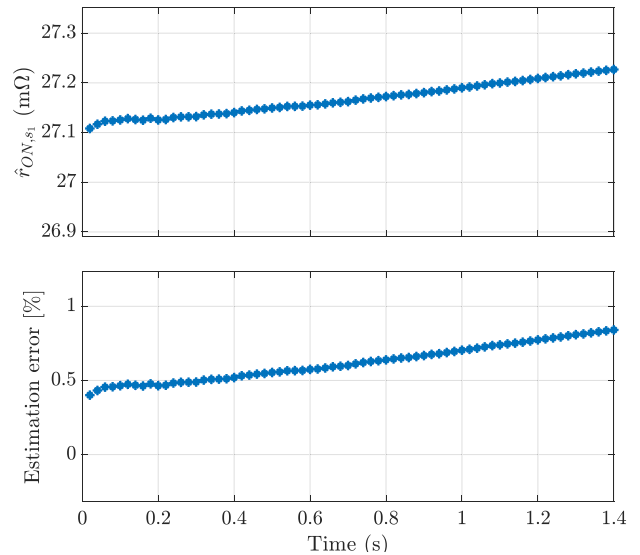


FIGURE 21. Estimated ON-state resistance of the IRFP4768 MOSFET in the forward conduction path, at $T = 90$ °C, and using the SHE method.

The online estimation of ON-state resistance is conducted at different temperatures of the SUT. That is, the SUT is heated, and the parameter estimation is conducted at the same temperature levels as those used in the offline measurements of Fig. 20. As an example, the output of the SHE method for the forward conduction path, and for when the SUT is at 90 °C is shown in Fig. 21. The estimation results for all temperatures are summarized in Table 3. In this table, the estimated values are taken after 0.5 s of estimation, which corresponds to 25 fundamental periods. It is observed that at all temperatures, the estimation error is still within the 1% range.

VI. CONCLUSION

In this article, a novel method for accurate online identification of semiconductor ON-state resistance is presented. The proposed solution consists of a frequency-based estimation technique. An analytical proof is provided showing that both the conduction current and ON-state voltage of the semiconductor under test (SUT) contain a fundamental frequency content. Hence, the proposed method can continuously and repeatedly estimate the ON-state resistance using the extracted frequency content of these voltage and current measurements. The main advantage of the proposed solution is its ability to provide accurate estimations even in extremely noisy environments, under variable load conditions, and in different temperatures of the SUT. These are all the foreseeable conditions for a power electronics system in normal operation; hence, the proposed solution is robust. A detailed comparison of online estimations and offline measurements from a commercial curve tracer has been provided, where the offline measurements are used as reference values in this comparison. It is shown that in the presence of small noise levels, both the proposed SHE and the recursive least-square (RLS) estimation methods provide accurate estimations. However, under extreme noise levels, the RLS estimation method suffers from low accuracy, while the SHE method provides reliable estimations. The efficacy of the proposed SHE method is verified through simulations, and on a hardware prototype. Moreover, the advantage of the SHE method under noisy conditions is explained analytically. In all experiments, the SHE method consistently achieves an estimation error of less than 1%. Hence, the proposed technique is suitable for online condition monitoring of semiconductor devices.

REFERENCES

- [1] S. Chen, S. Ji, L. Pan, C. Liu, and L. Zhu, "An ON-state voltage calculation scheme of MMC submodule IGBT," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7996–8007, Aug. 2019.
- [2] F. Yang, E. Ugur, and B. Akin, "Evaluation of aging's effect on temperature-sensitive electrical parameters in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6315–6331, Jun. 2020.
- [3] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A new complete condition monitoring method for SiC power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1654–1664, Feb. 2021.
- [4] M. A. Eleffendi and C. M. Johnson, "In-service diagnostics for wire-bond lift-off and solder fatigue of power semiconductor packages," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7187–7198, Sep. 2017.
- [5] V. Smet, F. Forest, J.-J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of V_{ce} monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2760–2770, Jul. 2013.
- [6] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by Thermo-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.
- [7] F. Hosseinabadi et al., "Implementation of onsite junction temperature estimation for a SiC MOSFET module for condition monitoring," in *Proc. 24th Eur. Conf. Power Electron. Appl. (EPE)*, 2022, pp. 1–6.
- [8] M. Guacci, D. Bortis, and J. W. Kolar, "On-state voltage measurement of fast switching power semiconductors," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 2, pp. 163–176, Jun. 2018.
- [9] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2531–2551, Mar. 2018.
- [10] "ECPE guideline AQG 324—Qualification of power modules for use in power electronics converter units in motor vehicles," presented at ECPE Eur. Center Power Electron., Nuremberg, Germany, 2021.
- [11] F. Yang, E. Ugur, and B. Akin, "Design methodology of DC power cycling test setup for SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4144–4159, Dec. 2020.
- [12] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, "Degradation assessment and precursor identification for SiC MOSFETs under high temp cycling," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2858–2867, May 2019.
- [13] A. Abuelnaga, M. Narimani, and A. S. Bahman, "A review on IGBT module failure modes and lifetime testing," *IEEE Access*, vol. 9, pp. 9643–9663, 2021.
- [14] S. Baba, A. Gieraltowski, M. Jasinski, F. Blaabjerg, A. S. Bahman, and M. Zelechowski, "Active power cycling test bench for SiC power MOSFETs—Principles, design, and implementation," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2661–2675, Mar. 2021.
- [15] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Developing a standardized method for measuring and quantifying dynamic on-state resistance via a survey of low voltage GaN HEMTs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2018, pp. 2717–2724.
- [16] K. Li, A. Videt, N. Idir, P. L. Evans, and C. M. Johnson, "Accurate measurement of dynamic on-state resistances of GaN devices under reverse and forward conduction in high frequency power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9650–9660, Sep. 2020.
- [17] L. Rossetto and G. Spiazzi, "A fast ON-state voltage measurement circuit for power devices Characterization," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 4926–4930, May 2022.
- [18] S. Bezkowski, P. Ghimre, A. R. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online Vce measurement method for wear-out monitoring of high power IGBT modules," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, 2013, pp. 1–7.
- [19] F. Stella, G. Pellegrino, E. Armando, and D. Daprà, "Online junction temperature estimation of SiC power MOSFETs through on-state voltage mapping," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3453–3462, Jul. 2018.
- [20] J. V. M. Farias, L. Camurca, and M. Liserre, "Development of a VCE-measurement board for medium-voltage modular multilevel converter," in *Proc. Int. Exhibit. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2023, pp. 1–6.
- [21] Y. Peng and H. Wang, "A simplified on-state voltage measurement circuit for power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10993–10997, Oct. 2021.
- [22] Y. Peng and H. Wang, "A self-power method for a converter-level ON-state voltage measurement concept," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8743–8751, Aug. 2021.
- [23] M. Asoodar, M. Nahalparvari, Y. Zhang, C. Danielsson, H.-P. Nee, and F. Blaabjerg, "Accurate condition monitoring of semiconductor devices in cascaded H-bridge modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3870–3884, Mar. 2023.
- [24] M. Tsukuda, L. Guan, K. Watanabe, H. Yamaguchi, K. Takao, and I. Omura, "V-I curve based condition monitoring system for power devices," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2020, pp. 82–85.
- [25] P. Liu, C. Chen, X. Zhang, and S. Huang, "Online junction temperature estimation method for SiC modules with built-in NTC sensor," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 94–99, Mar. 2019.
- [26] H. Higa, T. Hayashi, M. Takiguchi, S. Urushibata, and Y. Tadano, "On-line junction temperature estimation method of power device with deterioration based on on-state voltage measurement," in *Proc. Int. Power Electron. Conf. (IPEC)*, 2022, pp. 447–452.
- [27] M. Schubert and R. W. D. Doncker, "Semiconductor temperature and condition monitoring using gate-driver-integrated inverter output voltage measurement," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2894–2902, May 2020.
- [28] B. T. Vankayalapati, M. Farhadi, R. Sajadi, B. Akin, and H. Tan, "A practical switch condition monitoring solution for SiC traction inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 2190–2202, Apr. 2023.
- [29] M. Yun et al., "Aging and sintered layer defect detection of discrete MOSFETs using frequency domain reflectometry associated with parasitic resistance," *IEEE Trans. Device Mater. Rel.*, vol. 24, no. 1, pp. 129–141, Mar. 2024.

- [30] F. Karakaya, A. Maheshwari, A. Banerjee, and J. S. Donnal, "An approach for online estimation of on-state resistance in SiC MOSFETs without current measurement," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11463–11473, Sep. 2023.
- [31] K. M. Barón, M. C. J. Weiser, K. Sharma, and I. Kallfass, "Analysis of a transistor-based on-state voltage measurement circuit for condition monitoring of power transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2023, pp. 2556–2562.
- [32] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, vol. 18. Hoboken, NJ, USA: Wiley, 2003.
- [33] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 268–283, Jan. 2015.
- [34] H. Zhang, L. Ängquist, S. Norrga, H.-P. Nee, and S. Östlund, "Benchmark of high-power STATCOM topologies for flicker compensation," in *Proc. 18th Eur. Conf. Power Electron. Appl. (ECCE)*, 2016, pp. 1–10.



IMAN SHAFIKHANI received the Ph.D. degree in electrical engineering, specializing in vehicular systems, from Linköping University, Linköping, Sweden, in 2021.

He currently works as a Data Scientist with Scania Group, Södertälje, Sweden, where he focuses on developing machine learning solutions for various applications.



MOHSEN ASODAR (Student Member, IEEE) received the M.Sc. degree in electrical engineering from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2014.

In 2014, he joined ABB's Corporate Research Center, Västerås, Sweden, as a Research Scientist. Later, he served as a Research and Development Engineer with ABB FACTS, Västerås. He is currently working with Hitachi Energy, Västerås, as a Senior Research and Development Engineer and conducting his industrial Ph.D. studies in

collaboration with the KTH Royal Institute of Technology. His research interests include the design, control, and grid integration of power electronic systems.



GUNNAR INGESTRÖM received the M.Sc. degree in physics from Linköping University, Linköping, Sweden, in 1992.

He joined ABB (formerly, ASEA), Västerås, Sweden, in 1986, where he worked with system design of static VAR compensators and series capacitors, as well as the development of thyristor-controlled series compensators and protection equipment. During the last 20 years, he has been involved in standardization activities and is currently the Chair of IEC TC33. He is currently

working with Hitachi Energy, Västerås, as a Senior Principal Research and Development Engineer with a focus on the development of STATCOMs and energy storage solutions.



MEHRDAD NAHALPARVARI (Student Member, IEEE) received the M.Sc. degree in power electronics from Tampere University, Tampere, Finland, in 2019. He is currently pursuing the Ph.D. degree in electrical engineering with the KTH Royal Institute of Technology, Stockholm, Sweden.

His research interests include modeling and control of power electronic converters.



SIMON SCHNEIDER received the M.Sc. degree in electric power engineering from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2022.

He joined Volvo Cars Corporation, Gothenburg, Sweden, in 2022 as a Motor Controls Software Developer for Traction Inverters.



HANS-PETER NEE (Fellow, IEEE) was born in Västerås, Sweden, in 1963. He received the M.Sc., Licentiate, and Ph.D. degrees in electrical engineering from the Royal Institute of Technology (KTH), Stockholm, Sweden, in 1987, 1992, and 1996, respectively.

Since 1999, he has been a Professor of Power Electronics with the Department of Electrical Engineering, KTH. His research interests include power electronic converters, semiconductor components, and control aspects of utility applications, such as flexible ac transmission systems and high-voltage direct-current transmission, and variable-speed drives.

Dr. Nee was a member of the Board of the IEEE Sweden Section for many years and was the Chair of the Board from 2002 to 2003. He is also a member of the European Power Electronics and Drives Association and is involved with its Executive Council and International Scientific Committee.