# Materials Integration for Printed Zinc Oxide Thin-Film Transistors: Engineering of a Fully-Printed Semiconductor/Contact Scheme

Xinxin Liu, Moritz Wegener, Sebastian Polster, Michael P. M. Jank, Andreas Roosen, and Lothar Frey

*Abstract—***We report for the first time on the impact of a printed indium tin oxide (ITO) layer inserted between a printed silver conductor and solution processed zinc oxide (ZnO) leading to an optimized semiconductor/contact scheme for full print integration. Introducing the ITO interlayer, the contact resistance is reduced by two orders of magnitude. Nanoparticle thin-film transistors (TFTs) in this Ag/ITO contact configuration show improved saturation** mobility of 0.53 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  s<sup>-1</sup> with respect to 0.08 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  $s^{-1}$  without ITO interlayer. The contact improvement can be at**tributed to either an increased charge carrier concentration or a reduction of band offsets at the ZnO/electrode interface.**

*Index Terms—***Contact resistance, indium–tin–oxide, thin-film transistors (TFTs), zinc oxide (ZnO).**

#### I. INTRODUCTION

**T** HIN-FILM transistors (TFTs) based on metal oxide semiconductors have drawn increasing interest recently due to their high electron mobility, high  $I_{on}/I_{off}$  ratio, optical transparency, and applicability to low temperature and low cost solution processing. Dedicated ink formulation and conversion routes enable the processing of low-viscosity nanoparticle suspensions into thin semiconducting films, most likely by spin coating and inkjet printing [1]. Poor interface and morphological quality of dispersion processed nanoparticle thin films can be addressed by adequate process optimization [2]–[4]. However, nearly all publications on "printable" metal oxide TFTs only address the development of single, solution processible semiconductor layers, which typically are integrated with conventionally processed insulators from thermal oxidation as well

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X. Liu, S. Polster, and L. Frey are with the Chair of Electron Devices, University of Erlangen-Nuremberg, Erlangen, Germany (e-mail: xinxin.liu@leb. eei.uni-erlangen.de).

M. Wegener and A. Roosen are with the Chair of Glass and Ceramics, University of Erlangen-Nuremberg, Erlangen, Germany.

M. P. M. Jank and L. Frey are with the Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany.

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as gate and source/drain electrodes from CVD or PVD techniques. Only very few work in this field concentrates on the development of devices or device features that integrate two or more printable materials [5].

Restriction to all-printable materials is essentially critical in the source/drain region of the device. Whereas a broad range of metals can be accessed for optimization of metal-semiconductor contacts by PVD [6], only silver and, with more elaborate and expensive processing schemes, copper and aluminum are available for print integration. Silver however typically forms significant energy barriers at the metal/zinc oxide contact which are deteriorating the device performance with respect to current drivability [5].

An improvement of the contacts can be achieved by either using surface preparation to reduce the metal semiconductor barrier height to increase carrier injection probability or by engineering the charge carrier concentration of the semiconductor at the interface [7]. Ho *et al.* used a co-sputtered ITO-ZnO film as electrode to the n-type ZnO layer and achieved an optimization of contact resistance due to the outdiffusion of the oxygen atoms from the ZnO layer at the interface [8].

In this work, we develop an ink jet printing process for ZnO semiconductor films starting from a ZnO nanoparticle formulation optimized for spin-coating. The morphological, as well as electrical, properties of spin-coated and printed ZnO layers are compared. Furthermore, an inkjet printed indium–tin–oxide interlayer between zinc oxide and the Ag layer is introduced to reduce the contact resistance at the metal/semiconductor interfaces and the contact resistances between semiconductor layer and electrodes with and without ITO interlayer are determined. The insertion of an ITO interlayer results in the reduction of contact resistance by two orders of magnitude and the improvement of the electrical characteristics of thin-film transistors (TFTs).

#### II. EXPERIMENT

The ZnO ink was based on a ZnO nanoparticle powder (Evonik Industries AG, Essen, Germany) with a primary particle size of 20 nm. The ZnO suspension in ethanol was dispersed with a disperser DAS H 200-K (LAU GmbH, Hemer, Germany) using yttrium stabilized zirconia milling beads. The dispersion has a content of 20 wt.% ZnO and was stabilized by 2-[2-(2-methoxyethoxy)ethoxy]acetic acid [trioxadecanoic acid (TODA)]. In order to remove larger nanoparticle aggregates and agglomerates, the ZnO suspension was centrifuged in a 3K30 centrifuge (SIGMA Laborzentrifugen GmbH, Osterode am Harz, Germany) at 20000 rpm for 2 min. The supernatant was extracted and used as ink of 3 wt.% for spin-coating. For

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Fig. 1. Schematic device structure of the staggered ZnO TFTs with: (a) and without (b) ITO interlayer.

inkjet printing, the ZnO suspension was diluted in 50 vol.% distilled water and 50 vol.% ethylene glycol (Bernd Kraft GmbH, Duisburg, Germany) with regard to the volume of the ZnO suspension in order to achieve good printing performance [1], [2], [9].

The ITO ink (0.5 wt.%) was based on a nano-sized indium tin oxide powder (Evonik Industries AG, Essen, Germany) with a primary particle size of 19 nm (determined by BET measurements, ASAP 2000, Micromeritics Instrument Corp., Norcross, GA, USA), a carboxylic acid based dispersing agent (Sigma Aldrich, Milwaukee, WI, USA) and a solvent mixture consisting of 70 wt.% bi-distilled water, 15 wt.% ethanol and 15 wt.% ethylene glycol (both: VWR International GmbH, Darmstadt, Germany). This solvent mixture provides good printing performance and homogeneous structure formation upon drying. The ink had a solid content of 2 vol.% [10]. The ITO powder, the solvent mixture, and the dispersing agent were combined in a PE bottle for the dispersing procedure. The dispersing step was done in a tumbling mixer (Turbula, Willy A. Bachofen AG, Basel, Switzerland) for 72 h. Yttrium-stabilized zirconia milling balls (YTZ Grinding Media, Nikkato Corp., Japan) of 1.0 mm in diameter were added to induce shear forces during the dispersing step. The ITO ink exhibited a mean agglomerate size (x50.3 value) of around 90 nm, a viscosity of 4 mPas and a surface tension of 38 mN/m.

Fig. 1 shows a schematic cross section of the staggered bottom-gate ZnO TFTs with (a) and without (b) ITO interlayer. ZnO was spin-coated or inkjet printed onto a Si substrate, where the  $p^+$ -doped Si Wafer and 200 nm of SiO<sub>2</sub> function as gate electrode and gate insulator. After annealing at  $400\degree C$  for 30 min in air, ITO ( $t \approx 500$  nm) was inkjet printed on top of the ZnO layer ( $t \approx 50$  nm) and annealed again at 400 °C for 30 min in air for the TFTs with ITO interlayer. Finally, silver source and drain electrodes with a thickness of around 170 nm were ink-jet printed (Sun Tronic Jet Silver U5603) either on top of the ITO layer or directly on top of the ZnO layer. A few reference samples received a 100 nm-thick Al layer by electron-beam evaporation which was deposited at an evaporation rate of 0.2 nm/s. Patterning was achieved through a shadow mask in this approach. The electrical characteristics of TFTs were measured at room temperature with a Precision Semiconductor Parameter Analyzer 4156C (Agilent) in ambient conditions or with two Keithley 2636 Dual Channel Source Meters in  $N_2$  atmosphere.



Fig. 2. SEM top views and cross sections of spin-coated (a) and printed ZnO films. Printed ZnO after ink-jet deposition in 1 (b), 2 (c), or 3 (d) passes [13].

To investigate the contact resistance between the source and drain electrode stacks and the ZnO layer, the transfer length method (TLM) was applied [11], [12]. The TLM samples were prepared on insulating glass substrates (1737F, Praezisions Glas & Optik GmbH, Iserlohn, Germany) to rule out gate-induced effects. The electrical characterization was again conducted in  $N_2$  atmosphere.

# III. RESULTS AND DISCUSSION

# *A. Morphological Optimization and Electrical Characterization of Ink-Jet Printed ZnO Thin Films*

The ink-jetting process for the semiconductor was optimized and compared against the spin-coated reference aiming simultaneously at a densely packed film for good percolation, smooth interface to the insulator for good gate control, and a low film thickness for suppression of bulk leakage. Fig. 2 shows top views and cross sections of spin-coated (a) and printed ZnO layers (b)–(d). A single printed film (b) is not fully covering the surface, whereas layers deposited by two (c) or three (d) passes show a projected packing density comparable to that of the spincoated film. The cross section insets reveal the formation of a smooth interface with the insulator and an increasing surface roughness with increasing number of ink-jet passes. Films printed with two passes roughly deliver the same thickness as spin-coated layers derived from the spin-coating formulation that has twice the solids content.

Fig. 3 shows transfer characteristics of TFTs based on spincoated ZnO (a) and two times printed ZnO (b) with evaporated Al electrodes. Top views of the TFTs taken by an optical microscope are shown in the insets. The channel length and width of the TFTs were 80  $\mu$ m and 2000  $\mu$ m respectively. Ink-jet printed ZnO thin films from the modified nanoparticle dispersion can reach TFT performance of spin-coated layers from the same starting material. Current levels of 10  $\mu$ A at a  $W/L$  ratio of 25 and gate overdrive of 30 V as well as  $I_{ON}/I_{OFF}$  ratios exceeding  $10<sup>4</sup>$  can be reached. The off-state current of printed ZnO TFTs is significantly improved due to a reduction of the leakage current to the gate electrode by the directly patterned



Fig. 3. Transfer characteristics of TFTs based on spin-coated ZnO (a) and ink-jet printed ZnO (b) with evaporated Al electrodes. Both samples were measured in ambient conditions.



Fig. 4. TLM-structure with (a) and without (b) ITO interlayer [Schematic representation is found in Fig. 1(a) and (b)]. Dashed white line represents the boundary of the ITO layer.

semiconductor. A similar level of saturation charge-carrier mobility (0.03 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  s<sup>-1</sup> of TFTs based on printed ZnO versus  $0.07 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  of TFTs based on spin-coated ZnO) can be achieved.

# *B. Reduction in Contact Resistance of ZnO TFTs by Using a Printed ITO Interlayer*

The formation of fully printed metal–ZnO contacts by ink-jet deposition of silver has several structural and electrical implications. While adhesion problems [5] are partly compensated by the rough surface in our samples, the high work function of Ag [8] as well as thus far only fairly controllable interface charge states (Fermi-level pinning) can lead to barriers for the electron injection at the Ag/ZnO interface. For experimental evaluation we compare directly printed Ag contacts against a work function engineering scheme by introduction of an interfacing layer. An ink-jet printed ITO layer is inserted between the spin-coated ZnO layer and the printed Ag layers (Fig. 4). This approach only makes use of the thin vertical extension of the ITO film. Although offering a large electron density with respect to the ZnO, the ITO interface layer cannot be applied for the preparation of laterally conducting lines since a sufficient sheet resistance can only be achieved upon laser annealing the ITO nanoparticle film [14], which, however, is not compatible to the previously deposited ZnO [9].

A TLM analysis of the samples prepared on insulating substrate is performed with two different line widths.  $I_D/V_D$  data are evaluated for different transfer lengths to determine the total resistance  $R_{\text{tot}}$ . Fig. 5 shows the normalized total resistance  $(R_{\text{tot}} \times W)$  as a function of the contact distance. The TLM structure with the ITO interlayer yields a contact resistance of  $102 \text{ k}\Omega$  for 2 mm line width. This is 2 orders of magnitude lower than for the TLM structure without the ITO interlayer yielding 12.1 M $\Omega$  for the same width. The weak dependence on the transfer length in Fig. 5(b) furthermore shows that with



Fig. 5. Contact resistance determined by using the TLM with: (a) and without (b) ITO-interlayer.

using an Ag only contact approach, the total resistance is clearly dominated by the contact resistance, even for the 500  $\mu$ m long resistors and in non-gated condition. The contact resistances for half of the line width roughly double, i.e., 281 k $\Omega$  for Ag/ITO and and 27.3 M $\Omega$  for Ag-only contacts, which proves the concept of Ag (global) conducting lines with an (local) ITO interlayer for contact engineering.

Based on the available results a number of reasons are considered for the improved contact resistance of TLM structures with Ag/ITO stack. Although the ITO layer should further roughen the surface, the 2 orders of magnitude improvement cannot only be attributed to structural effects. The reduction of the contact resistance is most likely attributed to the formation of localized interface states [15] leading to an increased interfacial charge carrier concentration in the ZnO [16] or the lowering of band offsets. More elaborate test structures and  $I-V$  techniques will give a deeper insight into the interface physics in the future. The out-diffusion of the oxygen atoms at the n-type ZnO layer surface and formation of oxygen vacancies near the ZnO surface observed by Ho *et al.* for sputtered layers [8] is not as likely because the nanoparticle layers are open to in-diffusion



Fig. 6. Transfer characteristics of TFTs based on spin-coated ZnO and printed Ag with (a) and without (b) ITO interlayer (measured in  $N_2$  atmosphere).

of oxygen-containing species that would compensate for this effect [8].

TFTs based on spin-coated ZnO with and without ITO interlayer were fabricated on  $SiO<sub>2</sub>/Si$  substrate. The transfer characteristics (Fig. 6) show that TFTs without ITO interlayer typically have current level of 10  $\mu$ A at a  $W/L$  of 25 and gate overdrive of 30 V as well as a saturation charge carrier mobility of  $0.08 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ , while TFT with ITO interlayer at identical boundary conditions reach a current level of 100  $\mu$ A and a saturation charge carrier mobility of 0.53 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  s<sup>-1</sup>.

The effective mobility in the linear regime was improved from 0.08 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  s<sup>-1</sup> to 0.4 cm<sup>2</sup>  $\cdot$  V<sup>-1</sup>  $\cdot$  s<sup>-1</sup>, which is attributed to the reduction of the contact resistance when using the ITO interlayer.  $I_{ON}/I_{OFF}$  ratios exceeding  $10^3$  were achieved. The increased overlap area between the ITO contacts and the gate [Figs.  $1(a)$  and  $4(a)$ ] results in a higher leakage current in the off state. The threshold voltage was shifted from 2.6 to  $-5.89$  V when introducing the ITO interlayer due to the higher thermal budget. The ZnO layer in the ITO contacted samples were annealed two times for 30 min at 400  $^{\circ}$ C in air. The device structure of spin-coated ZnO TFTs with unpatterned semiconductor (Fig. 1) results in high gate leakage currents. In the silver S/D configurations, the gate leakage current dominates over the drain current at low drain voltages [Fig. 6(b)]. Due to the strongly increased ON currents in ITO contacted TFTs, gate leakage is not an issue in the optimized devices.

# IV. CONCLUSION

TFTs based on printed ZnO thin films from nanoparticle dispersions can reach TFT performance of spin-coated layers from the same base material after morphological optimization. The insertion of an ITO interlayer for the source and drain contacts can reduce the contact resistance in ZnO TFTs contacted by silver electrodes. Carrier accumulation at the ZnO/ITO interface or the reduction of band offsets are the most likely explanations for the reduction of the contact resistance by two orders of magnitude. Contact engineering leads to a performance improvement of TFTs with a printed semiconductor-metal contact scheme. ZnO nanoparticle TFTs with printed Ag/ITO contacts reach saturation mobilities of 0.53 cm<sup>2</sup>/V · s at  $I_{ON}/I_{OFF}$  ratios of  $10^4$ .

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#### **REFERENCES**

- [1] S. Walther *et al.*, "Influence of annealing temperature and measurement ambient on TFTs based on gas phase synthesized ZnO nanoparticles," *Microelectron. Eng.*, vol. 87, pp. 2312–2316, 2010.
- [2] S. Walther, S. Polster, B. Meyer, M. P. M. Jank, H. Ryssel, and L. Frey, "Properties of SiO2 and Si3N4 as gate dielectrics for printed ZnO transistors," *J. Vac. Sci. Technol., B*, vol. 29, pp. 01A601-1–6, 2011.
- [3] K. Okamura, N. Mechau, D. Nikolova, and H. Hahn, "Influence of interface roughness on the performance of nanoparticulate oxide field-effect transistors," *J. Appl. Phys.*, vol. 93, pp. 083105-1–3, 2008.
- [4] B. Sun and H. Sirringhaus, "Solution-processed zinc oxide field-effect transistors based on self-assembly of colloidal nanorods," *Nano Lett.*, vol. 5, pp. 2408–2413, 2005.
- [5] Y.-J. Kwack and Y.-S. Choi, "Screen-printed source-drain electrodes for a solution-processed zinc-tin-oxide thin-film transistor," *J. Kor. Phys. Soc.*, vol. 56, pp. 3410–3414, 2011.
- [6] E. Fortunato *et al.*, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, pp. 2945–2986, 2012.
- [7] J.-H. Lim and S.-J. Park, "Contacts to ZnO," in *Zinc Oxide Bulk, Thin films and Nanostructures : Processing, Properties, and Applications*, C. Jagadish and S. J. Pearton, Eds., 1st ed. New York, NY, USA: Elsevier Science, 2006, pp. 267–283.
- [8] C.-C. Ho, L.-W. Lai, C.-T. Lee, K.-C. Yang, B.-T. Lai, and D.-S. Liu, "Transparent cosputtered ITO–ZnO electrode ohmic contact to n-type ZnO for ZnO/GaN heterojunction light-emitting diode," *J. Phys. D: Appl. Phys.*, vol. 46, pp. 315102-1–7, 2013.
- [9] M. Baum, S. Polster, M. P. M. Jank, I. Alexeev, L. Frey, and M. Schmidt, "Efficient laser induced consolidation of nanoparticulate ZnO thin films with reduced thermal budget," *Appl. Phys. A.*, vol. 107, pp. 269–273, 2012.
- [10] N. Kölpin, M. Wegener, E. Teuber, S. Polster, L. Frey, and A. Roosen, "Conceptional design of nano-particulate ITO inks for inkjet printing of electron devices," *J. Mater Sci*, vol. 48, pp. 1623–1631, 2013.
- [11] D. Schroder*, Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006, pp. 127–184.
- [12] Y. Xu, R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra, and G. Ghibaudo, "Modified transmission-line method for contact resistance extraction in organic field-effect transistors," *Appl. Phys. Lett.*, vol. 97, pp. 063302-1–3, 2010.
- [13] X. Liu *et al.*, "Reduction in contact resistance of ZnO thin-film transistors by insertion of an indium tin oxide interlayer," in *ITC 2015 Abstracts*, Rennes, France, 2015, pp. 69–70.
- [14] M. Baum, I. Alexeev, and M. Schmidt, "Laser treatment of ITO and ZnO nanoparticles for the production of thin conducting layers on transparent substrates," *J. Laser Micro/Nanoeng.*, vol. 6, pp. 191–194, 2011.
- [15] L. Brillson and Y. Lu, "ZnO Schottky barriers and ohmic contacts," *J. Appl. Phys.*, vol. 109, pp. 121301-1–33, 2011.
- [16] J.-H. Bae, W.-H. Kim, C.-. J. Yu, and S.-D. Lee, "Reduction in contact resistance of pentacene thin-film transistors by formation of an organometal hybrid interlayer," *Jpn. J. Appl. Phys.*, vol. 48, pp. 020209-1–3, 2009.



**Xinxin Liu** received the B.S. degree in chemistry with marketing from both Reutlingen University, Reutlingen, Germany, and Donghua University, Shanghai, China in 2009, the M.S. degree in material science from Friedrich-Alexander-University of Erlangen-Nuremberg (FAU), Erlangen, Germany, in 2011, and is currently working toward the Ph.D. degree from the Chair of Electron Devices at FAU.

Her current research interests include ZnO/GIZO thin-film transistors, printed devices, advanced device architectures, logic gates and applications.



**Moritz Wegener** received the B.Sc. degree in materials science in 2010, and the M.Sc. degree (Elite Master's programme of Advanced Materials and Processes) in 2012, from the Friedrich-Alexander-University of Erlangen Nuremberg (FAU) in 2010 and 2012, respectively, and since is working toward the Ph.D. degree under the guidance of Professor Andreas Roosen working in the functional ceramics group in the chair of glass and ceramics at the Materials Science Department of the FAU.

His work focusses on printing and coating techniques of nanoparticulate transparent conductive oxide materials for electronic devices.



**Sebastian Polster** received the diploma degree in materials science from the Friedrich-Alexander-University of Erlangen-Nuremberg (FAU) in 2009, and is currently working towards the Dr.-Ing. degree at the Chair of Electron Devices at FAU.

His current research interests include zinc oxide nanostructures and thin film devices.



**Michael P.M. Jank** received the diploma degree in electrical engineering from the Friedrich-Alexander-University of Erlangen-Nuremberg (FAU) in 1996, and the Dr.-Ing. degree with a thesis on extremely simplified routes to silicon CMOS devices in 2006.

He started his career as a teaching assistant at the Chair of Electron Devices at FAU. Following the Dr.- Ing. degree in 2006, he joined the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, where he is currently heading the thin-film systems group, a joint undertaking with FAU. The

group focuses on large area and printable thin-film electronics and develops materials, processing techniques, and thin-film devices based on of conventional PVD/CVD techniques as well as novel solution based approaches. He holds lectureships for Nanoelectronics and Printed Electronics from the FAU. He is reviewer for reknown international journals and contributes to scientific and industrial working groups on semiconductor memory devices and nanomaterials.



**Andreas Roosen** received the diploma degree in Glass and Ceramics from the Technical University of Berlin, where he also received the Ph.D. degree from the Institute of Nonmetallic-Inorganic Materials in 1984.

After an employment as a research associate at the Federal Institute for Materials Testing (BAM), Berlin, Germany, he was a visiting scientist at the Massachusetts Institute of Technology, Cambridge,MA, USA (Ceramics Processing Research Laboratories) for  $1\frac{1}{2}$  years. In 1986, he joined

the HOECHST AG, Frankfurt (Main), Germany, as an executive employee, heading the group of Functional Ceramics at the Corporate Research Department. Since 1995, he is professor for Glass and Ceramics at the Department of Materials Science of the Friedrich-Alexander-University of Erlangen-Nuremberg (Germany). His research is focused on ceramics colloidal processing, tape casting, ceramic multilayer technology and printed electronics. He is the (co-)author of more than 200 papers and several patent applications.



**Lothar Frey** received the Diploma degree in physics and the Dr. rer. nat. degree from the University Würzburg, Germany, in 1983 and 1987, respectively.

In 1987, he joined Rice University, Houston, for a post-doctorate position working on new laser sources. In 1989, he returned to Germany to the new Fraunhofer AIS, Erlangen, to build up a group on semiconductor characterization. In 1993, he joined the Friedrich-Alexander-University of Erlangen-Nuremberg being responsible for the clean room facility of the university and also heading

the department of silicon technology of the Fraunhofer IISB. During this period, research focused on micro technology for electron devices with special emphasis on ion beam based technologies and the introduction of new materials to silicon technology. In 2005, these activities brought him in to Infineon Technologies (Qimonda) Dresden. Two years later, he became full professor for applied physics at the Technical University Freiberg. Since 2008, he holds the chair of Electron Devices (LEB) at the Friedrich-Alexander-University of Erlangen-Nuremberg and Director of the Fraunhofer Institute of Integrated Systems and Device Technology (IISB), Erlangen. His current activities cover two major research fields: silicon technology for electron devices, and power electronic systems from devices to complete systems.