# Dual-Stage Control Strategy for a Flying Capacitor Converter Based on Model Predictive and Linear Controllers

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***Abstract*—This article proposes a novel dual-stage control strategy for a flying capacitor converter. During transients, the proposed control scheme applies finite-control-set model predictive control to drive the system close to the desired reference, including all the known nonlinearities of the system in the converter model. When the converter state is in a neighborhood of the reference, the dual-stage controller switches to a pulsewidth modulation based linear controller with an integral action. In this case, the linear controller is reformulated in its feedback form. Thus, the internal linear controller states can be updated based on the actual input applied by the predictive controller. This allows the dual-stage controller to achieve a smooth transition when commuting between controllers and a zero-steady-state error even when load parameter errors are present. Experimental results are provided to verify the effectiveness of the proposed dual-stage controller.**

***Index Terms*—Flying capacitor converter (FCC), linear control, model predictive control (MPC).**

## I. Introduction

DURING the last decade, in the field of power electronics several works have proposed and promoted the use of model predictive control (MPC) to govern power converters and electrical drives [1]–[7]. In general, MPC is a control strategy where the input to be applied to the system is optimally determined by solving, at each sampling instant, an optimal control problem, i.e., by minimizing a cost function, which forecasts the tracking error evolution over a finite prediction horizon. MPC strategies can be classified into two major groups according to the nature of control input, $u$ [8].

For linear systems, an explicit solution of the optimal control problem can be obtained. This technique is called explicit-MPC (EMPC). With this approach $u$ is constrained to belong to a continuous control set, e.g., for an $m$-input system, $u \in [-1, 1]^m$. Therefore, a modulator is required to obtain the gate signals for the power converter. Then, in steady state all the benefits of using pulsewidth modulation (PWM) modulators remain. Further details on EMPC can be found in [9].

On the other hand, in direct control-applications, where no modulator is used, $u$ is constrained to belong to a finite control set (FCS) describing, the available switch combinations, e.g., $u \in \{0, 1\}^m$. Such approaches have attracted significant attention in the power electronics community, where it is referred to as FCS-MPC. This control technique is conceptually simple to understand, can deal with nonlinearities, is able to handle multiple control objectives, and provides a fast closed-loop dynamic response. Despite the advantages that FCS-MPC strategies in principle offer, there exist several issues that need to be addressed, as uneven switching distribution, wide spread signals spectra, and nonzero steady-state error [10], [11]. Most of these issues can be overcome by including them as control targets in the cost function [10], [12]–[14]. Nevertheless, this decrements the quality of the main variables since there is a tradeoff among the individual control objectives [15], [16].

To deal with the issues mentioned above, in [17], a switched control strategy based on FCS-MPC and EMPC is proposed. Here, FCS-MPC is used only during transients while EMPC is applied when the system state is near the reference. Therefore, a high dynamic during transients is achieved, since FCS-MPC is used to rapidly drive the system state to a neighborhood of the desired reference. After that, the controller switches to EMPC (along with a PWM) to govern the converter. Thus, a concentrated spectrum in the output signals is obtained during the steady state while even switching losses distribution can also be accomplished. Consequently, a significant improvement in the overall operation of the converter is achieved. The switched predictive control strategy proposed in [17] can also achieve a zero average steady-state error provided that system parameter values are accurately known. This is a naive assumption for real applications where uncertainties in system parameters are always present, due to the fact that nominal parameters are

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subject to errors (within some limits) and some of them might also change in time.

In this article, a bumpless dual-stage predictive controller for power converters, applied to a flying capacitor converter (FCC), is proposed. The FCC presents nonlinearities in the dynamics but that can be locally (near the reference) described by an accurate lineal model. This work is an extension of the preliminary work presented in [18]. Here, the use of FCS-MPC during transients is kept as in [17]. However, in this new approach, a traditional linear controller (TLC) with integral action is used instead of an EMPC scheme. The use of TLCs have all the advantages derived from the use of PWM modulators, additionally TLCs are widely accepted in industrial converters. This allows the proposed dual-control scheme to take advantage of both individual control strategies, achieving a fast transient dynamic and a zero-average error during the steady-state despite some reasonable model uncertainties. The work at hand extends [18] by analyzing in great detail the switching between control strategies, ensuring a smooth switching transition.

Extensive experimental results are provided to verify the closed-loop performance of the proposed dual-stage controller when governing a three-phase three-cell FC converter. Here, a standard proportional-integrative (PI) controller is used as linear controller. To highlight the fact that the proposed dual-control strategy can work with high order controllers that contain an integral action, in Section V, a more complex linear controller comprised of a resonant and a PI controller is also considered for the single-phase case.

## II. Linear and Predictive Control of Power Converters

This section describes the basics of the two control strategies for power converters that will be used to formulate the proposed dual stage controller.

### A. Traditional Linear Controllers

Generally, a power converter can be manipulated by changing the conduction state of its power switches, which can be either in ON-state (closed) or OFF-state (open). Therefore, from a control viewpoint, these power switches are, in fact, *binary* control inputs.

TLCs such as PI and proportional-resonant (PR) controllers are well established solutions to govern linear systems and apply continuous control signals to the system. When considering TLCs to govern power converters, it is required to use the following:

1) a PWM stage to transform the continuous control inputs in equivalent duty-cycles (average switch state) to indirectly manipulate the converter power switches;
2) a lineal average model of the power converter to relate continuous average system input signals (e.g., duty-cycles) with average system output (e.g., fundamental output current).

For control purpose, some power converters can be simply modeled as linear systems, usually a gain connected to a linear load. This leads to a linear dynamic model between the control input (e.g., duty-cycles) and system output (e.g., load current). However, for more complex topologies such as FCC [19] and NPC [20], the system model becomes more involved since it is also required to describe the internal system state dynamics (e.g., capacitor voltages), leading to nonlinear dynamic models. For these topologies, approximated linear system models can be obtained only if these internal states are closed to their references. Nevertheless, when these internal states are far from their references, their effect over the output variable increases, impacting the overall closed-loop performance.

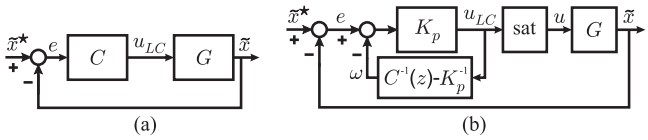


Fig. 1. TLC implementation: (a) standard form and (b) feedback form.

Depending on the topology, it is possible to move the internal states to their references by using an appropriate standard modulation stage [21], or including more sophisticated modulation schemes [22], [23], without any significant effect over the system steady-state performance. In such case, the discrete-time model of the power converter is given by

$$V_o(z) = z^{-1} V_{\text{dc}} \cdot u_{LC}(z) \tag{1}$$

where $V_o(z)$ stands for the converter output voltage, $u_{LC}(z)$ is the control input provided by the controller (e.g., duty cycle), and the single delay corresponds to the sampling delay due to the PWM scheme. Note, however, that (1) not necessarily stands in transient operation.

Generally, a conversion system comprised of a power converter and load has $n$-system states represented by $x$, which includes internal and external variables. By relaying the convergence of the internal states to the modulation stage, a TLC might govern a reduced number of $r$-system states $\tilde{x}(z) = G(z) \cdot u_{LC}(z)$, as shown in Fig. 1(a).

Most of the linear controllers used in industry and literature, such as PI or PR controllers, present a biproper structure. Therefore, they can be rewritten as

$$C(z) = \frac{u_{LC}(z)}{e(z)} = K_p \frac{z^n + \alpha_{n-1} z^{n-1} + \cdots + \alpha_0}{z^n + \beta_{n-1} z^{n-1} + \cdots + \beta_0} \tag{2}$$

where $e[k] = \tilde{x}^\star - \tilde{x}[k]$ is the system tracking error. These are the controller structures considered in this work.

Any biproper structure can be implemented through its feedback form [24], which is shown in Fig. 1(b). This representation is normally used to incorporate a generalized antiwindup strategy by simply saturating the controller output, i.e., $u[k] = \text{sat}(u_{LC}[k])$, where

$$u_{LC}[k] = K_p \left( e[k] - \omega[k] \right). \tag{3}$$

Besides the antiwindup application, the feedback form of the controller can also be used whenever the actual input applied to the plant, $u[k]$, differs from the input provided by the controller $C(z)$, i.e., $u[k] \neq u_{LC}[k]$. In such case, the internal local controller states, $\omega[k]$, can be *updated* according to the actual input,

$u_{[k]}$, applied to the system by using

$$\omega(z) = \left(C^{-1}(z) - K_p^{-1}\right) u(z). \tag{4}$$

This is a key concept that will be used in Section III for the design and implementation of a bumpless dual controller that could be used with any biproper linear controller.

### B. Finite-Control-Set Model Predictive Control

As previously stated, FCS-MPC is a popular predictive control alternative for power converters and electrical drives.

Since in power electronics it is desired to control several variables of different physical nature and order of magnitude, e.g., voltages, currents, power, toque, etc., to evaluate the future behavior of a power converter, a cost function which considers a weighted positive sum of the tracking errors of the controlled variables is required.

As detailed in [25], at the beginning of sample time $k$, the optimal actuation calculated in the previous sample time ($u_{[k-1]}$) is applied, therefore, the system state $x_{[k+1]}$ is already predetermined. This state can be *estimated* through

$$x_{e[k+1]} = f_e(\mathbf{x}_{[k]}, u_{[k-1]}) \tag{5}$$

where $f_e$ is the system model for the estimation (usually a full-system model), and $\mathbf{x}_{[k]}$ is the measured state at $k$.

Thus, in this work, a one-step quadratic cost function (for $k+2$) is considered

$$V(x_{[k]}, u_{[k]}) = \| x'_{[k+2]} - x^{\star}_{[k+2]} \|^2_P \tag{6}$$

where $x^{\star}_{[k+2]}$ is the system state reference, $x'_{[k+2]} = f_p(x_{e[k+1]}, u_{[k]})$ denotes the *predictions* for all the possible switches state combinations $u_{[k]} \in \mathbb{U} = \{0,1\}^m$, with $m$ the number of power switches, and $P = \text{diag}\{\lambda_1, \ldots, \lambda_n\}$ contains the weighting factors used to penalize future tracking errors. Note that the system model $f_p$ can be a simplified system model, in order to reduce the computational burden.

Thus, $\| \cdot \|^2_P$ in (6) represents a quadratic weighted Euclidean norm.

Finally, to obtain the optimal input, one can evaluate, at each sampling instant, each element of $\mathbb{U}$ in the cost function (6). Consequently, the optimal control actuation is the one that produces the minimum value of $V$, i.e.,

$$u_{\text{MPC}[k]} = \text{argmin}_{u \in \mathbb{U}} \left\{ V(x'_{[k+1]}, u_{[k]}) \right\}. \tag{7}$$

Further background related to this methodology (e.g., stability analysis) can be found in [11], [26], and [27].

## III. Dual-Stage Strategies

As evidenced by the power electronics literature, it is well known that FCS-MPC strategies can achieve a fast closed-loop dynamic performance. On the other hand, PWM-based linear controllers with integral action provide a good steady-state performance in terms of spectrum, commutations, and steady-state error. Motivated by this, in this article, a dual-stage control strategy for power converters, which combines these two controller classes is proposed.

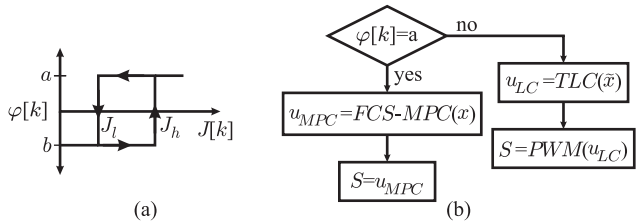


Fig. 2. Hysteresis comparator: (a) hysteresis bands and (b) controller selection.

### A. Commutation Between TLC and FCS-MPC

Due to the different nature of each controller in terms of structure and kind of input, the main challenge here is related to the transitions between both controllers. They must be as smooth as possible in order to avoid undesired bumps and oscillations (chattering effects).

To achieve this goal, the system state deviation, which has a similar structure than the cost function (6), is introduced first

$$J_{[k]} = \| x_{[k]} - x^{\star}_{[k]} \|^2_P \tag{8}$$

where $x_{[k]}$ is the whole system state, which can include, for example, internal capacitor voltages and output currents.

This allows the dual-stage controller to determine how far from the reference is the present value of the system state. Thus, $J_{[k]}$ is the input of the hysteresis comparator stage shown in Fig. 2. This is comprised of two bands $J_l$ and $J_h$ [see Fig. 2(a)], where $0 < J_l < J_h$. Therefore, the two controller transitions are as follows.

*1) Traditional Linear Controller to Finite-Control-Set Model Predictive Control:* Whenever $J_{[k]} > J_h$, the controller switch is at position $a$, as shown in Fig. 2(b). FCS-MPC is activated to rapidly move the states to the neighborhood of their reference values. Since the only information required by this predictive control strategy is the system state measurements at the beginning of each sampling instant, i.e., $x_{[k]}$, there is no need of additional actions to obtain an adequate transition.

*2) Finite-Control-Set Model Predictive Control to Traditional Linear Controller:* When $J_{[k]} < J_l$, it means that the system is close to its operation point, and therefore, the assumptions for the TLC design are valid. Therefore, the controller switches from FCS-MPC to the PWM-based TLC, i.e., the controller switch is now at the position $b$, as shown in Fig. 2(b). This transition is not trivial, as the linear controller have at least one internal state, which must be properly set to the new system operation point. This is required to obtain a fast and soft transition when the FCS-MPC is disconnected. Otherwise, the initial linear controller output will not be compatible with the new system state. Thus, the challenge is focused on the development of a fast and compatible manner to update the internal controller states.

*3) Hysteresis Path:* Finally, if $J_l < J_{[k]} < J_h$, the system uses the same controller scheme used at $k-1$. This avoid unnecessary commutations between the controllers once the system reaches either $J_l$ or $J_h$, and reduces the effect of noisy measurements.

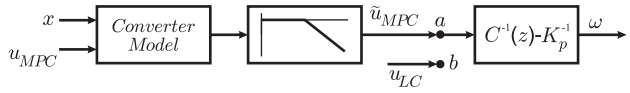


Fig. 3. Adaptation stage to initialize the PWM-based TLC.

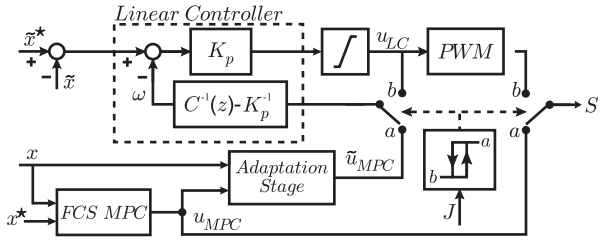


Fig. 4. General block diagram of the proposed dual-stage control strategy.

### B. Initialization of the TLC States for a Bumpless Operation

The *feedback form* is usefull as an antiwindup structure due to its ability to set all the controller inner states in concordance with the real actuation applied to the plant. Thus, by taking advantage of this property, when the FCS-MPC is active, the linear controller is constantly being fed with the actual switching input applied by the FCS-MPC, as depicted in Fig. 3. This way, the linear controller inner states are permanently updated avoiding overshoots and undesired dynamics when $J_{[k]} < J_l$.

Nevertheless, since the nature of $u_{LC}$ and $u_{\text{MPC}}$ is different (duty-cycles and power switches states), it is necessary to transform $u_{\text{MPC}}$ into a compatible signal for the linear controller (normally the inverter voltage). This can be easily done by using the converter model. Due to the discrete nature of the switching signals generates by the FCS-MPC, the output of this model is, in general, a staircase waveform. Therefore, for a cleaner linear states update, a low-pass filter can be used to obtain the fundamental components of the output voltage applied with FCS-MPC, $\tilde{u}_{\text{MPC}}$ in Fig. 3. Consequently, whenever the FCS-MPC is active (controller switch in position $a$ in Figs. 2 and 3), all the internal controller states, $\omega_{[k]}$, are updated based on the information provided by $\tilde{u}_{\text{MPC}}$, by using (4), i.e.,

$$\omega(z) = \left(C^{-1}(z) - K_p^{-1}\right) \tilde{u}_{\text{MPC}}(z). \tag{9}$$

Once the system state is led to the neighborhood of the reference, and the dual-stage control strategy commutes to the PWM-based linear controller (controller switch in position $b$ in Figs. 2 and 3), the linear controller will be aiming to an actuation similar to that of the FCS-MPC. So, bumps and unwanted oscillations will be drastically reduced.

Finally, the whole proposed dual-stage control strategy is presented in Fig. 4.

## IV. Case Study: FCC

To highlight the advantages of the proposed control strategy, this work considers the three-cell three-phase FCC shown in Fig. 5 as an illustrative example. However, the analysis can be easily extended to any cell number.

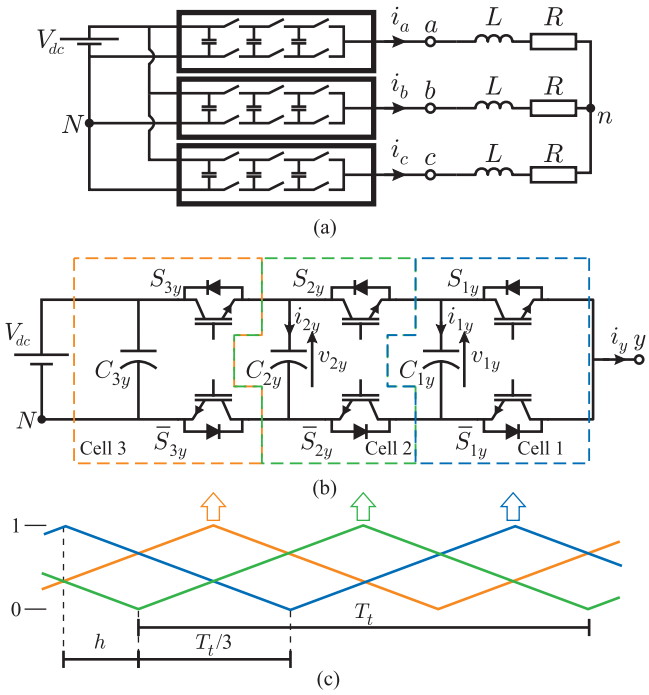


Fig. 5. (a) Three-phase three-cell FCC. (b) Single-phase three-cell FCC. (c) Triangular carriers used for the PS-PWM.

### A. FCS-MPC of an FCC

The FCC is a multilevel topology early introduced in [19]. Fig. 5(a) shows the topology for a three-cell three-phase FCC. Each phase $y \in \{a, b, c\}$ is composed of a tandem connection of three basic units called *cells*, as shown in Fig. 5(b). Each cell requires one capacitor $C_{jy}$, with $j \in \{1, 2, 3\}$, and two power switches $S_{jy}$ and $\bar{S}_{jy}$, which must be operated complementary. In this case, a passive three-phase load is considered, where $R$ and $L$ stand for the resistance and inductance, respectively.

To obtain a discrete-time model of the FCC, first, the per-phase system state and control signal are defined as

$$x_{y[k]} = \begin{bmatrix} i_{y[k]} \\ v_{1y[k]} \\ v_{2y[k]} \end{bmatrix}, \quad u_{y[k]} = \begin{bmatrix} S_{1y[k]} \\ S_{2y[k]} \\ S_{3y[k]} \end{bmatrix}, \quad y \in \{a, b, c\}. \tag{10}$$

Thus, the whole system state and control input of the FCC is given by

$$x_{[k]} = \left[x_{a[k]}^{\text{T}}\ x_{b[k]}^{\text{T}}\ x_{c[k]}^{\text{T}}\right]^{\text{T}}, \ u_{[k]} = \left[u_{a[k]}^{\text{T}}\ u_{b[k]}^{\text{T}}\ u_{c[k]}^{\text{T}}\right]^{\text{T}}. \tag{11}$$

Therefore, as presented in [25], the FCC can be modeled in the discrete-time domain with a sampling period of $h$, by

$$i_{y[k+1]} = k_a i_{y[k]} + k_b \left(v_{yN[k]} - v_{nN[k]}\right) \tag{12}$$

$$v_{1y[k+1]} = v_{1y[k]} + \frac{h}{C_{1y}} i_{y[k]} \left(S_{2y[k]} - S_{1y[k]}\right) \tag{13}$$

$$v_{2y[k+1]} = v_{2y[k]} + \frac{h}{C_{2y}} i_{y[k]} \left(S_{3y[k]} - S_{2y[k]}\right) \tag{14}$$

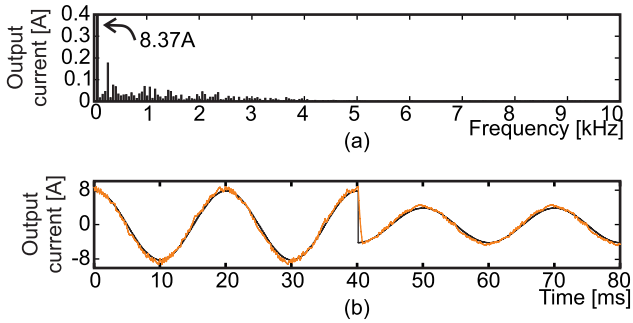


Fig. 6. Simulation results for FCS-MPC govern an FCC. (a) Spectrum for $i^\star$=8 A. (b) Dynamic behavior for a reference step from $i^\star$=8 A to $i^\star$= −4 A.

with $k_a = e^{-h\frac{R}{L}}$, $k_b = (1-k_a)/R$, and

$$v_{yN}[k] = (S_{1y}[k] - S_{2y}[k])\, v_{1y}[k] + (S_{2y}[k] - S_{3y}[k])\, v_{2y}[k] + S_{3y}[k] V_{\rm dc} \quad (15)$$

is the converter output voltage, and

$$v_{nN}[k] = \frac{v_{aN}[k] + v_{bN}[k] + v_{cN}[k]}{3} \quad (16)$$

is the common-mode voltage.

In order to achieve the desired balanced voltage condition, a closed-loop controller for an FCC should not only govern the output current, but also the internal floating voltages, where

$$v_{jy}^\star = j\,\frac{V_{\rm dc}}{3}, \qquad j \in \{1,2\} \quad (17)$$

cf., [25]. In this way, all semiconductors can be designed to block a voltage of $V_{\rm dc}/3$, generating a multilevel output voltage waveform of four-levels. Therefore, from a control viewpoint, an FCC is a challenging topology, which presents nonlinearities described in (12)–(16), and several control targets.

To design the FCS-MPC, matrix $P = \text{diag}\{P_a, P_b, P_c\}$ in the cost function (6) is tuned with

$$P_y = \text{diag}\{\lambda_{1y}, \lambda_{2y}, \lambda_{3y}\}. \quad (18)$$

Here, $\lambda_{jy} > 0$ are design parameters (weighting factors), which allow trading current tracking errors for deviations in capacitor voltages. It is also considered that $P_a = P_b = P_c$.

The proper setting of the $\lambda_{jy}$ can be nontrivial, and will depend on several factors as measurements quality, sampling time, and model accuracy. Moreover, it is important to notice that a high $\lambda_{1y}$ value will make the FCS-MPC put a higher effort in the current tracking than in the voltage capacitors. If these voltages are not properly controlled, a higher distortion in the output current will be generated. Therefore, as a rule of thumb, it is recommended to start with a lower value of $\lambda_1$. Finally, as both capacitor voltages are equally important, similar values for $\lambda_{1y}$ and $\lambda_{2y}$ are suggested.

Finally, taking into account the FCC model (12)–(16) and the cost function (6) tuned as per (18), the optimal control input, $u_{\rm MPC}[k]$, is obtained by following the same procedure presented in [25, Sec. III].

Fig. 6 shows the simulation results when a pure FCS-MPC is used to govern the system, with a 10% of error in the model resistance. As previously stated, a wide spread spectrum is obtained, as shown in Fig. 6(a), and a noticeable error in the fundamental component, reaches 8.37 A instead of the 8 A required by the reference. On the other hand, Fig. 6(b) shows the dynamic behavior of the system under a reference step from 8 to −4 A. Here, the system is rapidly led to the reference value with no noticeable oscillations.

### B. PWM-Based TLC of an FCC

It is well reported in the literature [21] that phase-shifted PWM (PS-PWM) is a simple modulation technique that allows us to keep the natural balance of the flying capacitors.[1] As three cells per phase are considered, three carriers phase-shifted in $T_t/3$ are required [see Fig. 5(c)]. Therefore, as the floating capacitors voltage balance relays on the modulation, it is only required to control the three-phase output current, which in this case are expressed in a *dq*-framework, i.e.,

$$\tilde{x}[k] = \begin{bmatrix} i_d[k] & i_q[k] \end{bmatrix}^{\rm T}, \quad \tilde{x}^\star = \begin{bmatrix} i_d^\star & i_q^\star \end{bmatrix}^{\rm T}. \quad (19)$$

An additional consequence of the capacitor voltage balance is that the overall FCC plus load system can be considered as a linear system. Therefore, the simplified *dq*-system, including the converter and the load in continuous time is given by

$$G_d(s) = G_q(s) = \frac{1}{sL+R} e^{-{\rm sh}} \frac{V_{\rm dc}}{2} \quad (20)$$

where $s$ is the Laplace operator, and $L$ and $R$ are the load parameters.

Then, as a three-phase sinusoidal current is desired, the system state reference becomes constant, and (20) is a "well-behaved" transfer function. Thus, simple PI controllers (one for each axis) are required.

The discrete-time PI controller structure is given by

$$C(z) = K_p \left( \frac{z-a}{z-1} \right). \quad (21)$$

Thus, $u_{LC}$ is obtained from (4) and (3). Then, this actuation is transformed to the original *abc*-framework and, thus, used as references for the PS-PWM.

Fig. 7 shows the results for the system govern by PI controllers (in $d$- and $q$-axis) under the same conditions than the results of Fig. 6. Here, a well-defined spectrum arround $T_t/3$ is obtained, due to the use of the PS-PWM scheme, with no steady-state error, even with an error in the resistance of 10%, as shown in Fig. 7(a). Under a reference step, the PIs are able to reach the new reference value but in a larger time than the FCS-MPC [see Fig. 6(b)], and with some small oscillations, as shown in Fig. 7(b). Regarding the capacitors voltage balance, large oscillations and very low dynamics are obtained, as shown in [18].

[1]Here, PS-PWM is preferred since it is easy to implement. However, any modulation strategy that guarantees the capacitor voltage balance can be used. See, e.g., [22], [28], where PD- and SV-PWM are considered.

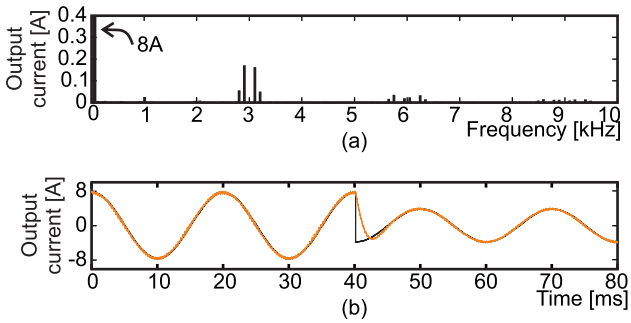


Fig. 7. Simulation results for a TLC govern an FCC. (a) Spectrum for $i^{\star}$=8 A. (b) Dynamic behavior for a reference step from $\hat{\imath}^{\star}$=8 A to $\hat{\imath}^{\star}=-4$ A.

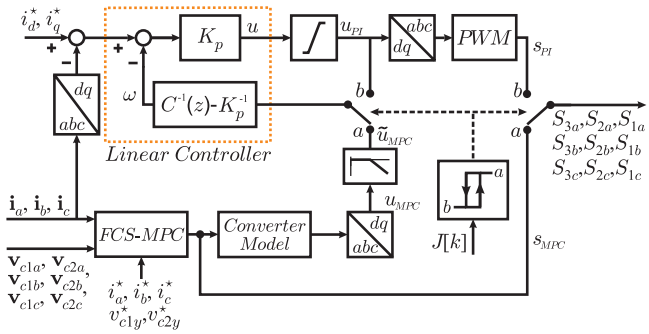


Fig. 8. Proposed dual-control scheme applied to a three-phase FCC.

### C. Proposed Dual-Stage Control of an FC Converter

To finally design the dual-stage controller for the FCC, it is required to adjust the hysteresis comparator stage.

A large value of $J_{[k]}$ indicates that the system state is far from the desired reference. This can be produced either by a large reference step and/or a system perturbation. In those cases, the system state is quickly led toward the reference by the FCS-MPC. A low value of $J_{[k]}$ indicates that the system state is near the reference, which may not be reached when using FCS-MPC with zero-steady-state error [10], [11]. Hence, the PWM-based linear controller is activated to finally achieve the desired reference.

The lower and upper bounds of the hysteresis, $J_l$ and $J_h$, respectively, are design parameters of the proposed dual-stage strategy. When the PWM-based linear controller is used, a synchronous sampling can be implemented. Therefore, in steady state, the average output current error can be neglected. In such case, the system deviation relays on the floating voltage error. The maximum floating voltage error for each capacitor $\widehat{\Delta}_v$, in normal operation, can be calculated through

$$\widehat{\Delta}_v = \frac{1}{C_{jy}} \hat{\imath}_y \, h \tag{22}$$

where $C_{jy}$ is the capacitance of the respective floating capacitor, $\hat{\imath}_y$ is the maximum value of the output current, and $h$ is the sampling time. Then, the maximum deviation per phase is given by

$$J_{hy} > \left( \frac{\lambda_{2y}}{C_{1y}} + \frac{\lambda_{3y}}{C_{2y}} \right) \hat{\imath}_y \, h. \tag{23}$$

Finally, the worst case for the steady-state operation of the system can be used as a limit for the hysteresis upper bound

$$J_h \geq J_{ha} + J_{hb} + J_{hc}. \tag{24}$$

The lower bound of hysteresis $J_l$ is adjusted via simulations, since it depends on the settings of the FCS-MPC (weighting factors, sample time, etc.) and the system deviation $J_{[k]}$, defined in (8). Since FCS-MPC have some issues to reach the zero-steady-state operation [10], a too low $J_l$ can be unreachable, and therefore, the TLC will not be activated. Otherwise, a too high $J_h$ value will switch to TLC when the system state is too far from the operation point. This can lead to floating voltages oscillations and/or a poor current tracking dynamics.

Finally, Fig. 8 shows the proposed scheme for the control of the three-phase FCC.

TABLE I
MAIN CONVERTER AND CONTROL PARAMETERS

| | Parameter | | Value |
|---|---|---|---|
| Converter | Main dc-link voltage | $V_{dc}$ | 300V |
| | Load Resistor | $R$ | 15-18Ω |
| | Load Inductor | $L$ | 5mH |
| | Floating Capacitors | $C_{1y} = C_{2y}$ | 330$\mu$F |
| Controller | Sampling Time | $h$ | 125$\mu$s |
| | Carriers Period | $T_t$ | 750$\mu$s |
| | Lower boundary | $J_l$ | 5 |
| | Upper boundary | $J_h$ | 100 |
| | Current weighting factor | $\lambda_{1y}$ | 0.05 |
| | Voltage weighting factors | $\lambda_{2y} = \lambda_{3y}$ | 2 |
| | Proportional Gain | $K_p$ | 4.3 |
| | Zero location | $a$ | 0.17 |
| | $C_{1y}$ voltage reference | $v^{\star}_{c1y}$ | 100V |
| | $C_{2y}$ voltage reference | $v^{\star}_{c2y}$ | 200V |

## V. EXPERIMENTAL RESULTS

The proposed dual-stage controller is tested in a 4 kW three-phase three-cell FCC. The main parameters of this prototype and the controller are summarized in Table I. The proposed scheme is implemented in a digital platform composed by a standard 225 MHz TMS320C6713 DSP and an XC3S400 FPGA. The execution time of the codes are as follows: 13 $\mu$s when the PIs controllers are used, while the time increases to 57 $\mu$s when FCS-MPC is selected (including the PIs inner state update).

As 1.33 kHz carriers are used, the semiconductors switching frequency is limited to that frequency when the proposed scheme uses the PI controllers. On the other hand, when FCS-MPC is selected the maximum switching frequency is limited to 4 kHz as a sampling frequency of 8 kHz is used. Therefore, for an appropriate filtering of the FCS-MPC signals in the adaptation stage, a second-order digital Butterworth filter with a cutoff frequency of 2 kHz is used.

Fig. 9 depicts the dual-stage control closed-loop behavior, for a step change reference on $i_d$, when no special considerations

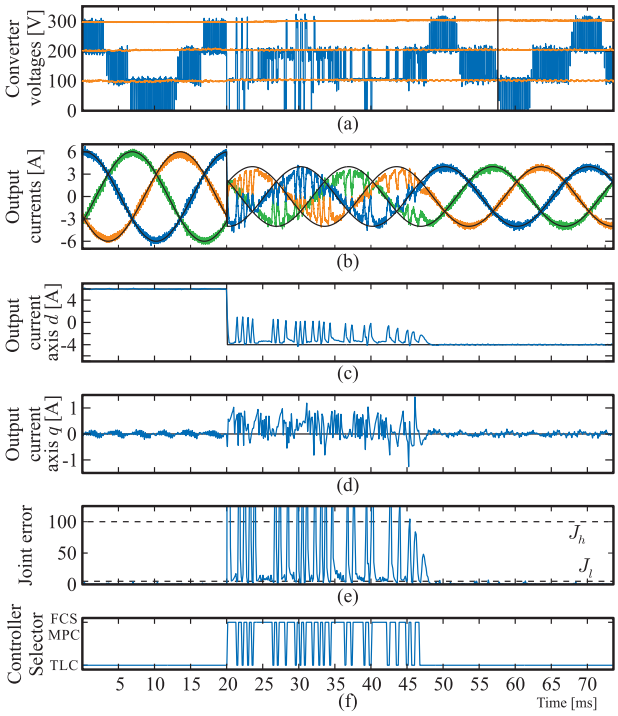


Fig. 9. System response for a dual-stage controller without an update of the linear controller states.

on the PI internal states are taken. Once the step is applied, FCS-MPC is activated, rapidly moving the currents to the new reference values, reducing the system state deviation, $J_{[k]}$, to $J_l$. Once $J_{[k]} < J_l$, the dual-stage controller applies the input calculated by the PI. As the internal states are not updated, the actuation of the PI corresponds to the optimal actuation for the previous reference (6 A in this case), increasing the $i_d$ value and, hence, $J_{[k]}$. Therefore, the dual-stage controller switches back to FCS-MPC, which reduces $J_{[k]}$ once again. Thus, the dual-stage controller returns to the PI. This situation is repeated over and over, until the PI states reaches adequate levels, in this case at $t = 47$ ms. Clearly, this kind of response is not acceptable for power converters, thus stressing the need of an appropriate way to update the internal states of the linear controllers, as detailed in Section III.

Fig. 10 shows the results obtained by using the internal controller states updating scheme proposed in Section IV-C with and without parameter mismatch (right and left column, respectively). As can be observed, the use of the *feedback form* successfully updates the linear controller states, leading to a soft transition from FCS-MPC to the PI controllers. A small oscillation can be observed in the $dq$-currents when using the proposed method and an accurate model [see left column in Fig. 10(c)]. This oscillation is generated by the adaptation stage since it has to initialize the internal PI controller states based on the previous switching input provided by the FCS-MPC. Therefore, during this transition, there is a slight difference between the actual PI inner states and their optimal values to achieved a zero-steady-state error. After that, the feedback form in the adaptation stage uses the actual PI actuation to update the internal states. Hence, this oscillation vanishes. This situation is also reflected in the joint error [see Fig. 10(e)], through a small increase in its value when the system commutes from FCS-MPC to the PWM-based PI controller.

Right column shows the system behavior when a parameter mismatch is introduced in the model. The resistance value used in the model is kept in 15Ω, while the real resistance used is set to 18Ω (a 20% error). As can be observed in the results, the linear controllers are able to lead the system to the reference values, due to their integral action. Therefore, results with and without parameter mismatch are almost the same when the PI controller is governing the system. Note, however, that FCS-MPC is applied for a longer time, as the model used to run the predictions considers an erroneous value of the load resistance. Also notes that FCS-MPC tends to operate with a steady-state error in the currents [see Fig. 10(d) and (e)]. As expected, once the system is moved to the neighborhood of the reference, the PIs take the control of the system and the steady-state error is eliminated. Fig. 10(f) shows, the output current spectrum in steady state, which is concentrated and well defined around 4 kHz, due to the use of PS-PWM, with triangular carriers of 1.33 kHz.

Fig. 11 shows the system behavior under an increase of the main dc-link voltage from 270 to 300 V. In order to keep the floating voltages ratio at their natural balance ratio, namely $V_{\text{dc}} : v_{c2y} : v_{c1y} = 3 : 2 : 1$, the floating voltage references $v^{\star}_{c1y}$ and $v^{\star}_{c2y}$ increase from 90 to 100 V and from 180 to 200 V, respectively. This change in the references increases the value of the joint error function, so the systems switches to FCS-MPC. Then, the floating voltages rapidly increase their values to the new references, reducing the value of $J_{[k]}$. Note that a fast, and almost oscillation-free, response is obtained in the floating capacitors due to the active control provided by the FCS-MPC, which considers the full nonlinear model of the system in order to find an optimal actuation. The response can be compared with the natural balance operation [17], [21], which can take several periods and have large oscillations.

To highlight the flexibility of the proposed control scheme, Fig. 12 depicts the results of the proposed scheme applied to a single-phase FCC. In this case, the output current reference is set to

$$i^{\star}(t) = \bar{i} + \hat{\imath}\sin(2\pi 50t) \tag{25}$$

with $\bar{i}$ changing from 5 to 3 A and $\hat{\imath}$ changing from 3 to $-2$ A at $t = 31$ ms. As the reference is composed by a constant and a sinusoidal component, a PI controller with a resonant component at 50 Hz is implemented

$$C(z) = K_p\,\frac{z-a}{z-1}\,\frac{z^2+bz+c}{z^2-2\cos(2\pi 50\,h)z+1} \tag{26}$$

where $K_p$, $a$, $b$, and $c$ are the controller design parameters. From (26), it can be stated that it is necessary to properly update three states for a bumpless transition.

As can be observed in Fig. 12, a fast response is obtained for this reference change, due to the FCS-MPC action. Once $J_l$ is reached, the dual-stage controller switches to the PI-resonant controller generating a small increase in $J_{[k]}$, which is too small to reactivate the FCS-MPC, therefore, a bumpless transition is

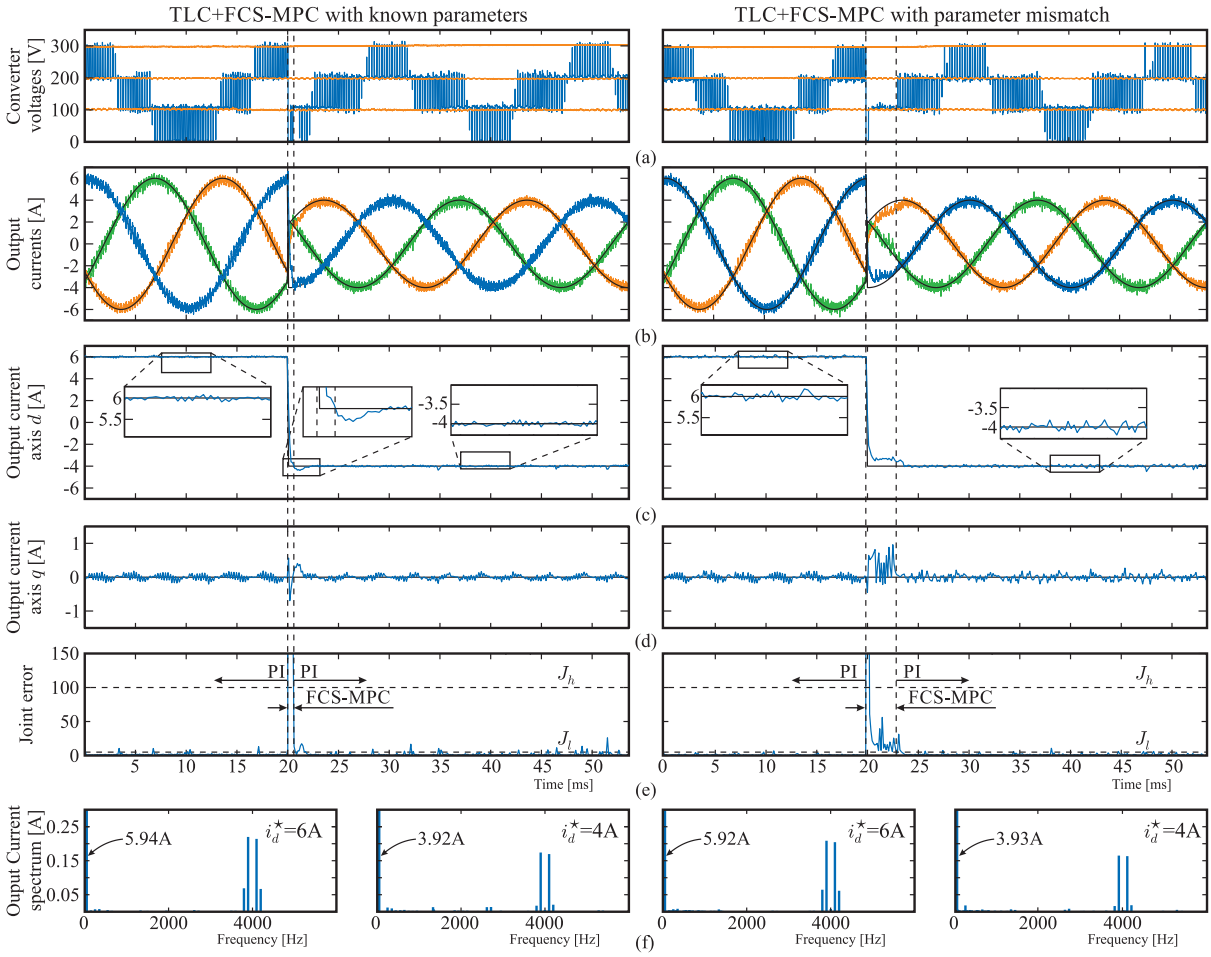


Fig. 10. System response for a dual stage controller with the proposed scheme.

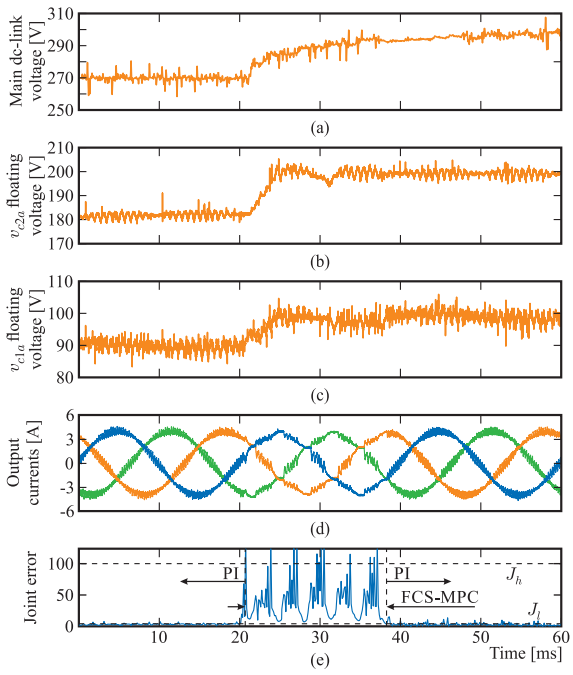


Fig. 11. System response for a disturbance on the main dc-link voltage.

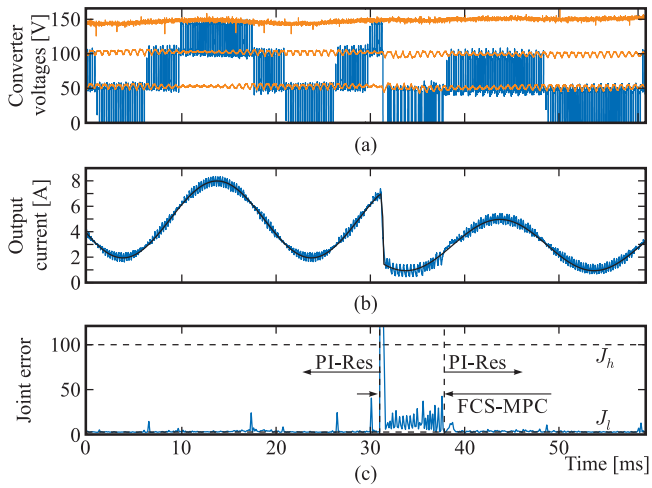


Fig. 12. Results for the proposed control scheme for a single phase FC converter with a PI-resonant controller.

obtained. Once the PI-resonant controller governs the system, it is able to provide a perfect tracking of the constant and sinusoidal part of the reference.

## VI. Conclusion

In this article, a dual-stage controller based on an FCS-MPC and a TLC was proposed. This scheme is able to operate with zero-steady-state error, even under model uncertainties, due to the high gain of the linear controller at the designed frequencies. On the other hand, excellent dynamic behavior is obtained, even for a power converters with a nonlinear relationship between inner- and switches-states as the FCC, due to the use of FCS-MPC when large deviation from the system reference is detected.

To obtain a soft transition when commuting from FCS-MPC to the TLC, an adaptation of the feedback implementation of the TLC is proposed. This way, the TLC states are properly updated accordingly to the FCS-MPC actuation.

The proposed dual-stage control strategy was experimentally tested in an FCC for different TLC structures (PI and PI-resonant). In all cases, a smooth controller transition was obtained, while achieving a fast closed-loop dynamic and an excellent steady-state performance, even under parameter missmatch, which cannot be achieved by a standard FCS-MPC.

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