Independent Time-Delay Signal Cancellation for Fast Harmonic-Sequence Filters Targeting Arbitrary Sequences and Frequencies

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***Abstract*—A new type of filter/extractor named independent time-delay signal cancellation (itDSC) method is proposed in this article. Unlike conventional harmonic sequence filter (HSF) designs, the phase modifying and vector recovering stages of the proposed itDSC are separately set with single targets to make time-delays independent from the targeted HS indices and fundamental period. Consequently, the proposed HSF is more flexible in design, more robust and accurate in performance as well as faster in dynamic response compared to the conventional ones. A new phasor representation of an arbitrary order and sequence is first introduced for three-phase signals by using only a single integer-index-number (*h*). Then, a generalized principle of filtering/extracting arbitrary HS is proposed where the conventional time-dependent methods are specific cases. Last, new designs with independent time-delays are proposed to avoid the drawbacks of dependent time-delays and improve the filter performance in the applied systems. Comparative performance and extended applications on fundamental-frequency positive-sequence extraction used in power converter control areas are presented. The experiments show the superiority, application potentials, and challenges of the proposed method in the power converter control area.**

***Index Terms*—Converter control, frequency-locked loop, grid connection, harmonic sequence (HS) filtering, phase-locked loop, sequence extraction.**

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I. Introduction

THE integration of distributed generation (DG) systems increases the complexity of electric power systems because microgrids can work in stand-alone or grid-connected modes [1]. Power electronic converter systems in DG microgrids play an important role in improving service reliability and address power quality issues, such as voltage sags, harmonic pollution, and voltage imbalances [2]. In the reliability and power quality aspects, the task of extracting reliable parameters of the frequency, voltage, and current characteristics is essential and challenging due to the inevitable contamination of harmonic sequences (HSs) incurred in power electronics [3].

Regardless of the HS distortion, it is essential to continuously monitor voltage/current characteristics in electric power systems for maintaining the reliability, quality, and stability of the power grid. The presence of HS disturbances in the grid voltage can cause errors in the frequency estimation, which can lead to inaccurate results of control and protection tasks [4]. In one perspective, it is important to have a good quality of instrumentation and measurement devices, as well as proper calibration, to minimize the offset and noise introduced by the instrumentation itself. In other perspectives, robust estimation methods are needed to handle these disturbances and provide accurate parameters [5].

The estimation of frequency, amplitude, and phase of voltages or currents in electric power systems is the core issue for various applications related to microgrids [5], DG [6], flexible alternating current transmission systems [7], and conditioner devices such as dynamic voltage restorers [8], active filters [9], unified power flow controllers, or static synchronous compensators [10]. For example, in microgrids, the extraction of fundamental frequency positive and negative sequence (FFPS/FFNS) voltages from HS disturbance is required for the proper operation and control of inverters [11]. Under microgrid faults, voltage distortion can become severe, and a fast response filter is needed to accurately extract the FFPS information to ensure the quick and accurate synchronization to the grid voltage and

frequency [12]. Besides, the frequency measurement is necessary to implement the conventional real power versus frequency droop controllers to maintain the active power balance [13]. Frequency control is particularly important during transitions between grid-connected and islanded modes, where high deviations of frequency can occur [14]. In transitions from islanding to grid-connected modes, the frequency of the microgrid cannot differ from the utility frequency by more than 0.1% according to IEEE 1547 (Standard for Interconnecting Distributed Resources with Electric Power Systems) [15]. Furthermore, frequency estimation is also needed for load shedding, frequency restoration, and grid code compliance in DG systems. In these applications, the adopted method must be fast, accurate, and robust even in the presence of harmonic distortion, voltage imbalances, magnitude fluctuations, and noise [16].

There are several state-of-the-art filtering methods for grid-side converters that have been proposed in the literature. The popular methods can be listed as complex bandpass filter (CBF) [17], moving average filter (MAF) in *dq*-frame [18], delayed signal cancellation (DSC) [19], cascaded DSC (CDSC) [20], multiple DSC (MDSC) [21] (as another form of MAF in $\alpha\beta-$frame), and the recent three-sample filter (3SF) method [22]. Interestingly, the harmonic sequence filter (HSF) effects can be achieved without an explicit filter design as a merit of the integral operator such as in second-order generalized integrator (SOGI) based methods [23], [24] or the popular proportional-integral (PI) control or in observer designs. These methods can be technically classified into three categories based on the HS cancellation principles: two-sample filter (2SF) [e.g, DSC, generalized DSC (GDSC), CDSC], 3SF, and multiple sample filter (MSF) (e.g., MAF, MDSC, integrator-based methods) principles. The 2SF principle does the cancellation by creating an 180° phase-shifted signal to combine with the original one. In the 2SF principle, only one phase-shifted vector is needed to cancel the original one. Meanwhile, the 3SF does the cancellation by the parallelogram law where two phase-shifted vectors of the parallelogram are created to cancel with the original vector [22]. The MSF principle such as the MAF in dq-frame, recent MDSC method [27], or integrator-based methods does the cancellation by creating multiple delayed samples covering the whole period of targeted harmonics. Each sample is evenly phase-shifted where the phase-shifted step and the number of samples have been designed to ensure the summation of all samples can cancel multiple targeted HS components at once. Each of these methods has its own advantages and disadvantages and they are suitable for different types of applications. The CBF is simple but it cannot totally cancel out the targeted HS components [28]. The MAF, MDSC, and integrator-based methods are useful for eliminating multiple high-order HSs, but its length of the moving window or the integration should be done in periods of time for low-order HS, which affects its dynamic response. Besides, the MSF can deal with a wide range of HS but it requires all necessary delayed samples within a period of targeted harmonic hence there are errors in transient times where the filter has not collected the necessary samples for cancellation.

In summary, the importance of filtering/extracting methods in microgrids is significant and the most challenges of the current methods are still on slow dynamic response due to the inevitable time-delay to collect enough necessary samples (especially for the low-frequency HS components), robustness to parameter mismatches such as the fundamental frequency (FF), and the simultaneous contamination of multiple unknown harmonic-sequence contents (implicit harmonic frequency and sequence). To overcome the mentioned challenges, this article proposes a new type of harmonic-sequence filter/extraction with independent time-delays (itDSC) for fast dynamic response targeting arbitrary sequences and frequencies. The key novelty is the required time-delays, which is independent of the targeted HS indices and FF to improve both robustness and dynamic response. A generalized phasor representation of arbitrary HSs is first introduced for three-phase signals using only a single integer number (h). Then, a generalized principle of filtering arbitrary harmonic sequences is introduced where the conventional time-dependent methods are thoroughly analyzed and generalized. From the generalization, the independent time-delay approach is proposed. Extended applications on FFPS/FFNS extractions in power converter control areas are also introduced with both simulation and experiment results. The experiments show an in-depth view of the superiority, fast-response advantages as well as challenges of the proposed approach when applied to the power converter control.

II. Representation and Generalized Principle of Three-Phase HS Filter/Extractor

This section is on the phasor representation of an arbitrary three-phase HS using a single integer number (h) to indicate both harmonic frequency and sequence (positive/negative), called in short "harmonic-sequence" (HS). Then, a generalized principle to eliminate arbitrary undesired HS components (h_x) from the desired one (h_1) is presented as a background for the proposed method.

A. Generalized Presentation and Principle of Harmonic-Sequence Filter/Extractor

The single-phase signal (s_x) in the time-domain comprises harmonic (h) components as the following:

$$s_x(t) = \sum_{h=0}^{\infty} s_x^{(h)}(t),\ x = \{a, b, c\},\ h = \{0, 1, 2 \ldots\} \tag{1}$$

where h is a non-negative integer representing the harmonic order components in the single-phase signal $s_x(t)$. In special cases, $h = 0$ represents the dc-offset component; $h = 1$ represents the FF component.

The real-time signal of the (h) component can be represented via complex numbers (phasor representation) as follows:

$$\begin{aligned} s_x^{(h)}(t) &= S_x^{(h)} \cos\left(h\omega t + \varphi_x^{(h)}\right) \\ &= S_x^{(h)} \left(e^{jh\omega t} e^{j\varphi_x^{(h)}} + e^{-jh\omega t} e^{-j\varphi_x^{(h)}}\right) \\ &= 0.5 \times \left(\dot{s}_x^{(h)} e^{jh\omega t} + \dot{s}_x^{*(h)} e^{-jh\omega t}\right), \\ \text{where } \dot{s}_x^{(h)} &= S_x^{(h)} e^{j\varphi_x^{(h)}} \end{aligned} \tag{2}$$

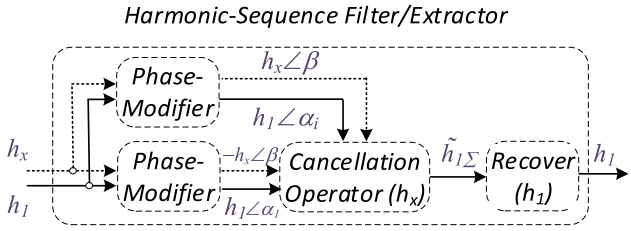

Fig. 1. Generalized principle for an HS filter/extractor with two targeted HS components (h_x) and (h_1) using only two samples to cancel out the unwanted HS component.

where s_x denotes the signal in time-domain, S_x is the amplitude, ($\dot{s}_x$, $\dot{s}_x^*$) are the corresponding complex number and its conjugate, and (h) is the harmonic order.

For three-phase signals, the phasor representation on a stationary $\alpha\beta$-frame via complex number can be obtained by Clarke transformation and the substitution from (2) as

$$\dot{s}_{\alpha\beta}^{(h)} = (2/3) \times \left(s_a^{(h)} + s_b^{(h)} e^{j2\pi/3} + s_a^{(h)} e^{-j2\pi/3} \right) = \dot{s}_{\alpha\beta+}^{(h)} e^{jh\omega t} + \dot{s}_{\alpha\beta-}^{*(h)} e^{-jh\omega t} = \dot{s}_{\alpha\beta}^{(+h)} + \dot{s}_{\alpha\beta}^{(-h)} \quad (3)$$

where

$$\dot{s}_{\alpha\beta}^{(+h)} = \dot{s}_{\alpha\beta+}^{(h)} e^{jh\omega t} = (1/3) \times \left(\dot{s}_{ha} + \dot{s}_{hb} e^{j2\pi/3} + \dot{s}_{hc} e^{-j2\pi/3} \right) e^{jh\omega t}$$

$$\dot{s}_{\alpha\beta}^{(-h)} = \dot{s}_{\alpha\beta-}^{*(h)} e^{-jh\omega t} = (1/3) \times \left(\dot{s}_{ha} + \dot{s}_{hb} e^{-j2\pi/3} + \dot{s}_{hc} e^{j2\pi/3} \right)^* e^{-jh\omega t}. \quad (4)$$

Equation (3) shows the composition of any balanced three-phase signals by positive and negative sequences. In a short form, a balanced three-phase signal s_{abc} ($s_{\alpha\beta}$) can be represented via harmonic-sequence components as

$$\dot{s}_{\alpha\beta} = \sum_{h=-\infty}^{\infty} \dot{s}_{\alpha\beta}^{(h)} \quad (5)$$

where the index number (h) is a general integer number with positive/negative values corresponding to positive/negative sequence and an absolute value of (h) denotes the harmonic order. For simplicity, the HS component of a three-phase signal is now denoted by only (h), which indicates both harmonic order and sequence.

Fig. 1 shows the generalized principle to filter an undesired HS component (h_x) from the desired HS one (h_1) or in other words, extracting (h_1) component from a signal contaminated by (h_x) component. The generalized principle shown in Fig. 1 comprises three main operators: phase modifiers, a cancelation operator, and a "recover". First, the signal is modified in phase by phase-modifiers such as time-delay and/or phase-shifting operators. The target of the phase modifiers is to make different phase-shifts between h_x and h_1 to ensure that in the next step of cancellation, the undesired HS (h_x) can be eliminated without eliminating the desired one (h_1). The cancellation operator can be as simple as a vector summation operator. After the cancellation operator, the desired HS (h_1) may be modified both in phase and amplitude due to the previous operators. Therefore, recovering operators for (h_1) should be used to recover the original desired component.

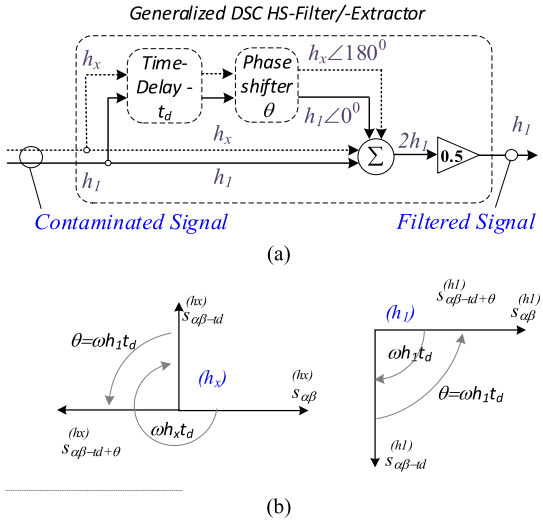

Fig. 2. Working principle of a GDSC HS-filter/extractor with dependent time-delay blocks. (a) Block diagram of main operators. (b) Illustration with phasor presentation of the filtering process with $h_1 = 1$, $h_x = 3$.

To change the phase of component signals, there are two types of phase-modifiers being applied: 1- Time-delay, 2- Phase-shifter by a rotation matrix. A rotation matrix can make an arbitrary phase-shift for HS components by multiplying the rotation matrix by the original vector using only algebraic calculation, which may not cost much delay-time in processing. However, the rotation matrix offers the same phase-shifts to all HS components regardless of their HS indices (h). Therefore, using only the rotation matrix for phase-shift is not enough to both cancel the h_x and retain the h_1 components. The other phase-modifier called time-delay operator can offer different phase-shifts to different HS components after the same time-delay due to the difference in HS index ($h_1 \neq h_x$). Hence, the time-delay is an inevitable operator in the filtering/extraction process, which presents explicitly or hidden in some operators.

B. Generalization of Dependent Time-Delay Methods

This section derives popular methods of dependent time-delay methods such as GDSC) [29], MAF [30], and recent MDSC [28] from the previously mentioned principle.

Fig. 2 shows the block diagram of the GDSC filter/extractor where the phase-modifiers comprise two operators: time-delay within t_d and a phase-shifter of an angle θ (rotation matrix). These two phase-modifiers achieve two targets simultaneously: 1) inverse the phase of h_x and 2) preserve the phase of h_1 as illustrated in Fig. 2(b). Therefore, after a simple summation between the phase-modified and original signals, a simple "recover" process is used with only a scaling operator of 0.5 as seen in Fig. 2(a).

Mathematically, the phase-modifiers with a time-delay t_d and matrix-rotation (θ) have the following transfer function with simultaneous two targets set as:

$$\dot{s}^{(h)}_{\alpha\beta-t_d+\theta}/\dot{s}^{(h)}_{\alpha\beta} = e^{j(-h\omega t_d+\theta)} = \begin{cases} -1 \,|h = h_x \\ +1 \,|h = h_1 \end{cases} \tag{6}$$

where $s_{\alpha\beta-td+\theta}$ denotes the phase-shifted signal after the phase-modifiers by time-delay t_d and phase-shift θ and $s_{\alpha\beta}$ denotes the original signal.

The general solutions of the trigonometric (6) are as

$$t_d = \frac{(m-n+0.5)T}{h_1-h_x}, \theta = 2\pi\left(\frac{m-n+0.5}{1-h_x/h_1}+n\right) \tag{7}$$

where $T = 2\pi/\omega$ is the fundamental period, and m and n are two arbitrary integers of the trigonometric solution.

From (7), it is obvious that for the condition of a positive time-delay $t_d > 0$ and to minimize the time delay t_d in the filtering process, the optimal selection of integers, m and n, results into the following optimal parameters:

$$t_d = 0.5 \times T/\left|h_x - h_1\right|, \theta = \pi h_1/\left|h_x - h_1\right|. \tag{8}$$

When optimal parameters of (8) are selected for an HS filter design, there is always a group of harmonic components ($\tilde{h}_x$, $\tilde{h}_1$) that will be filtered and persevered, respectively, at the same time, due to the arbitrary selection of m and n in (7). The group of HS components being filtered by the settings in (8) is identified from (7) as

$$\tilde{h}_x = h_1 - (k+0.5) \times T/t_d. \tag{9}$$

The results found in (8) and (9) are the general solution of DSC filters, which is also called the GDSC. For example, the filter design to eliminate the FFNS component from the FFPS one with respect to the indices: $h_x = -1$ (FFNS); $h_1 = 1$ would result in optimal parameters (8) with $t_d = T/4$ and $\theta = \pi/2$ as illustrated in Fig. 2(b). The group of simultaneously filtered HS (9) will be as $\tilde{h}_x = 4m + 3 = \{\ldots -5, -1, 3, 7, \ldots\}$. In another example for dc-offset, $h_x = 0$, $h = 1$, $t_d = T/2$, and $\theta = \pi$, $\tilde{h}_x = 2m = \{\ldots -4, -2, 0, 2, 4 \ldots\}$, resulting in elimination of all even HS components in both positive/negative sequences.

The interesting findings can be summarized from solutions (8) and (9) as follows.

1) The GDSC can eliminate an arbitrary HS regarding both frequency and sequence aspects (h_x) while preserving the (h_1) component because two parameters in (9) are available for any $h_1 \neq h_x$ (the arbitrary HS component can be any h_x).
2) Parameters, particularly time-delay t_d depends on the targeted HS components, i.e., ($h_x - h_1$) and the fundamental period (T). The value of t_d can be very large for the case that the undesired harmonic order h_x is very near the desired one h_1 (i.e., the dc-offset case).
3) From (8), the time-delay t_d depends on T and $|h_x, -h_1|$. This dependence on time-delay t_d not only slows down dynamic response but also reduces the robustness because the filtering performance is affected by the mismatches of T and h_x.

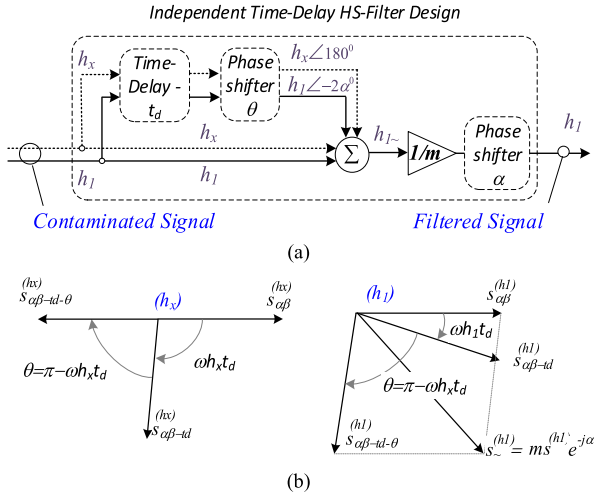

Fig. 3. Working principle of the independent time-delay design for HS filters. (a) Block diagram of main operators. (b) Illustration with vector presentation for the filtering process with $h_1 = 1$ and $h_x = 3$.

4) With the same harmonic order h_x, the time-delay t_d is larger if h_x is of the same sequence (i.e., positive or negative) with h_1 and vice versa.

To this end, the key reason for the large time-delay t_d is its dependence on the targeted HS indices especially when h_x is near h_1. To improve the dynamic performance and increase the robustness against the mismatches of T, a new strategy is to make the time-delay t_d independent from the targeted HS indices (h_x, h_1) and fundamental period (T). The solution is simple by reducing one target set in (6) in the phase-modifier stage as proposed in Section III.

III. Independent Time-Delay Designs for Fast Dynamic Response

This section presents the proposed approach of independent time-delay designs developed from the generalized principle and the generalization of DSC methods.

A. Arbitrary Time-Delay Design

As seen in Fig. 2(a), the dependence of time-delay t_d and phase angle θ on the targeted HS components (7) is due to the simultaneous targets set for two relevant phase modifiers. To set the t_d as an independent parameter, only a single target is set with respect to the parameter θ to cancel h_x as follows:

$$\dot{s}^{(h)}_{\alpha\beta-t_d+\theta}/\dot{s}^{(h)}_{\alpha\beta} = e^{j(-h\omega t_d-\theta)} = -1 \,|h = h_x \tag{10}$$

The solution of the trigonometric (10) is

$$\theta = (2n+1)\pi - \omega h_x t_d \tag{11}$$

where t_d is flexible as an independent time delay, which can be arbitrarily selected as small as a single sampling period ($t_d = T_s$), and n is an arbitrary integer. For simplicity, $n = 0$, which results in a new type of filter design illustrated in Fig. 3(b).

As seen in Fig. 3, the desired HS component (h_1) has been modified in both phase and magnitude after phase modification

(10) and cancellation stages as

$$\dot{s}^{(h_1)}_{\alpha\beta\sim}/\dot{s}^{(h_1)}_{\alpha\beta} = 1 + e^{j(-h_1\omega t_d-\theta)} = me^{-j\alpha} \tag{12}$$

where $m = 2\sin[0.5 \times (h_x - h_1)\omega t_d]$, $\alpha = 0.5 \times [\pi + (h_1 - h_x)\omega t_d]$, and $s_{\alpha\beta\sim}$ denotes the summed-up signal after the cancellation stage.

Hence, the phase and magnitude of the desired HS component (h_1) can be recovered by the following operator:

$$\dot{s}^{(h_1)}_{\alpha\beta} = (1/m) \times \dot{s}^{(h1)}_{\alpha\beta\sim}e^{j\alpha}. \tag{13}$$

It can be seen from (12) and (13) that in comparison with the GDSC, there is more computation for magnitude and phase recovery of the (h_1) component. However, there are significant benefits on targeting arbitrary HS components including the dc-offset as detailed in the following section.

B. Filtered and Unfiltered HS-Groups of the Proposed Method

From (11), the selected parameters of (t_d, θ) aiming at filtering the HS component h_x can simultaneously filter the following HS-group:

$$\theta = \pi - \omega h_x t_d = (2n+1)\pi - \omega \tilde{h}_x t_d$$
$$\leftrightarrow \tilde{h}_x = h_x + n \times (T/t_d), n \in \text{int} \tag{14}$$

where T is a fundamental period and T/t_d can be defined as a harmonic step of the filter.

Also, from (12), the unfiltered group of HS component due to the extraction of (h_1) is determined by

$$m = 2\sin\left[0.5 \times (\tilde{h}_1 - h_1)\omega t_d\right] = 0$$
$$\leftrightarrow \tilde{h}_1 = h_1 + m \times (T/t_d), m \in \text{int}. \tag{15}$$

It is worth noting that to remove the dc-offsets, (14) and (15) are set for $h_1 = 1$, $h_x = 0$ and $\tilde{h}_1 \neq 0$ $\forall m$ integer, then the time delay $t_d \neq$ n $\times$ T. From (14) and (15), it is worth the selection of the harmonic step (T/t_d) to ensure $\tilde{h}_1 \neq \tilde{h}_x$ $\forall m$, n integer.

From (14) and (15), the following conclusions can be made on the proposed independent time-delay designs.

1) For each filter design with a pair of parameters (t_d, θ) aiming at a specific pair of HS component (h_x, h_1), there are relevant HS-groups ($\tilde{h}_x$) to be filtered simultaneously and unfiltered HS ($\tilde{h}_1$) components to be preserved.
2) The time delay determines the width of the filter step (T/t_d) of filtered/unfiltered HS groups.
3) The proposed filter can effectively filter/extract the negative component from the positive sequence (i.e., $h_x = -h_1$) overcoming the drawback of the three-vector method [22].

C. Total Time-Delay in HS Extraction With Cascaded Filter Structure

This section applies the itDSC design to simultaneously filter multiple HS components to extract an arbitrary HS component taking the FFPS as an example.

The section also exhibits the capability of the proposed itDSC to cover the feasibility of the DSC as a generalized method. To highlight the superiority, comparative analyses are presented in Fig. 4.

It is assumed that the task is to extract a specific HS component, e.g., FFPS, from all contaminated HS components up to n order harmonics including both positive and negative sequences ($h_x = 0, -1, \pm2, \pm3, \ldots \pm n$). Conventionally, the CDSC and MDSC can be designed as Fig. 4(a) and (b) with the note that Fig. 4(b) is an MDSC design to work directly on the $\alpha\beta$-frame signal without dq-transformation while in dq-frame, the MDSC becomes the MAF method.

For the CDSC, from (8) and (9) to remove all the even harmonics ($h_x = 0, \pm2, \pm4, \ldots$), the time-delay of T/2 is required. Similarly, to remove ($h_x = -5, -1, 3, 7, 11$), a time delay of $T/4$ is required. Hence, to remove all the HS components up to $n = 2^k$ order, k-filters are cascaded as shown in Fig. 4(a). The total time required in the cascaded system is

$$t_{d\Sigma} = \sum_{i=1}^{k} T/2^i = \left(1 - 1/2^k\right) T = (1 - 1/n)\, T \tag{16}$$

where $n = 2^k$ is the width of harmonic band to be filtered. From (16), it can be inferred that for $k \to \infty$, the delay-time approaches one fundamental period (T) for all HS order greater than one.

Similarly, the MDSC design uses a series of time-delay (T/n) and rotation-matrix (phase-shifter) ($\alpha = 2\pi/n$) as shown in Fig. 4(b) to remove all the HS components up to n order and the total time delay is

$$t_{d\Sigma} = \sum_{i=1}^{n-1} T/n = (1 - 1/n)\, T. \tag{17}$$

The MDSC can be interpreted as a version of the MAF in $\alpha\beta-$frame.

The cascaded version of the proposed itDSC method is shown in Fig. 4(c). Based on (14) and (15), with a fixed time-delay equal to (T/n) to filter out all the hamronics up to n orders (both sequences), it needs ($n-1$) cascaded itDSC blocks. Hence, the total delay time for the cascaded design is

$$t_{d\Sigma} = \sum_{i=1}^{n-1} T/n = (1 - 1/n)\, T. \tag{18}$$

However, due to the flexibility of time delays, the time-delays of cascaded itDSC can be selected as the same as the CDSC mentioned above. With the same time-delay settings, the CitDSC turns into CDSC as a generalized method.

From (17) and (18), one can conclude the same total time-delay of the CDSC, recent MDSC, and CitDSC methods. It can be concluded that to totally remove the same full band of harmonics, the total delay time is the same. However, to remove a specific number of HS, the itDSC shows its flexibility and reduces time-delays in the filtering process. The flexibility of itDSC is to combine a group of target HS components and then assign to one itDSC filter because the time-delay determines the filter step (T/t_d) as seen in (14). The flexibility of itDSC

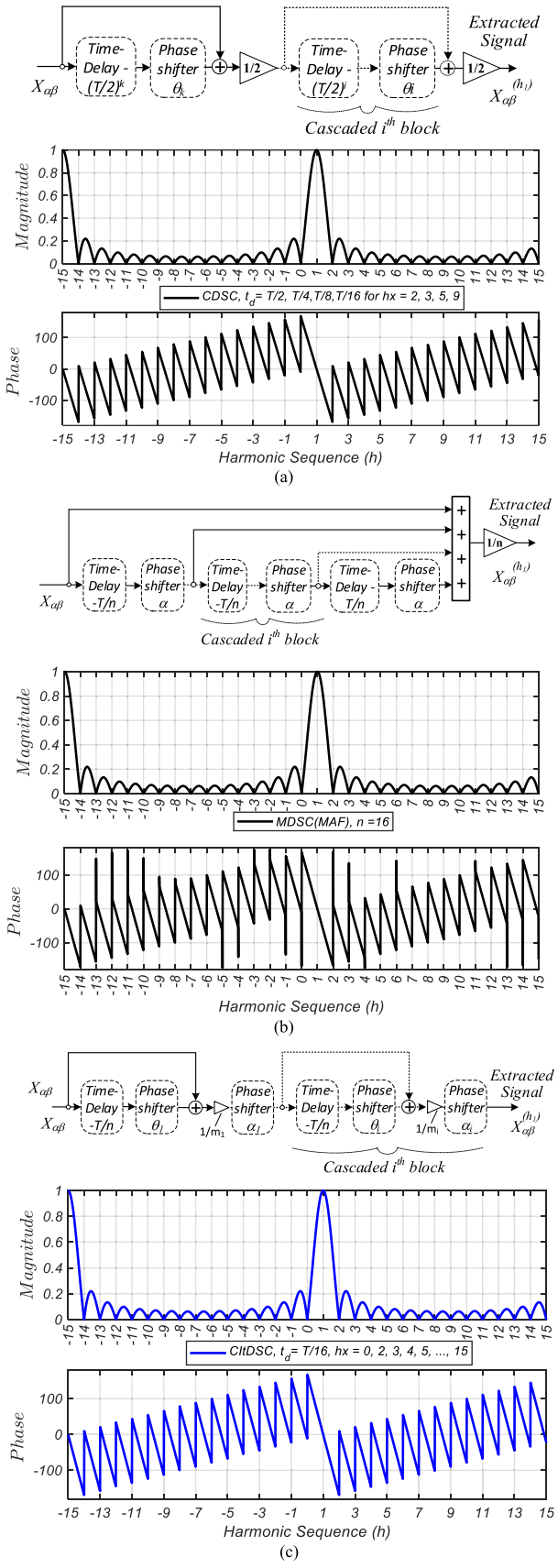

Fig. 4. Comparative bock diagrams of extraction methods. (a) Cascaded multiple DSC method in [20]. (b) Multiple DSC recently proposed in [21] as an MAF in $\alpha\beta$-frame. (c) Cascaded version of itDSC.

design can help to significantly reduce the computation burden by simplifying the cascaded filter structure.

To this point, the advantages of the proposed itDSC is exploiting the rough information of contaminated HS (h_x) available in power electronics and power systems, especially the fast dynamic response for the low-order HS components. Furthermore, in the next section, the itDSC can turn into the conventional DSC with the same setting time-delay making the proposed itDSC a generalization of DSC.

From the above-mentioned theoretical analyses, the advantages of the proposed itDSC can be expected as follows.

1) Flexible designs with a flexible selection of the time-delay t_d. If the time delay is selected as same as the DSC filters, the itDSC turns into a conventional DSC.
2) One filter design can target multiple HS components at once. Multiple HS components can be simultaneously filtered out by a single itDSC via a suitable selection of t_d because the group of filtered harmonics and the width of the filter step is flexible with the flexibility of t_d design.
3) Robustness of the designed filters based on itDSC method against the mismatches of fundamental period T, HS indices h_1 and h_x thanks to the independences of t_d.
4) Fast response of the filter and the overall related system thanks to small t_d.
5) High potentials in power electronics and power system applications where the harmonic indices (h_x) are roughly determined in terms of sidebands (roughly deterministic harmonics).

IV. Comparative Performance and Validation in Extended Applications

This section presents comparative studies to validate the superiority of the itDSC in applications. The advantage verification of the proposed itDSC method is on the following points.

1) Generalization of the itDSC covering the performance of the conventional DSC.
2) Flexible groupings of harmonic components to be simultaneously filtered by a single itDSC filter.
3) Fast dynamic response of filtering process under explicit indices of HS components.
4) Robustness of the itDSC under various scenarios of mismatches in applications, such as implicit harmonic noises, FF mismatches, frequency step-change, phase jump, and amplitude step-change.

Most updated competitive methods of the same categories on 2SF filter/extracting methods are adopted for a fair comparison.

A. Experimental Setup

Fig. 5 shows the comparative designs and experimental setup to investigate the performance of comparative methods. Fig. 5(a) shows the block diagram of adaptive and nonadaptive time-delay schemes where the HSFs are designed with DSC and itDSC concepts in fair conditions. Fig. 5(b) shows the diagram of the experiment setup and Fig. 5(c) shows the photography of the experiment application setup. As seen in Fig. 5(b), the grid voltages are emulated by an ac-grid emulator provided

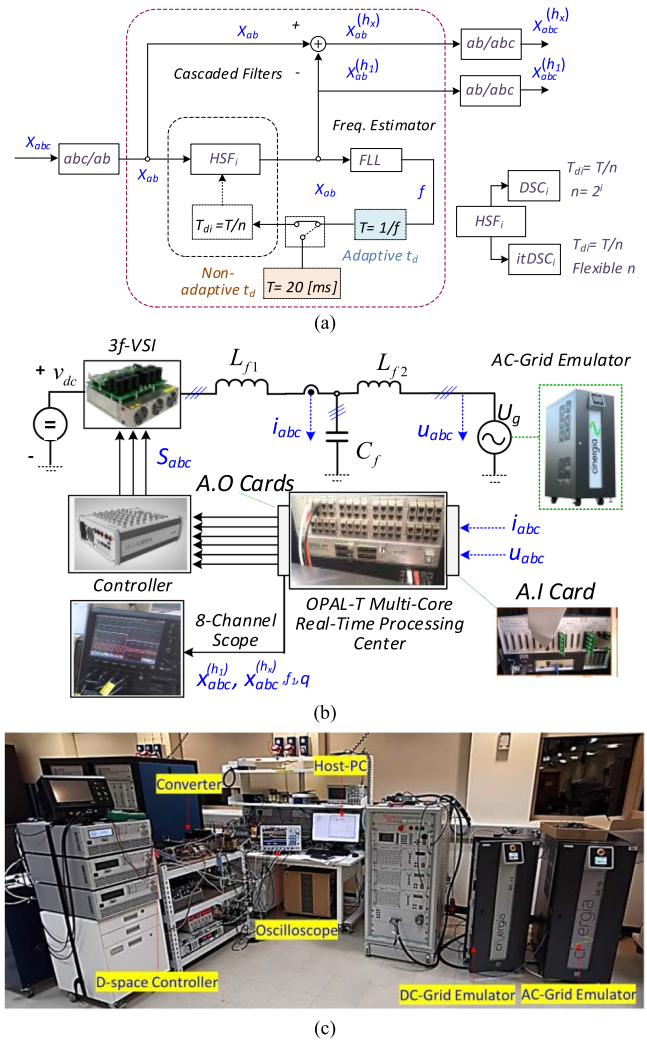

Fig. 5. Comparative filter/extractor designs in the application and the experiment setup. (a) Comparative designs with adaptive/nonadaptive mechanism from FLL. (b) Application of FFPS extraction in a control structure of grid-converters. (c) Photography of the overall experimental setup.

by CINERGIA-GE15 where the current and voltage signals from sensors are sent to the OPAL-RT 5700. The grid emulator can produce various conditions of three-phase grid voltages including the changes of harmonic, frequency, and phase. The sensor signals of currents and voltages are fed into the analog input card of the OPAL-RT 5700 where all the signals are processed for real-time applications. The powerful computation capability of OPAL-RT 5700 is on multicore processors and field programmable gate arrays to reduce the processing time and enable real-time operation. Processed signals from OPAL-RT are then fed into the D-SPACE MicroLabBox acting as a controller. Observed signals are exported to the analogy output card to show in the oscilloscope. Fig. 5(c) shows the overall setup in the laboratory where the proposed HSFs are a part of the overall microgrid system. The HSF are used to extract FFFS for an accurate and fast-response control system without using any PLL or the necessity of conventional PI controller published in [31] and [32].

B. Generalization Characteristic of itDSC Method and Flexible Designs for Fast Filter/Extraction of Explicit HSs

Fig. 6 shows the comparative frequency response in case of explicit HSs, i.e., $h_x = \{-1, 5\}$, $h_1 = +1$. Based on (9), to filter out $h_x = \{-1, 5\}$, the optimal dependent time-delay design requires two CDSC filters with $t_d = \{T/4, T/8\}$ and the frequency response is shown in Fig. 6(a). Fig. 6(b) shows the frequency response of a cascaded itDSC design with time-delay settings with the CDSC shown in Fig. 6(a). As seen in Fig. 6(a) and (b), both methods (DSC and itDSC) show the same frequency response under the same delay-time settings to prove the generalization characteristic of the proposed itDSC method over the conventional DSC. That is, it can be inferred that the DSC is a special time-delay setting of the itDSC.

Furthermore, Fig. 6(c) shows a flexible design using only one itDSC filter to simultaneously filter $h_x = \{-1, 5\}$. This single itDSC filter can be designed to filter out both HS, $h_x = \{-1, 5\}$ under the specific time-delay of $T/6$ (3.3 ms) compared to the total delayed time ($T/4+T/8$) (7.5 ms) of the CDSC design. It can be seen from Fig. 6(c) that under explicit information of HSs, itDSC can be flexibly designed with small time delays and less filter blocks compared to the DSC methods. Another version of cascaded itDSC design is shown Fig. 7 where the time delay is selected at $T/25$ and the total delay-time equals $2 \times t_d = 2 \times T/25$ (1.6 ms). As seen from Fig. 7, the comparative performance of the CDSC and CitDSC shows the benefits of the fast-dynamic response of filtering with arbitrary time delays of itDSC. The left figures show the three-phase signals including the original contaminated one, filtered signals from the CDSC and CitDSC, named by U(V), U_{DSC}(V), and U_{itDSC} (V), respectively.

The typical HS components ($h_x = -1$, 5) suddenly occur at $t = 0.05$ (s) in simulation. The right figures show errors in the relevant signals compared to the FFPS one (h_1). The error signals in the left figures are obtained by subtracting each signal, i.e., U(V), U_{DSC}(V), and U_{itDSC} (V) to the FFPS U_{h1}(V). The dynamic responses of CDSC and CitDSC are therefore observed from the relevant error signals, namely, U_{DSChx} (V) and U_{itDSChx} (V) shown in the left side of Fig. 7. That is, the cascaded DSC takes almost ($T/4+T/8 = 7.5$ ms) to filter out the signal where the cascades itDSC takes only ($2 \times T/25 = 1.6$ ms) to filter out the undesired components. Fig. 7(b) shows the validation from the experiment with the error signals relevant to the simulated results in Fig. 7(a).

The results shown in Figs. 6 and 7 confirm the benefits of the new itDSC design on:

1) generalization characteristic;
2) fast dynamic response; and
3) flexible grouping by suitable time delays to simplify the cascade structure.

These advantages are especially beneficial in power electronic applications where the HS components are partially explicit with dominant harmonic orders.

C. Enhanced Filter Performance and Robustness Under Implicit HSs

This section shows the superiority of the itDSC design in case of implicit HS. In power electronics and power systems,

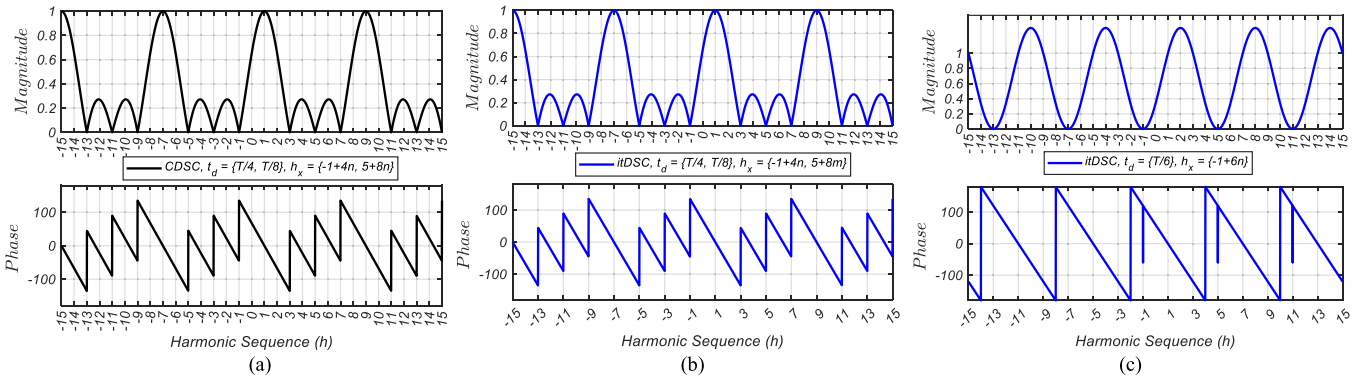

Fig. 6. Comparative magnitude and phase response of the CDSC and itDSC for filtering specific HS components ($h_x = -1, 5$). (a) Cascaded DSC with $t_d = \{T/4;\ T/8\}$ for $h_x = \{-1, 5\}$, respectively. (b) Cascaded itDSC with $t_d = \{T/4;\ T/8\}$ for $h_x = \{-1, 5\}$. (c) Single itDSC with $t_d = T/6$ for $h_x = \{-1, 5\}$.

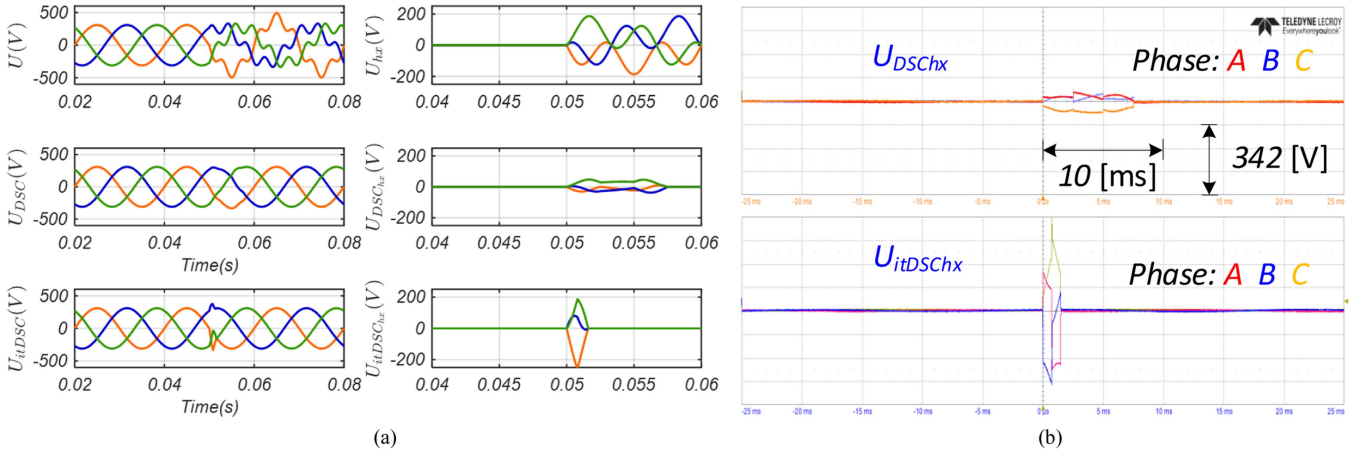

Fig. 7. Comparative performance on filtering/extracting HSs in case of $h_1 = 1$, $h_x = \{-1, 5\}$ where CDSC with $t_d = \{T/4,\ T/8\}$ and itDSC with $t_d = T/25 + T/25$. (a) Simulation results. (b) Experimental results.

the contaminated HS components can be implicit with implicit harmonic order and sequence (e.g., the original noises are not multiple order of the FF). That is, there is only some available information on some sidebands without precise HS order such as the sidebands near negative sequence ($h_x = -1$), fifth harmonics ($h_x = 5$), and other typical bands (e.g., $h_x = 7$, 11, 13, etc.). Note that this case is typical in power electronic applications. In this context, the itDSC can be flexibly designed to enhance the filtering performance around the mentioned harmonic sidebands and a single HSF design can aim at multiple sidebands at once to reduce the computation burden by significantly reducing the cascaded HSFs.

Fig. 8 shows the comparative frequency responses of two designs to filter out a specific range of HS where the order and sequence of harmonics are not precisely known. HSs simultaneously exist in a range of $h_x = [-14,+15]$ with dominant sidebands around $h_x = \{5, 7, 11, 13\}$ as typical ones in power electronic applications. The filter design is enhanced at the mentioned sidebands by additional itDSC filters. The frequency response shown in Fig. 8 exhibits the advantages of the proposed itDSC on further restraining the sidebands around the specific harmonic orders. This performance is beneficial in practice where the harmonics are not explicitly occurring into sidebands of specific integer orders.

Fig. 9 shows the comparative performance under the case of implicit HS in the sidebands of $h_x = \{[-0.5\ ,\ -1]\ ,\ [4,\ 4.5]\}$ where the extra itDSC filters at $h_x = \{-0.5,\ 4.5\}$, $t_d = T/55$ were added to the conventional CitDSC at $T/2$, $T/4$, …$T/64$. The CitDSC shows better performance with smaller SSEs of about 10 [V] compared to the SSE of 23 [V] from the conventional CDSC $\{T/2;\ T/4,\ \ldots,\ T/64\}$ as observed from Fig. 9. As seen in Fig. 9(b), the enhanced itDSC shows it advantage on removing the low-order HS, which is a challenge to the conventional DSC.

D. Robustness Under Mismatches of FF

Another advantage of the itDSC is the independence of the time delay on the parameters, such as FF and targeted harmonic orders (h_1, h_x). Hence, it is expected to be more robust in case of nonadaptive time delays and there is a change/mismatch in the FF. Fig. 10 shows the comparative extracting performance in case of frequency mismatches (true FF of $f_1 = 49$ Hz where the time-delays are designed from the FF of 50 Hz and harmonics, $h_x = \{-1, 5\}$. As seen in Fig. 10(a), the proposed CitDSC shows

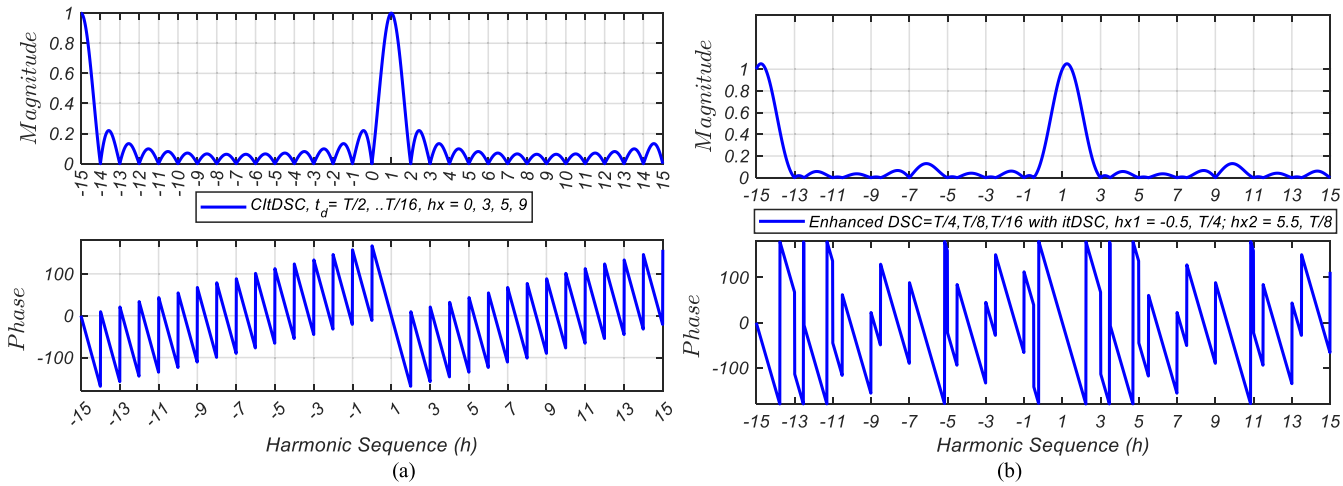

Fig. 8. Comparative frequency response of the itDSC design for a full range of HS components ($h_x = -14 \rightarrow 15$). (a) Cascaded itDSC design on $h_x = 0, 3, 5, 9, 17$ with $t_d = \{T/2, T/4, T/8, T/16\}$, which is equivalent to CDSC. (b) Enhanced itDSC design with $t_{d1} = T/4$, $h_x = -0.5$, $t_{d2} = T/8$, $h_{x2} = 5.5$, and DSC at $\{T/4, T/8, T/16\}$.

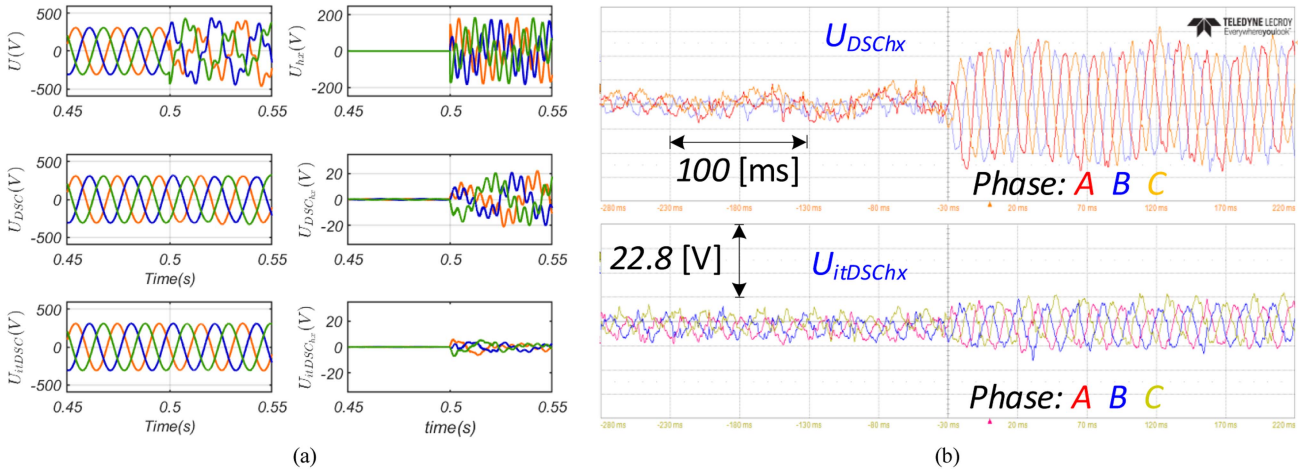

Fig. 9. Comparative performance on extracting FFPS from implicit harmonic components, i.e., $h_x \in \{[-0.5, -1], [4, 4.5]\}$ where the itDSC is enhanced with $t_d = T/55$ for two filters at $h_x = \{-0.5, 4.5\}$. (a) Comparative performance from simulation. (b) Comparative filter errors from experiment results.

more robustness with smaller errors [unfiltered component amplitude of 8(V) compared to 22(V) of the CDSC]. Fig. 10(b) verifies the results from experiments. It is noted that the itDSC still shows its faster dynamic response compared to the DSC. When there is a mismatch in the information of FF (50 Hz versus 49 Hz), the dependent time delays on DSC methods, such as $T/2$ and $T/4$ affect the performance of the whole filters/extractor. Meanwhile, due to the independence time delay of the itDSC, the proposed method shows more robustness to the mismatch of the fundamental period (T) with smaller filtering errors.

E. Robustness and Dynamic Response Under Critical Changes of Parameters

This subsection investigates the critical cases on the HS filter/extraction task in power electronics of microgrids where the HS component is not specifically known, but only side-band information is available (unclear information on h_x). Also, the parameters of FF component are subjected to change in operation (i.e., frequency, phase, and magnitude). For fair comparison under the change of fundamental period (T), the adaptive-frequency mechanism is applied to all HSF methods as shown in Fig. 5(a). Fig. 11 shows the comparative performance under step-change of frequency ($50 \rightarrow 52$ [Hz]) while the harmonic noises are implicit in the band of $[-1, 0]$ and $[4, 4.5]$ as the previous case shown in Fig. 9.

As seen in Fig. 11, the itDSC shows its accuracy on filter/extracting performance with smaller errors and cleaner extract waveforms. The superior performance results in better frequency estimation as shown in Fig. 11(b). It is worth noting that even if the filter/extractor is faster, due to the same FLL setting, the dynamic of frequency estimation shows the same dynamic

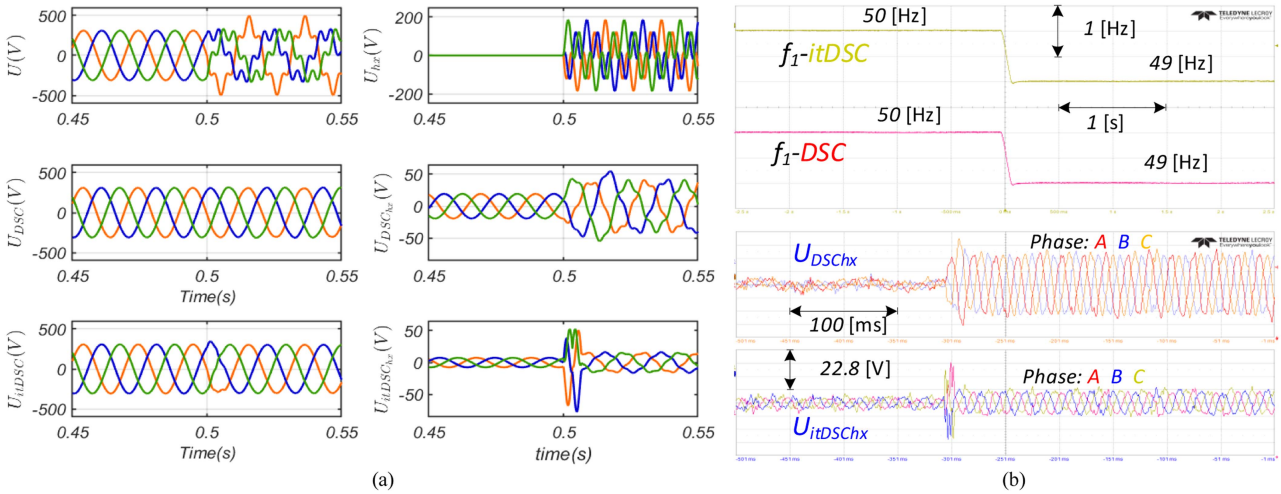

Fig. 10. Comparative performance on nonadaptive time delays for the case of mismatched time delays due to the mismatch of FF, $f_1 = 49$ Hz where the design time delay based on $T = 1/50$ [s]. (a) Comparative simulation results. (b) Comparative experiment results.

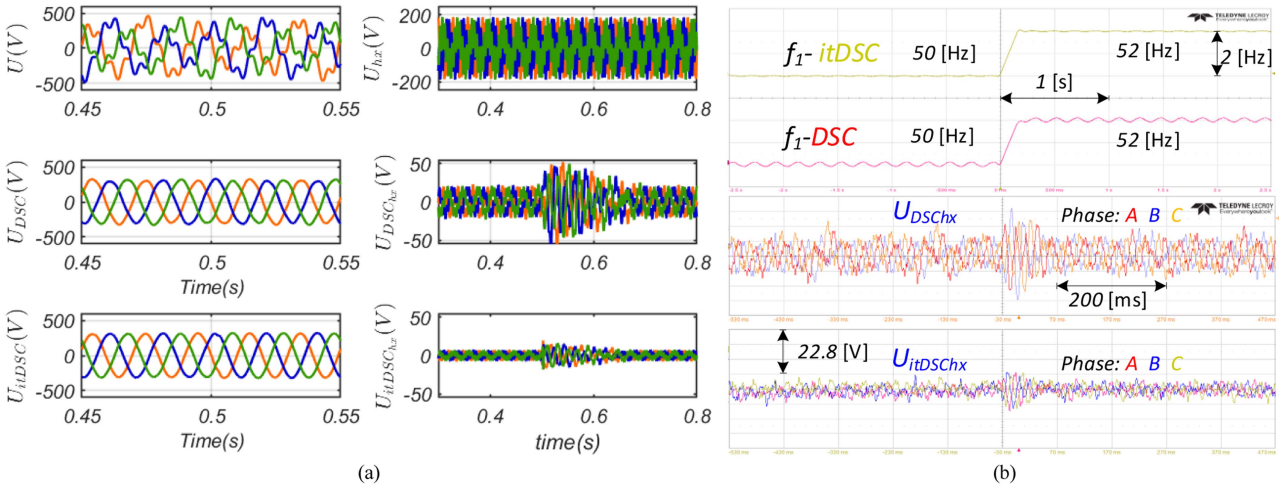

Fig. 11. Dynamic response of the filters/extractors under a step-change of FF, $\Delta f = +2$[Hz] and implicit harmonic noises in some sidebands. (a) Comparative simulation results. (b) Comparative experiment results.

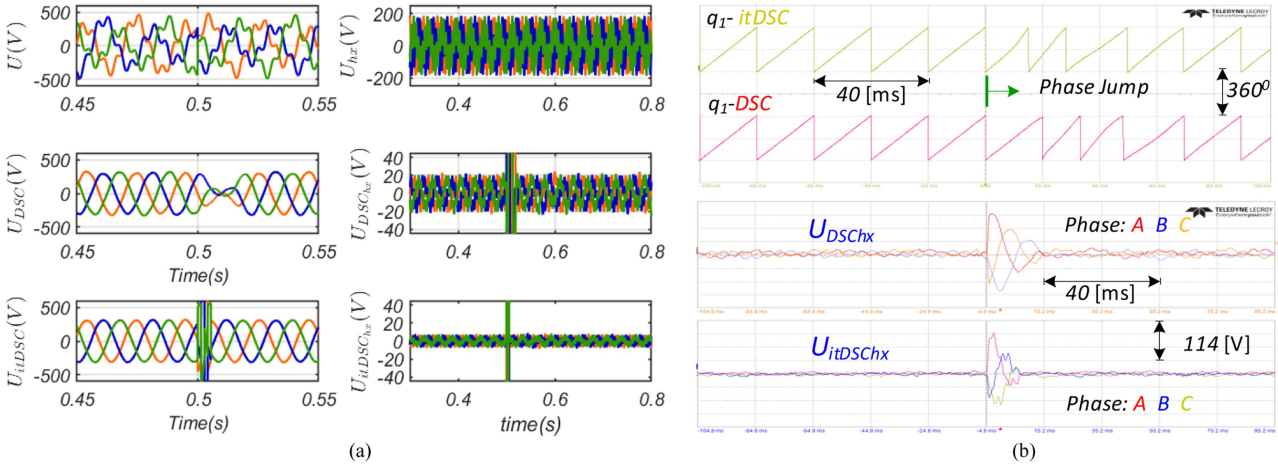

Fig. 12. Dynamic response of the filters/extractors under step-change of phase-angle $\Delta\phi = 180°$ and implicit harmonic noises in some sidebands. (a) Comparative simulation results. (b) Comparative experiment results.

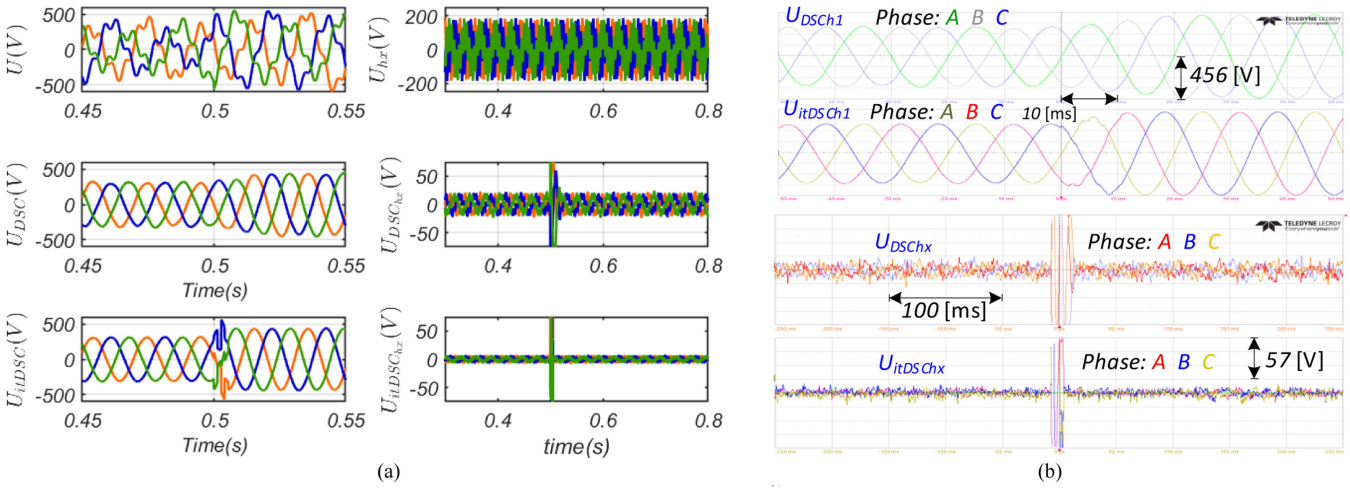

Fig. 13. Dynamic response of the filters/extractors under step-change of magnitude, $\Delta m = 40\%$ (0.4 pu) and implicit harmonic noises in some sidebands. (a) Comparative simulation results. (b) Comparative experiment results.

response of frequency estimation. This issue can be considered as the bottleneck between HSF and FF extraction problems where the HSF performance depends on the parameters of the FF components and vice versa. In this aspect, the robustness of the itDSC design against the mismatches of the FF parameters is an advantage.

The superiority is also observed in the other two cases when the FFPS is step-changed in phase and magnitude. Faster dynamic response and smaller errors are observed from both simulation and validation experiment results in Figs. 12 and 13. The superiority can be explained from the theory analyses on the advantages of the proposed itDSC including short time delay, flexible designs for implicit harmonics, accurate filtering with arbitrary targeted HS components, and robustness under mismatch parameters.

V. Conclusion

This article proposed a new type of HSF named itDSC with fast dynamic response targeting filter/extraction of arbitrary HS components. The prominent advantage is the independence of time delays from the targeted HS indices and fundamental period, which can improve the dynamic response and robustness of applications. The proposed method shows its high potential for applications in power electronics and power systems where the information of harmonics such as orders and sequences are implicit and roughly known as sidebands. The proposed itDSC can turn into the general DSC as a generalization characteristic while enhancing restraints on the specifically targeted HS sidebands. The filters can be designed to directly filter out a group of HS components, which is not necessarily a multiplier of the fundamental one, especially the low-order HS. The proposed itDSC has high potential to combine other intelligent HS detection mechanisms in adaptive approaches and fast response dynamic control.

References

[1] N. Patel, R. C. Bansal, A. A. Adam, A. Elnady, and A.-K. Hamid, "Multimode control for power quality improvement in an electronically coupled distributed generation unit under grid connected and autonomous modes," *IEEE Trans. Power Del.*, vol. 38, no. 4, pp. 2274–2289, Aug. 2023, doi: 10.1109/TPWRD.2023.3237835.

[2] X. Liang, "Emerging power quality challenges due to integration of renewable energy sources," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 855–866, Mar./Apr. 2017, doi: 10.1109/TIA.2016.2626253.

[3] F. Chishti, S. Murshid, and B. Singh, "Frequency adaptive multistage harmonic oscillator for renewable-based microgrid under nonideal grid conditions," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 358–369, Jan. 2021, doi: 10.1109/TIE.2020.2965474.

[4] S. M. Hoseinizadeh, S. Ouni, H. Karimi, M. Karimi-Ghartemani, and K. L. Lian, "Comparison of PLL-based and PLL-less vector current controllers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 436–445, Feb. 2022, doi: 10.1109/JESTPE.2021.3066512.

[5] M. S. Reza, M. M. Hossain, and V. G. Agelidis, "A method without stability issue for robust estimation of three-phase grid frequency," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 3, pp. 854–859, Jul. 2022, doi: 10.1109/JESTIE.2021.3074886.

[6] L. Sun, K. Sun, Y. Hou, and J. Hu, "Optimized autonomous operation control to maintain the frequency, voltage and accurate power sharing for DGs in Islanded systems," *IEEE Trans. Smart Grid*, vol. 11, no. 5, pp. 3885–3895, Sep. 2020, doi: 10.1109/TSG.2020.2992802.

[7] D. Jovcic, "Phase locked loop system for FACTS," *IEEE Trans. Power Syst.*, vol. 18, no. 3, pp. 1116–1124, Aug. 2003, doi: 10.1109/TPWRS.2003.814885.

[8] D. Somayajula and M. L. Crow, "An integrated dynamic voltage restorer-ultracapacitor design for improving power quality of the distribution grid," *IEEE Trans. Sustain. Energy*, vol. 6, no. 2, pp. 616–624, Apr. 2015, doi: 10.1109/TSTE.2015.2402221.

[9] M. Kashif et al., "A fast time-domain current harmonic extraction algorithm for power quality improvement using three-phase active power filter," *IEEE Access*, vol. 8, pp. 103539–103549, 2020, doi: 10.1109/ACCESS.2020.2999088.

[10] A. Meligy, T. Qoria, and I. Colak, "Assessment of sequence extraction methods applied to MMC-SDBC STATCOM under distorted grid conditions," *IEEE Trans. Power Del.*, vol. 37, no. 6, pp. 4923–4932, Dec. 2022, doi: 10.1109/TPWRD.2022.3162959.

[11] X. Liu, B. Wu, and L. Xiu, "A fast positive-sequence component extraction method with multiple disturbances in unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8820–8824, Aug. 2022, doi: 10.1109/TPEL.2022.3161734.

[12] N. Hui, Z. Luo, Y. Feng, and X. Han, "A novel grid synchronization method based on hybrid filter under distorted voltage conditions," *IEEE Access*, vol. 8, pp. 65636–65648, 2020, doi: 10.1109/ACCESS.2020.2981946.

[13] Y. Khayat et al., "Decentralized frequency control of AC microgrids: An estimation-based consensus approach," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5183–5191, Oct. 2021, doi: 10.1109/JESTPE.2020.2980675.
[14] M. Ganjian-Aboukheili, M. Shahabi, Q. Shafiee, and J. M. Guerrero, "Seamless transition of microgrids operation from grid-connected to islanded mode," *IEEE Trans. Smart Grid*, vol. 11, no. 3, pp. 2106–2114, May 2020, doi: 10.1109/TSG.2019.2947651.
[15] IEEE, "IEEE STD 1547-2018," *IEEE Standard Interconnect. Interoperability Distrib. Energy Resour. with Assoc. Electr. Power Syst. Interfaces*, pp. 1–138, 2018.
[16] P. Roncero-Sánchez, X. Del Toro García, A. P. Torres, and V. Feliu, "Robust frequency-estimation method for distorted and imbalanced three-phase systems using discrete filters," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1089–1101, 2011, doi: 10.1109/TPEL.2011.2107580.
[17] S. Golestan and J. M. Guerrero, "Conventional synchronous reference frame phase-locked loop is an adaptive complex filter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1679–1682, Mar. 2015, doi: 10.1109/TIE.2014.2341594.
[18] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A method to improve the dynamic performance of moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5978–5990, Oct. 2015, doi: 10.1109/TPEL.2014.2381673.
[19] Q. Huang and K. Rajashekara, "An improved delayed signal cancellation PLL for fast grid synchronization under distorted and unbalanced grid condition," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4985–4997, Sep. 2017, doi: 10.1109/TIA.2017.2700282.
[20] Y. F. Wang and Y. W. Li, "Three-phase cascaded delayed signal cancellation PLL for fast selective harmonic detection," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1452–1463, Apr. 2013, doi: 10.1109/TIE.2011.2162715.
[21] S. Gude and C. C. Chu, "Dynamic performance improvement of multiple delayed signal cancelation filters based three-phase enhanced-PLL," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5293–5305, Sep./Oct. 2018, doi: 10.1109/TIA.2018.2819131.
[22] X. Li and F. Gao, "A three-sample filter for fast arbitrary harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 5122–5131, May 2022, doi: 10.1109/TIE.2021.3078398.
[23] C. M. Hackl and M. Landerer, "Modified second-order generalized integrators with modified frequency locked loop for fast harmonics estimation of distorted single-phase signals," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3298–3309, Mar. 2020, doi: 10.1109/TPEL.2019.2932790.
[24] C. Hackl and M. Landerer, "A unified method for generic signal parameter estimation of arbitrarily distorted single-phase grids with DC-offset," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 235–246, 2020, doi: 10.1109/OJIES.2020.3017379.
[25] H. Nguyen and J. W. Jung, "Disturbance-rejection-based model predictive control: Flexible-mode design with a modulator for three-phase inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2893–2903, Mar. 2018, doi: 10.1109/TIE.2017.2758723.
[26] T. D. Do and H. T. Nguyen, "A generalized observer for estimating fast-varying disturbances," *IEEE Access*, vol. 6, pp. 28054–28063, 2018, doi: 10.1109/ACCESS.2018.2833430.
[27] S. Gude and C. C. Chu, "Three-phase PLLs by using frequency adaptive multiple delayed signal cancellation prefilters under adverse grid conditions," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3832–3844, Jul./Aug. 2018, doi: 10.1109/TIA.2018.2823263.
[28] S. C. Gulipalli, S. Gude, S. C. Peng, and C. C. Chu, "Multiple delayed signal cancellation filter-based enhanced frequency-locked loop under adverse grid conditions," *IEEE Trans. Ind. Appl.*, vol. 58, no. 5, pp. 6612–6628, Sep./Oct. 2022, doi: 10.1109/TIA.2022.3180325.
[29] F. A. S. Neves, M. C. Cavalcanti, H. E. P. De Souza, F. C. Bradaschia, E. J. Bueno, and M. Rizo, "A generalized delayed signal cancellation method for detecting fundamental-frequency positive-sequence three-phase signals," *IEEE Trans. Power Del.*, vol. 25, no. 3, pp. 1816–1825, Jul. 2010, doi: 10.1109/TPWRD.2010.2044196.
[30] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014, doi: 10.1109/TPEL.2013.2273461.
[31] H. T. Nguyen et al., "Fast harmonic rejecting control design to enable active support of charging stations to micro-grids under distortion," *IEEE Trans. Transp. Electrif.*, vol. 9, no. 3, pp. 4132–4146, Sep. 2023, doi: 10.1109/TTE.2023.3241392.
[32] N. T. Hoach, A. S. Al-Sumaiti, K. Al Hosani, and M. S. Elmoursi, "Multifunctional control of wind-turbine based nano-grid connected to distorted utility-grid," *IEEE Trans. Power Syst.*, vol. 37, no. 1, pp. 576–589, Jan. 2022, doi: 10.1109/TPWRS.2021.3093713.

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