Session 32 Overview: *Frequency Synthesizers*

RF SUBCOMMITTEE

Session Chair:
Wei Deng
Tsinghua University, Beijing, China

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Jaehyouk Choi
KAIST, Daejeon, Korea

Session Moderator:
Wanghua Wu
Samsung, San Jose, CA

This session presents the latest advances in digital and analog phase-locked loops (PLLs) and FMCW chirp generators from 2.4 to 60GHz for high-performance wireless applications.

8:30 AM

32.1 A 365fs$_{rms}$-Jitter and −63dBc-Fractional Spur 5.3GHz-Ring-DCO-Based Fractional-N DPLL Using a DTC Second/Third-Order Nonlinearity Cancelation and a Probability-Density-Shaping ΔΣM

Hangi Park, KAIST, Daejeon, Korea

In Paper 32.1, KAIST presents a low-jitter and low-spur fractional-N ring-DPLL that performs a DTC second/third-order nonlinearity cancelation and employs a probability-density-shaping ΔΣM. At near-integer frequencies (worst case), the rms jitter and fractional spurs are less than 365fs and -63dBc, respectively.

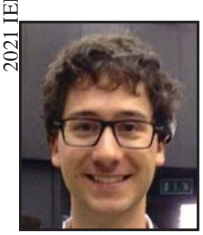
8:38 AM

32.2 A 14nm Analog Sampling Fractional-N PLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 80fs Integrated Jitter and 93fs at Near-Integer Channels

Wanghua Wu, Samsung Semiconductor, San Jose, CA

In Paper 32.2, Samsung Semiconductor demonstrates a 6GHz 14nm analog sampling fractional-N PLL with a DTC range reduction technique. It achieves an rms jitter of 80fs (integrated from 10kHz to 40MHz) and -72.4dB fractional spur at 14.2mW power consumption. The PLL also supports a low-power mode with 91.5fs$_{rms}$ jitter and 8.2mW power consumption.

8:46 AM



32.3 A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter

Mario Mercandelli, Politecnico di Milano, Milan, Italy

In Paper 32.3, Politecnico di Milano presents a fractional-N bang-bang digital PLL that overcomes the typical quantization-noise limit of bang-bang phase detectors by employing an adaptively calibrated noise-shaping technique to the single-bit phase detector. Consuming 10.8mW, the PLL achieves a 107.6fs integrated jitter, which is at par with state-of-the-art analog PLLs.

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8:54 AM

32.4 A 104fs$_{rms}$-Jitter and –61dBc-Fractional Spur 15GHz Fractional-N Subsampling PLL Using a Voltage-Domain Quantization-Error Cancelation Technique

Juyeop Kim, KAIST, Daejeon, Korea

In Paper 32.4, KAIST presents a 14-to-16GHz low-jitter fractional-N SSPLL that cancels the quantization error (Q-error) in the voltage domain. The measured rms jitter and fractional spur were 104fs and –61dBc near 15GHz.

9:02 AM

32.5 A 24GHz Self-Calibrated ADPLL-Based FMCW Synthesizer with 0.01% rms Frequency Error Under 3.2GHz Chirp Bandwidth and 320MHz/μs Slope

Zhengkun Shen, Peking University, Beijing, China

In Paper 32.5, Peking University introduces a 24GHz self-calibrated ADPLL-based FMCW synthesizer. The synthesizer uses a self-calibration scheme with adaptive overlap compensation and continuous ramp tracking. The synthesizer achieves a 3.2GHz chirp bandwidth and 320MHz/ms slope.

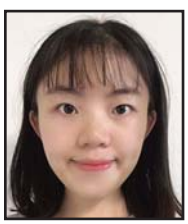
9:10 AM

32.6 A K-Band 12.1-to-16.6GHz Subsampling ADPLL with 47.3fs$_{rms}$ Jitter Based on a Stochastic Flash TDC and Coupled Dual-Core DCO in 16nm FinFET CMOS

Edwin Thaller, Intel, Villach, Austria

In Paper 32.6, Intel presents a 12.1-to-16.6GHz sub-sampling ADPLL that is based on a stochastic flash TDC and a coupled dual-core DCO. It is implemented in 16nm FinFET CMOS and achieves 47.3fs$_{rms}$ jitter performance at 56mW power dissipation.

9:14 AM



32.7 A 32kHz-Reference 2.4GHz Fractional-N Oversampling PLL with 200kHz Loop Bandwidth

Junjun Qiu, Tokyo Institute of Technology, Tokyo, Japan

In Paper 32.7, Tokyo Institute of Technology demonstrates a 32kHz-reference 2.4GHz fractional-N oversampling PLL, which captures amplitude/phase information of the reference and realizes 256 phase detections per reference cycle. It realizes 200kHz loop bandwidth and 5.79ps$_{rms}$ jitter in the fractional mode with 4.97mW power consumption.

9:22 AM

32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays

Alessio Santiccioli, Politecnico di Milano, Milano, Italy

In Paper 32.8, Politecnico di Milano reports a 12.9-to-15.1GHz digital bang-bang PLL-based LO phase-shifting system. Implemented in 28nm CMOS, it achieves 98.4fs$_{rms}$ jitter at 10.8mW power and 0.6° rms accuracy.