Session 10 Overview: *Continuous-Time ADCs and DACs*

DATA CONVERTER SUBCOMMITTEE

Session Chair:
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Continuous-time ΔΣ ADCs offer compact silicon area and low power consumption for various applications. The first two papers in this session present different techniques in continuous-time ΔΣ ADCs for audio applications and achieve impressive figures of merit. The third paper describes a new hybrid CT/DT loop architecture for a ΔΣ modulator without requiring any calibration or tuning. The fourth paper proposes a CT loop filter with DT noise shaping achieving 4th-order noise shaping using a single OTA. The fifth paper introduces a pipelined ADC with a 1st stage SAR and 2nd stage 2×-time-interleaved CT incremental ΔΣ ADC. The last two papers in this session describe techniques utilized to achieve high-linearity multi-GHz DACs. The sixth paper describes a 16GS/s DAC for software radio base stations. The last paper presents a 64GS/s DAC for BIST of RF sampling ADCs.

7:00 AM

10.1 A 116μW 104.4dB-DR 100.6dB-SNDR CT ΔΣ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage Compensated Off-Transistor-Based Bias Noise Filter

Chilun Lo, Samsung Electronics, Hwaseong, Korea

In Paper 10.1, Samsung Electronics presents a 116μW audio-band CT ΔΣ ADC using a tri-level current-steering DAC with a gate-leakage-compensated noise filter that achieves 104.4dB dynamic range in 24kHz bandwidth resulting in a 187.5dB Schreier FoM.

7:08 AM

10.2 A 139μW 104.8dB-DR 24kHz-BW CTΔΣM with Chopped AC-Coupled OTA-Stacking and FIR DACs

Somok Mondal, University of California, San Diego, La Jolla, CA, now with Apple, San Diego, CA

In Paper 10.2, the University of California San Diego reports a CT ΔΣM for audio applications with chopped AC-coupled OTA-stacking and FIR DACs that achieves 104.8dB dynamic range in a 24kHz bandwidth and consumes 139μW resulting in a 187.2dB Schreier FoM.

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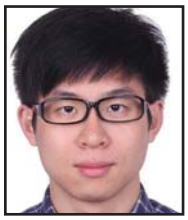
7:16 AM



10.3 A 100MHz-BW 68dB-SNDR Tuning-Free Hybrid-Loop DSM with an Interleaved Bandpass Noise-Shaping SAR Quantizer

Lu Jie, University of Michigan, Ann Arbor, MI

In Paper 10.3, University of Michigan describes a tuning-free hybrid-loop ΔΣ modulator with an interleaved bandpass noise-shaping SAR quantizer that achieves 68dB SNDR in a 100MHz bandwidth.

7:24 AM

10.4 A 3.7mW 12.5MHz 81dB-SNDR 4th-Order CTDSM with Single-OTA and 2nd-Order NS-SAR

Wei Shi, University of Texas, Austin, TX

In Paper 10.4, University of Texas at Austin presents a 4th-order CT ΔΣ modulator with single-OTA and 2nd-order NS-SAR that achieves 81dB-SNDR in 12.5MHz bandwidth and consumes 3.7mW.

7:32 AM

10.5 A 12b 600MS/s Pipelined SAR and 2×-Interleaved Incremental Delta-Sigma ADC with Source-Follower-Based Residue-Transfer Scheme in 7nm FinFET

Seungyeob Baek, Samsung Electronics, Hwasung, Korea

In Paper 10.5, Samsung Electronics reports a 12b 600MS/s pipelined SAR and 2×-interleaved Incremental ΔΣ ADC in 7nm FinFET.

7:40 AM

10.6 A 12b 16GS/s RF-Sampling Capacitive DAC for Multi-Band Soft-Radio Base-Station Applications with On-Chip Transmission-Line Matching Network in 16nm FinFET

Daniel Gruber, Intel, Villach, Austria

In Paper 10.6, Intel describes a 12b 16GS/s RF-sampling capacitive DAC for multi-band soft-radio base-stations in 16nm FinFET.

7:48 AM

10.7 A 64GS/s 4×-Interpolated 1b Semi-Digital FIR DAC for Wideband Calibration and BIST of RF-Sampling A/D Converters

Martin Clara, Intel, Santa Clara, CA

In Paper 10.7, Intel presents a 64GS/s 4×-interpolated 1b semi-digital FIR DAC for wideband calibration and BIST of RF-sampling A/D converters.