F6: *Optical and Electrical Transceivers for 400GbE and Beyond*

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The proliferation of 400Gb/s Ethernet (400GbE) in our computing and networking infrastructure is stimulating rapid transformations in our wireline links. A wide array of new technologies are under research to support next-generation 800GbE in the areas of optics, packaging, modulation, coding, and of course transceiver architectures and circuits. Over the past two decades, progress on wireline interface bandwidth scaling has followed a relatively clear path. But, for many, the coming years seem less certain. In this forum, eight experts illuminate the future, sharing their diverse expertise across the broad range of topics that promise to impact optical and electrical transceiver R&D in the 2020's.

The forum begins with an overview of optical transceivers for 400GbE and beyond, surveying market needs, technology options, and an overview of the key challenges. Next, two presentations describe silicon photonic transceiver and device technologies with the potential for low-power optical interconnects above 100Gb/s per lane. Direct-detection transceiver circuits for micro-ring modulator links are described, promising low-power dense wavelength-division multiplexed links. The latest research on silicon photonics for spatial-division multiplexing and single-sideband modulation are also described. A fourth presentation reviews the modeling and compensation of VCSEL nonlinearity and bandwidth limitations in pursuit of low-cost 100+Gb/s optical transmission. Finally, modulation, equalization, and transceiver architectures for 200+Gb/s per-wavelength coherent optical links are presented.

Next, the forum turns toward the electrical interfaces required in support of 400GbE and beyond. The theoretical limits of signaling over electrical interconnect between chips are established. In pursuit of those limits, new combinations of modulation, coding, and signal processing are considered and compared. Different transceiver architectures are likely to emerge for different applications. Implementations are considered in the final two talks.

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Inside 400GE Optical Modules

Mark Nowell, *CISCO Systems, Kanata, ON, Canada*

Driven by the demand for increased capacity, networks are now deploying 400Gb/s Ethernet and the industry is looking forward to what is next. New optical and electrical interconnect technologies and transceivers are emerging to enable the transition. This forum begins by looking at the challenges for these interfaces and the underlying technologies and approaches that are being considered as solutions.

Mark Nowell is a Cisco Fellow in Cisco's Data Center Business Unit. His focus is on next generation interconnect technology innovation to meet Cisco's needs. Mark is also active within the industry standards and forums and has chaired multiple IEEE 802.3 Ethernet projects. He represents Cisco on various industry alliances and Consortia. Mark also chairs a number of industry MSA (Multi-Source Agreement) groups focusing on next generation optical module form factors (QSFP-DD, QSFP-DD800) and optical interface signaling technologies (100G Lambda MSA).

100+Gb/s PAM4 Silicon-Photonic Optical Transceivers

Ganesh Balamurugan, *Intel, Hillsboro, OR*

Hybrid-integrated optical transceivers based on silicon photonic and CMOS ICs offer a compelling solution for low-cost 100+G PAM4 interconnects. In this talk, we will highlight system and circuit level aspects of the design of such transceivers. In particular, we will focus on ultra-compact micro-ring modulator-based (MRM-based) PAM4 transmitters and present techniques to electronically compensate for their electro-optic nonlinearity. We will also cover MRM thermal control methods which are essential to compensate for process and temperature variations. On the receiver side, we will highlight design techniques used to meet the bandwidth and noise requirements of 100+G PAM4 optical front-ends using mainstream bulk CMOS processes. We will present design details and measured results from our recent 112G PAM4 optical transceiver prototypes to demonstrate the proposed techniques and also indicate directions for further research.

Ganesh Balamurugan received the B.Tech degree in electronics and communication engineering from the Indian Institute of Technology, Madras in 1996, the M.S. degree in electrical and computer engineering from the University of Texas at Austin in 1998, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 2004. Since 2004, he has been with Intel Corporation working on high-speed wireline links. His research interests include energy-efficient electrical and optical link design, silicon photonics-based communication circuits and system-level optimization of electro-optic links. He is currently a principal engineer leading the silicon photonics circuits research group at Intel Labs.

Silicon Photonics for Spatial-Division Multiplexing and Advanced Optical Transceivers

Hon Ki Tsang, *The Chinese University of Hong Kong, Shatin, Hong Kong*

Spatial-division multiplexing (SDM), mode-division multiplexing (MDM), and new implementations of coherent optical communications can provide the high bandwidth density and low power consumption needed for data center interconnects. We present our recent work on the use of micro-ring modulators (MRM) and Ge-Si electro-absorption modulators (EAMs) with novel waveguide grating couplers for enabling MDM in few-mode fibers, and SDM in multicore fiber (MCF) for the next 4× increase in bandwidth density.

Hon Ki Tsang received the B.A. (Hons) in 1987 and the Ph.D. in 1991 from the University of Cambridge. He has been with the Department of Electronic Engineering, The Chinese University of Hong Kong (CUHK) since 1993. In 2002-03, he was a Director at Bookham Technology plc (UK), which developed some of the first silicon-waveguide-based products (most notably the silicon electronic variable optical attenuators) to be deployed in telecommunication networks. His research on silicon photonics spans over two decades, and he was elevated to Fellow of OSA and a Fellow of IEEE for his contributions to advanced waveguide grating couplers and nonlinear silicon photonics. He is also currently the Editor-in-Chief of the IEEE Journal of Quantum Electronics.

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VCSEL-Based Optical Transmitters Above 100Gb/s

Urs Hecht, *TU Berlin, Berlin, Germany*

This talk gives an overview of transmitter systems for VCSELs, which are vertically produced, low-cost, high-efficiency LASERs. The fastest NRZ systems using directly modulated VCSELs have not succeeded 80Gbit/s and surprisingly, PAM-4 systems are even slower. To surpass the 100Gbit/s threshold, a model of a VCSEL is presented and a custom equalization scheme which optimizes PAM-4 transmission is proposed. With the scheme being verified by transmission measurements, a transmitter optimized for the new scheme is designed.

Urs Hecht received the B.Sc. and M.Sc. degrees in electrical engineering in 2016 and 2018, respectively, from the Technische Universität Berlin. During his studies, he concentrated on analog circuit design. His Master's Thesis "56 GBaud PAM-4 CMOS Transmitter Architectures" investigates finding the optimal transmitter equalization architecture to push the boundaries of VCSEL-based optical communication systems beyond 100Gbit/s, and was awarded the Friedrich-Wilhelm Gundlach Award in 2018. He joined as Chair of mixed-signal circuit design at the TU Berlin in May 2018. His main research work involves VCSEL-tailored equalization and data transmission with several publications advancing the state of the art.

DSP and FEC Architectures for Beyond 400Gb/s Data Center Interconnects

Ilya Lyubomirsky, *Inphi, Santa Clara, CA*

The relentless growth of data-center bandwidth requirements is driving innovation in high-speed transceivers. DSP and FEC are key enabling technologies for sustaining the scaling of data-center interconnect speeds, while reducing the cost and energy per bit. In this talk, we present DSP and FEC architectures for future direct-detect and coherent systems for data-center applications.

Ilya Lyubomirsky received a Ph.D. degree in Electrical Engineering from the Massachusetts Institute of Technology in 1999. Early in his career at Telcordia, ONI Systems, and Ciena Corp., Ilya worked on system modeling and design of high-speed packet networks, optical metro networks, and ultra-dense WDM long-haul transmission systems. From 2003 to 2010, he was an Electrical Engineering Faculty member at the University of California, Riverside, teaching and researching on high-capacity direct-detect and coherent optical communication systems. During a stint at Finisar Corp. from 2011 to 2015, Ilya researched advanced modulation formats, DSP algorithms, and coding techniques to enable high-speed optical modules for data-center interconnects. From 2016 to 2017, Ilya led the Facebook engineering team on the Voyager project, successfully demonstrating the world's first 800Gb/s DWDM white box coherent transponder. Ilya joined Inphi Corp. in 2017 to work on coherent DSP architecture and algorithms for 400G ZR. Currently, Ilya is a Senior Technical Director at Inphi, leading the Systems/DSP architecture team on research and development of 400G/800G PAM-4 DSP ASICs. During his career in industry and academia, Ilya has contributed extensively to IEEE 802.3 Ethernet standards, has co-authored more than 50 peer-reviewed journal and conference papers, and is an inventor on 15 patents.

Signalling, Modulation, Coding, and Signal Processing Architectures to support 400GbE and Beyond

Troy Beukema, *IBM Research, Yorktown Heights, NY*

This talk discusses line signaling, modulation/coding options, and I/O architecture approaches to support the high data rates required for state-of-the-art 100Gb/s and beyond electrical-interconnect data transmission systems. A discussion of channel capacity limits derived from system parameters such as channel loss, crosstalk, circuit noise and clock jitter will be covered to gain insight into maximum practical data-rate limits achievable for wireline systems.

Troy J. Beukema received the B.S.E.E. and M.S.E.E. degrees from Michigan Technological University, Houghton, in 1984 and 1988, respectively. Since 1996, he has been with IBM Research, Yorktown Heights, NY, where he has primarily focused on system designs and analysis for high-speed CMOS serial electrical interconnects spanning data rates from 6 to 100Gb/s and higher. His ongoing research activity is in the area of advanced modulation, equalization, and coding intended to extend electrical data rates to 100Gb/s and beyond, with an emphasis on system designs for robust 200Gb/s long-reach electrical links.

112Gb/s-and-Beyond Long-Reach and Short-Reach Electrical Interfaces

Nhat Nguyen, *Rambus, San Jose, CA*

Design challenges associated with LR, VSR, and XSR electrical interfaces at 112Gb/s are described. ADC-based and analog architectures are considered for the overall performance based on signal integrity, SNR constraint, power consumption, silicon area, and design flexibility. The LR interface, up to 36 dB of channel loss, is discussed in the context of backplane and direct-attached cable applications; the VSR interface, up to 22 dB, for pluggable optical modules; and the emerging XSR interface, up to 10 dB, for co-packaged optical modules are also discussed. Finally, some insights into next-generation electrical interfaces at 224Gb/s are shared.

Nhat Minh Nguyen received the B.S. degrees with highest honors in computer engineering, computer science, and mathematics from Portland State University, Portland, OR, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1987 and 1991, respectively. From 1991 to 1995, he was with Hewlett Packard working on RF circuits in standard silicon bipolar technology. He was with MicroUnity in 1996 working on analog circuits for graphic processors. Since 1996 he has been with Rambus working on high-speed and low-power serial links and I/O interfaces for data centers, AI/ML, and computing applications. He is presently a Sr. Technical Director. He has published one book chapter and authored over 30 journal and conference papers. He holds over 30 U.S. patents. His current research interests include multi-level serial links, optical communications, PLL and CDR designs, clocking architectures, memory interfaces, and wideband circuits. Dr. Nguyen was a past Associate Editor of the IEEE Transactions on Circuits and Systems. Presently he is also an adjunct professor at San Jose State University, San Jose, California.

Designs of Communication Circuits for Side-by-Side and Stacked Chiplets

Kenny C.H. Hsieh, *TSMC, Hsinchu, Taiwan*

As CMOS scales deeply, conventional single-die package systems face increasing challenges in performance and cost. As a result, System-in-Package solutions, where multiple chiplets are integrated on various substrates or on top of each other, quickly become mainstream for applications from mobile phones to supercomputers. To take full advantage of the trend, co-optimizing system demand and package technology, as well as new interface circuits bridging between chiplets are all necessary. From a system viewpoint, the interface circuits need transparency to software and minimized power, area, and latency. Here, we will give an overall view of side-by-side and stacked chiplet technologies and outline their potentials and limitations. We will explore circuit techniques for these ultrashort-haul links to overcome challenges in synchronization, interconnect routing, design reuse, and design for testability. We will show how designers deliberate the tradeoffs between hardened and compiled IP. We will also discuss recent design examples achieving high bandwidth and high energy efficiency all at once.

Kenny C. H. Hsieh received his B.S.E.E. degree from National Cheng Kung University, Tainan, Taiwan, and his M.S.E.E. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1985 and 1989 respectively. He designed SRAM and DRAM circuits at Winbond and Etron for 6 years prior to spending 2 years in PLL and Gm-C filter research at the University of California, Irvine. From 1997 to 2012, he designed high-speed SerDes systems at Ohm Technology, LSI/Avago, and Xilinx in California. Mr. Hsieh joined TSMC in 2012 where he is currently a Deputy Director leading a mixed-signal design group. His current research interests include equalization theory for digital communication and design/technology co-optimization of advanced CMOS technologies.

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