Session 25 Overview: *DRAM*

MEMORY SUBCOMMITTEE

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DRAM memories continue to have a significant impact on a wide range of applications, including high-performance graphics, smartphones, server applications, and machine learning. Two 8Gb GDDR6 DRAM papers for next-generation graphics applications show an increase to maximum pin speed to 22-24Gb/s/pin, and a 16Gb LPDDR5 DRAM with sub-1V operation and a 7.14Gb/s/pin IO speed is introduced for low-power mobile applications. Function-in-memory DRAM based on HBM2 is also introduced, which achieves a 1.2TFLOPS programmable computing unit (PCU).

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7:45 AM

25.1 A 24Gb/s/pin 8Gb GDDR6 with a Half-Rate Daisy-Chain-Based Clocking Architecture and IO Circuitry for Low-Noise Operation

Kyunghoon Kim, SK hynix Semiconductor, Icheon, Korea

In Paper 25.1, SK hynix presents a 24Gb/s/pin 8Gb GDDR6 DRAM with half-rate daisy-chain-based WCK tree: with an LC PLL, and I/O circuits optimized for low-noise operation and a wide range supply voltages. Based on its configuration, it performs 1.3× faster than the previously published GDDR6 DRAM.

7:53 AM

25.2 A 16Gb Sub-1V 7.14Gb/s/pin LPDDR5 SDRAM Applying a Mosaic Architecture with a Short-Feedback 1-Tap DFE, an FSS Bus with Low-Level Swing and an Adaptively Controlled Body Biasing in a 3rd-Generation 10nm DRAM

Yong-Hun Kim, Samsung Electronics, Hwaseong, Korea

In Paper 25.2, Samsung Electronics presents a 16Gb sub-1V 7.14Gb/s/pin LPDDR5 DRAM. An innovative mosaic architecture is introduced to increase the density within a limited package size. I/O performance is improved by shortening the length of the top metal and a newly introduced short-feedback SA with dedicated V_{REF}s for a 1-tap DFE. The 1.64× long bus line is managed by a fully-source-synchronous (FSS) bus and a low-level swing (LLS) scheme. To enhance power efficiency and yield, an adaptive body bias (ABB) scheme is used.

8:01 AM

25.3 An 8Gb GDDR6X DRAM Achieving 22Gb/s/pin with Single-Ended PAM4 Signaling

Timothy M. Hollis, Micron Semiconductor, Boise, ID

In Paper 25.3, Micron shows an 8Gb GDDR6X DRAM that features a PAM4 encoded, single-ended I/O to double the per-pin bandwidth for a given data-clock. Three CTLE pre-amplifiers shield the four-phase clocked latches from the pad. A de-emphasis PAM4 transmitter is implemented for read operations. The package is optimized for crosstalk to address the decreased voltage margins of PAM4 signaling. Full device operation exceeding 22Gb/s/pin is demonstrated.

8:09 AM

25.4 A 20nm 6GB Function-In-Memory DRAM, Based on HBM2 with a 1.2TFLOPS Programmable Computing Unit Using Bank-Level Parallelism, for Machine Learning Applications

Young-Cheon Kwon, Samsung Electronics, Hwaseong, Korea

In Paper 25.4, Samsung Electronics shows a HBM2-based function-in-memory DRAM that improves system performance by on-chip data processing and reduces system power consumption by inter-chip data movement. The measurement results show a 2.1× improvement in system performance with a 71% power reduction compared to a conventional system.