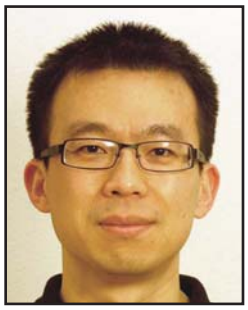
Session 26 Overview:
RF Power-Amplifier and Front-End Techniques

RF SUBCOMMITTEE



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RF PAs and front-end building blocks are critical for the output power, noise, power-efficiency, out-of-band rejection, and antenna impedance tuning of wireless transceivers. The first three papers in this session cover mm-wave PAs with efficiency enhancement techniques for 5G applications. The next paper presents a 28GHz reflection-coefficient sensor for mm-wave antenna-tuner applications. The session continues with two digital-PA papers in sub-6GHz frequency bands with back-off efficiency enhancement. The session concludes with an N-path filter exhibiting impedance transformation and passive voltage gain.

7:00 AM

26.1 A 26-to-60GHz Continuous Coupler-Doherty Linear Power Amplifier for Over-An-Octave Back-Off Efficiency Enhancement

Tzu-Yuan Huang, Georgia Institute of Technology, Atlanta, GA

In Paper 26.1, the Georgia Institute of Technology describes a continuous Marchand Doherty PA. The proposed PA demonstrates the broadband saturation performance of P_{sat}>18.3dBm and peak PAE>23.3% from 26 to 60GHz.

7:08 AM

26.2 A Doherty-Like Load-Modulated Balanced Power Amplifier Achieving 15.5dBm Average P_{out} and 20% Average PAE at a Data Rate of 18Gb/s in 28nm CMOS

Valdrin Qunaj, KU Leuven - MICAS, Leuven, Belgium

In Paper 26.2, KU Leuven presents a Doherty-like load-modulated balanced amplifier achieving 15.5dBm of average output power and 20% average efficiency at the data-rate of 18Gb/s in 28nm bulk CMOS.

7:16 AM

26.3 A mm-Wave Power Amplifier for 5G Communication Using a Dual-Drive Topology Exhibiting a Maximum PAE of 50% and Maximum DE of 60% at 30GHz

Edgar Felipe Garay, Georgia Institute of Technology, Atlanta, GA

In Paper 26.3, the Georgia Institute of Technology shows a dual-drive PA core architecture that exploits the concurrent driving of the gate/source terminals. This design achieves the maximum PAE of 50% and maximum DE of 60% at 30GHz.

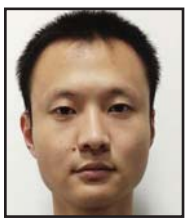
7:24 AM

26.4 A Reflection-Coefficient Sensor for 28GHz Beamforming Transmitters in 22nm FD-SOI CMOS

Yang Zhang, imec, Heverlee, Belgium

In Paper 26.4, imec presents a sensor in 22nm FDSOI that measures complex reflection coefficients for VSWR values up to 5.7. The sensor costs 0.024mm^2 in die area, 13mW in power consumption, and up to 0.2dB in extra insertion loss.

7:32 AM

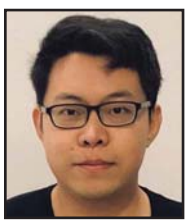


26.5 A Watt-Level Quadrature Switched/Floated-Capacitor Power Amplifier with Back-Off Efficiency Enhancement in Complex Domain Using Reconfigurable Self-Coupling Canceling Transformer

Bingzheng Yang, University of Electronic Science and Technology of China, Chengdu, China

In Paper 26.5, the University of Electronic Science and Technology of China introduces a watt-level quadrature switched/floated-capacitor PA with a hybrid Doherty topology and impedance boosting. The chip achieves 30.3dBm peak output power with 36.5% PAE and efficiency enhancement at 3/6/9/12/15dB PBOs.

7:40 AM



26.6 A 5-to-6GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-Off Efficiency

Aoyang Zhang, University of Southern California, Los Angeles, CA

In Paper 26.6, the University of Southern California describes a current-mode subharmonic switching (SHS) digital-PA architecture for PBO efficiency enhancement. The 65nm CMOS PA achieves P_{sat} of 27dBm and 40.1/29.2% efficiency at peak and -9dB PBO.

7:48 AM

26.7 An Impedance-Transforming N-Path Filter Offering Passive Voltage Gain

Mohammad Khorshidian, Columbia University, New York, NY

In Paper 26.7, Columbia University describes an N-path bandpass filter that combines impedance-transformation and passive voltage amplification. The two-stage (three-stage) design achieves a gain of 15dB (17dB) with maximum OOB rejection of 27dB (33dB).