Session 30 Overview: *Non-Volatile Memories*

MEMORY SUBCOMMITTEE

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A 3D NAND flash memory continues to increase in bit density and performance for both local and cloud data storage applications. The number of WL layers increases to more than 170 layers, up from 96-128 layers presented previously at ISSCC. A floorplanning technique used to put page buffer circuits into a small area under a highly-stacked memory array is shown in paper 30.1. Paper 30.2 and 30.4 present independent multi-plane read techniques to improve random read performance. Paper 30.3 and 30.4 reveal high-speed 2.0Gbps interfaces.

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8:30 AM

30.1 A 176-Stacked 512Gb 3b/Cell 3D-NAND Flash with 10.8Gb/mm² Density with a Peripheral Circuit Under Cell Array Architecture

Jae-Woo Park, SK hynix Semiconductor, Icheon, Korea

In Paper 30.1, SK hynix presents a 176-stacked 512Gb 3b/cell 3D NAND-flash memory that realizes a 10.8Gb/mm² bit density via an optimized floorplan and a high-efficiency charge pump, in addition to, using a peripheral-circuit-under-cell-array architecture. This design achieves a 168MB/s program throughput and a 50us read time.

8:38 AM

30.2 A 1Tb 4b/Cell 144-Tier Floating-Gate 3D-NAND Flash Memory with 40MB/s Program Throughput and 13.8Gb/mm² Bit Density

Ali Khakifirooz, Intel, Santa Clara, CA

In Paper 30.2, Intel shows a 144-tier 1Tb 4b/cell 3D NAND-flash memory with a 13.8Gb/mm² bit density via a CMOS-under-array technique; achieving a 40MB/s program throughput and a 85us read time. Independent multi-plane reads, which double random read performance, and a block-by-deck technique, to reduce block size, are also implemented.

8:46 AM

30.3 A 512Gb 3b/Cell 7th-Generation 3D-NAND Flash Memory with 184MB/s Write Throughput and 2.0Gb/s Interface

Jiho Cho, Samsung Electronics, Seoul, Korea

In Paper 30.3, Samsung presents a 512Gb 3b/cell 3D NAND-flash memory featuring the 7th generation of cell-over-peri (COP) 3D NAND technology; achieving a 184MB/s program throughput and a 40us read time. Low-tapped termination-type circuits that support a 2.0Gbps interface are introduced.

8:54 AM

30.4 A 1Tb 3b/Cell 3D-Flash Memory in a 170+ Word-Line-Layer Technology

Tsutomu Higuchi, KIOXIA, Yokohama, Japan

In Paper 30.4, KIOXIA describes a 170+ stacked 1Tb 3b/cell 3D-flash memory with a 10.4Gb/mm² bit density. An asynchronous and independent plane read is introduced to increase random access performance. An enhanced read scheme and an IO duty-cycle correction technique are introduced to achieve a 50us read time and a 2Gbps IO throughput.