Session 23 Overview: THz Circuits and Front-Ends **RF SUBCOMMITTEE**







steering pixel-array source with the capability to spatially and electronically steer is presented in the second paper. The session continues with an ultra-low power and area THz detector with leading-edge noise performance and concludes with a W-band PLL demonstrating best-in-class

9:15 AM



23.1 270-to-300GHz Double-Balanced Parametric Upconverter Using Asymmetric MOS Varactors and a Power-Splitting-Transformer Hybrid in 65nm CMOS

Zhiyu Chen, University of Texas, Dallas, TX

In Paper 23.1, the University of Texas, Dallas, presents a 270-to-300GHz double-balanced parametric upconverter based on asymmetric MOS varactors and a power-splitting-transformer hybrid in 65nm CMOS. Among upconverters operating near 300GHz, the paper reports the highest conversion gain and 1st-order linearity.

9:23 AM

23.2 A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS

Hossein Jalili, University of California, Davis, CA

In Paper 23.2, the University of California, Davis, presents a reconfigurable lens-integrated 436-to-467GHz radiating source with the peak directivity of 26dBi, 51-to-95mW power consumption, and continuous uninterrupted 2D electronic beam scanning leveraging multiple steering methods. The circuit is capable of supporting high-resolution and fast imaging for THz applications.



9:31 AM

23.3 A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving 2.3pW/ \sqrt{Hz} NEP in 28nm CMOS

Ariane De Vroede, KU Leuven - MICAS, Leuven, Belgium

In Paper 23.3, KU Leuven presents a 605GHz sub-1mW harmonic injection-locked receiver achieving $2.3pW/\sqrt{Hz}$ noise-equivalent power (NEP) in a 28nm CMOS process. The paper introduces a new approach for THz detection with the lowest published NEP for CMOS detectors operating above 500GHz.

23



9:39 AM

23.4 An 82fs_{rms}-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector in 65nm CMOS

Suneui Park, KAIST, Daejeon, Korea

In Paper 23.4, KAIST presents a PLL that can directly generate an ultra-low-jitter W-band signal. The 65nm-CMOS 102GHz W-band PLL uses a gated injection-locked frequency-multiplier-based phase detector to achieve 82fs_{rms} jitter.