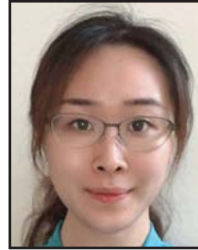
F5: *Enabling New System Architectures with 2.5D, 3D, and Chiplets*

Organizers:

Christopher Gonzalez
IBM, Yorktown Heights, NY



Huichu Liu
Facebook, Menlo Park, CA

Committee: **Mijung Noh,** *Samsung Electronics, Hwaeong-si, Gyeonggi-do, Korea*
Eric Karl, *Intel, Portland, OR*
Thomas Toifl, *Cisco Systems, Wallisellen, Switzerland*
Shawn Hsu, *National Tsing Hua Univeristy, Hsinchu, Taiwan*

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365834

The end of transistor scaling drives innovative 2.5D, 3D and chiplet technologies to further extend Moore's law. Recent advancements in multi-die integration effectively reduce the costs at advanced nodes while providing more flexibility, modularity and heterogeneous integration, which require designers to rethink the system architectures to exploit these advantages. This forum focuses on the most recent advancements of the 2.5D, 3D and chiplet technologies as well as the key components for integration to enable new system architectures. This forum aims to bring together technologists, designers and architects from industry and academia to discuss the practical challenges and solutions in 2.5D/3D technologies, and to provide insights on how to leverage the technology benefits with different system requirements. The forum starts with an overview of foundry solutions on 2.5D, 3D and chiplets technologies, followed by deep dive topics inspired by application focuses. For example, FPGA with 2.5D/3D heterogeneous integration has emerged with promising data-centric applications. High-bandwidth memory (HBM) has been widely adopted in commercial processors, and yet advanced integration techniques and design strategies remain the key to overcome the practical challenges to satisfy power density and performance requirements. Recent advancements in chiplets rapidly evolves the design space in SoC, driving both cost reduction and modularity. Meanwhile, design considerations to address power delivery, signaling, and thermal challenges at the circuit level as well as advanced heterogeneous integration at the process level have attracted research interests and innovations to further improve the system-level efficiency and reliability in the multi-chip stacking era. Co-optimization of high-speed serial links with 2.5D/3D technologies plays another essential role to continuously improve off-chip communication and system performance. Moreover, driven by the growth of edge computing and advanced 3D stacking empowers sensor integration for latency reduction with near-sensor intelligence. Finally, the forum concludes with a hierarchical view of the 3D interconnect technology landscape and long-term roadmap, shedding light on future technology directions.

Foundry Solutions for 2.5D/3D Integration

Douglas Yu, *TSMC, HsinChu, Taiwan*

Industry needs advanced packaging solutions to optimize system performance, power efficiency, form-factor/profile and cost-effectiveness for various applications. Leading foundries provide disruptive platform technology with new process modules and integration flows to realize the most advanced chiplet stacking to achieve best system PPAC. These platform solutions have good flexibility and synergy so that they can mutually leverage for design and manufacturing among the various applications. We will also discuss the foundry 2.5D/3D integration roadmap to align the R&D of academia, research institutes and industry supply chain (process/design tools, materials, etc.) for commercialization.

Dr. Doug Yu is a vice president of TSMC R&D, currently responsible for the development of advanced integrated interconnect & packaging technologies. He has been in charge of on-chip interconnects (Cu/Low-K and Cu/ELK), and TSMC 3DFabricTM (WLSI technologies including CoWoS®, InFO and SoICTM, etc.) technology developments. TSMC IC interconnects and advanced packaging technologies set new technology standards and start new trends for the semiconductor industry. Doug worked with AT&T Bell Labs previously. He received his Ph.D. in materials engineering from the Georgia Institute of Technology. Dr. Yu is an IEEE Fellow in recognition of his leadership in IC interconnect technology development. He was awarded the President Science Prize, Taiwan's highest science and technology honor. Doug has been granted 1,100+ US patents as (co)authors. He also has numerous technical publications, plus plenary, keynote and invited speeches in leading international conferences, and several semiconductor book chapters.

New Directions in 2.5D/3D Heterogeneous Integration of FPGAs

Farhana Sheikh, *Intel, Portland, OR*

This talk presents 2.5D and 3D-HI FPGAs and chiplets leveraging Intel's EMIB/Foveros technologies with a focus on emerging applications. We present FPGA-based sub-THz systems that can leverage nano-/micro-/macro-3D HI. We leverage our previous research in 2.5D FPGA-chiplet integration to forge a path towards new 3D-FPGA platforms. Challenges in packaging, power delivery, design, and thermals are outlined; and we present opportunities to standardize die-to-die interfaces for 3D-HI of IPs.

Farhana Sheikh has a Ph.D. in EECS from UC Berkeley 2008, and has worked in FW, SW, embedded system design prior to her PhD. Farhana joined Intel in 2008 as a senior researcher in digital circuits for cryptography, graphics, wireless, 2D/3D heterogeneous integration, sub-THz distributed/non-distributed massive MIMO circuits and architectures, high-frequency wireless control for quantum computers, adaptive and deep-learning based circuits/architectures for next generation intelligent wireless systems, and cryogenic CMOS circuits with 48 published papers, 22 patents, and multiple awards including two ISSCC Best Paper Awards in 2012 and 2019. Farhana is the IEEE SSCS Oregon Chapter Chair, and holds TPC positions in multiple SSCS conferences.

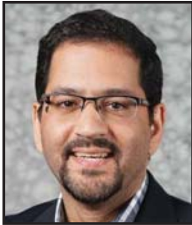
3D-Stacked Memory Architecture with 2.5D Heterogenous Integration

Kyomin Sohn, *Samsung, Hwasung-City, Korea*

HBM DRAM provides unparalleled high bandwidth by wide IO utilizing 3D-stacked DRAM with TSV technology. However, there are challenges like power density, thermal dissipation, testability and reliability in 2.5D integration. In this talk, various 2.5D/3D integration techniques are introduced such as chip partitioning, die-to-die interfaces, TSV signaling, power delivery, and thermal considerations. Design strategy for power-efficiency, performance, testability and reliability are also discussed.

Kyomin Sohn received the B.S. and M.S. degrees in Electrical Engineering in 1994 and 1996, respectively, from Yonsei University, Seoul. From 1996 to 2003, he was with Samsung Electronics, Korea, involved in the SRAM Design Team. He designed various kinds of high-speed SRAM. He received the Ph.D. degree in EECS in 2007 from KAIST, Korea. He rejoined Samsung Electronics in 2007, where he has been involved in the DRAM Design Team. He is a Master (technical VP) in Samsung and he is responsible for the future architecture and circuit technology of DRAM. His interests include 3D-DRAM, reliable memory design, and processing-in-memory. In addition, he has currently served as a technical program committee member of the Symposium on VLSI Circuits since 2012.

 978-1-7281-9549-0/21/$31.00 ©2021 IEEE



2.5D and 3D Polylithic Integrated Circuit Technologies

Muhannad S. Bakir, *Georgia Tech, Atlanta, GA*

Monolithic ICs have progressed at an unprecedented rate of innovation in the past ~60 years. But, with Moore's Law slowing down, 'polylithic' integration of heterogeneous ICs (or chiplets) is projected to be a key driver for performance, power, and cost in the next era of Moore's Law. This presentation will first discuss polylithic integration approaches using 2.5D and 3D IC technologies and their advantages. Design considerations and benchmarking of power delivery, signaling, and thermal are described. Second, passive self-alignment and assembly approach for optical fibers for 2.5D ICs is demonstrated using a combination of silicon micromachining and 3D printing to achieve efficient and accurate near-vertical coupling to a silicon-on-insulator (SOI) substrate with monolithic ridge waveguides and grating couplers. The alignment process is repeatable and the peak efficiency is comparable to the active fiber alignment efficiency. Third, we demonstrate embedded microfluidic cooling in 2.5D/3D ICs along with coaxial TSV integration approaches to enable dense 2.5D/3D electronics with no thermal limits; silicon microfluidic cooling demonstrations will be shown using active chips.

Muhannad S. Bakir is the Dan Fielder Professor in the School of Electrical and Computer Engineering at Georgia Tech. Dr. Bakir. His research group has received more than thirty conference and student paper awards including six from the IEEE Electronic Components and Technology Conference (ECTC), four from the IEEE International Interconnect Technology Conference (IITC), and one from the IEEE Custom Integrated Circuits Conference (CICC). Dr. Bakir's group was awarded 2014 and 2017 Best Papers of the IEEE Transactions on Components Packaging and Manufacturing Technology (TCPMT). Dr. Bakir is the recipient of the 2013 Intel Early Career Faculty Honor Award, 2012 DARPA Young Faculty Award, 2011 IEEE CPMT Society Outstanding Young Engineer Award, and was an invited participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. Dr. Bakir is the recipient of the 2018 IEEE Electronics Packaging Society (EPS) Exceptional Technical Achievement Award "for contributions to 2.5D and 3D IC heterogeneous integration, with focus on interconnect technologies." He is also the co-recipient of the 2018 McKnight Foundation Technological Innovations in Neuroscience Awards. In 2020, Dr. Bakir was the recipient of the Georgia Tech Outstanding Doctoral Thesis Advisor Award. Dr. Bakir serves on the editorial board of IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT) and IEEE Transactions on Electron Devices (TED). Dr. Bakir serves as a Distinguished Lecturer for IEEE EPS.

MCM/Chiplet Solutions

Samuel Naffziger, *AMD, Fort Collins, CO*

Chiplet architecture has many benefits in enabling lower costs from smaller die combined with modularity to scale performance and configuration. The costs of splitting and modularizing an SOC into chiplets will be discussed, which include the need for high-bandwidth and low-latency communication between dies, overheads of testing and power-managing what used to be individual SOC modules as standalone chips, and engineering the package substrate to provide routing and power delivery resources.

Samuel Naffziger is AMD senior vice president, Corporate Fellow, and Product Technology Architect. Naffziger works across the company to optimize product technology choices and deployment with a continued focus on driving best practice power/performance/area methodology to maximize product competitiveness, efficiency, and cost.

Naffziger has been the lead innovator behind many of AMD's low-power features and chiplet architecture. He has over 32 years of industry experience with a background in microprocessors and circuit design at Hewlett Packard, Intel and AMD.

Naffziger received a Bachelor of Science degree in Electrical Engineering from the California Institute of Technology (CalTech) and a Master of Science from Stanford. Naffziger holds more than 130 U.S. patents in the field and authored dozens of publications and presentations on processors, architecture and power management. He is an IEEE Fellow.

High-Speed Interconnect Challenges within Systems Leveraging Advanced Packaging Techniques

Walker Turner, *NVIDIA, Raleigh-Durham, NC*

The end of Moore's Law requires high-performance computational systems to leverage architectural and system-level improvements in conjunction with advanced packaging techniques to continue increasing computational performance to meet market demands. The high-speed serial links that interconnect these systems are a key enabler to this continued performance increase but can no longer rely on the transistor-speed scaling that comes from porting old designs into newer technology nodes to meet ever-increasing bandwidth requirements. The use of advanced packaging techniques, such as 2.5D, 3D, and chiplet technologies, impose several challenges on the design of these interconnects, which must operate at data-rates high enough to approach the on-chip bisection bandwidth while consuming a fraction of total system power. While improvements to package manufacturability will help to increase channel bandwidths, future serial links will require solutions that leverage a co-optimization of both the high-speed circuitry and the signaling channel along with more advanced signaling techniques.

Dr. Turner received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville, in 2009, 2012, and 2015, respectively. In 2014, he was a contractor with the U.S. Army Research Laboratory in Adelphi, Maryland, developing wirelessly powered systems and integrated low-noise amplifiers for piezoelectric E-field sensors. Since 2015, he has been with the Circuits Research Group at NVIDIA Inc. in Durham, North Carolina, where he currently works as a Senior Research Scientist on energy-efficient, high-speed signaling systems for on- and off-chip communication. He also joined North Carolina State University, Raleigh, as a Teaching Assistant Professor in 2019, where he instructs an undergraduate microelectronics engineering course.

Evolving Image Sensor Architecture through Stacking Devices

Yusuke Oike, *Sony, Kanagawa, Japan*

The evolution of CMOS image sensors and the prospects utilizing advanced imaging technologies promise to improve our quality of life. This talk introduces the contribution of stacking technologies for accelerating drastic performance improvements and for integrating edge computing connected to the sensor layer. Furthermore, the fine pitch connection between the pixel and logic layers is making the pixel parallel circuit architecture practical for the next evolution.

Dr. Yusuke Oike joined Sony Corporation, where he was involved in research and development of architectures, circuits and devices for image sensors, after he received Ph.D. degree in electronic engineering from the University of Tokyo in 2005. From 2010 to 2011, he was a Visiting Scholar at Stanford University. Currently he is responsible for developing CMOS image sensors at Sony Semiconductor Solutions. His research interests include pixel architecture, mixed-signal circuit design for image sensors and image processing algorithms. He was a TPC member of ISSCC from 2012 to 2016, and he currently serves as the Program Chair of VLSI Symposium on Circuits 2021.

3D System Integration: Technology Landscape and Long-Term Roadmap

Eric Beyne, *IMEC, Leuven, Belgium*

As electronic systems become more complex and CMOS scaling becomes more specialized, a variety of heterogenous device technologies will be required to realize them. The highly successful system-on-chip (SOC) design methodology of complex systems will need to evolve to effectively become a “3D-SOC” heterogeneous system design methodology. This requires a functional partitioning of the systems in separate die (“chiplets”) that require high bandwidth, low latency, and low energy 2.5D and 3D integration technologies to “reconstitute” the systems. A broad range of possible technologies are available to realize this. Proposing a hierarchical view of the 3D interconnect fabric, we define a 3D interconnect technology landscape, that extends from the package-level all the way to the transistor level, spanning eight orders of magnitude in 3D interconnect density. This Landscape is highly dynamic, as each technology has its own roadmap and scaling roadmap. This presentation will cover the main technology contenders and discuss their projected roadmap. Technology elements such as laminate interposers, Si interposers, through-silicon via technologies, solder microbumping, and hybrid wafer-to-wafer or die-to-wafer bonding will be discussed.

Eric Beyne obtained a degree in electrical engineering in 1983 and the Ph.D. degree in Applied Sciences in 1990, both from the Katholieke Universiteit Leuven, Belgium. Since 1986, he has been with imec in Leuven, Belgium, where he has worked on advanced packaging and 3D interconnect technologies. Dr. Beyne is currently imec Senior Fellow, VP R&D, and Program Director of imec’s 3D System Integration program.

 978-1-7281-9549-0/21/$31.00 ©2021 IEEE