Session 11 Overview:
Advanced Wireline Links and Techniques

WIRELINE SUBCOMMITTEE

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2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365823

High-performance SerDes with both high area efficiency (mm²/lane) and energy efficiency (pJ/b) are driven by the ever-increasing demands of bandwidth and capacity in data centers. They also enable chiplets, multi-die, and silicon-photonics integration for a low cost, high yield, and high throughput solution. Besides, low-power SerDes is essential to overall system power savings by reducing the power overhead and cost for cooling. This session introduces advanced wireline techniques that support both high-speed and energy-efficient data transmission over electrical, fiber, and dielectric waveguide channels. The first three papers of the session describe short-reach power- and density-optimized transceivers in state-of-the-art 7nm FinFET technology. The next two describe low-power clock generators for high-speed transceivers. The remaining four papers of the session focus on design solutions to enable future high-speed link scaling, including optical and dielectric waveguides, ultra-low power CDRs, and the potential for >50Gb/s simultaneous, bidirectional signaling over high-loss channels.

7:00 AM

11.1 A 1.7pJ/b 112Gb/s XSR Transceiver for Intra-Package Communication in 7nm FinFET Technology

Ramy Yousry, MediaTek, Irvine, CA

In Paper 11.1, MediaTek describes a short-reach (XSR) PAM-4 transceiver operating at 112Gb/s with 1.7pJ/bienergy efficiency. It features a delay-line based continuous-time linear equalizer and automatic calibration algorithms for performance optimization and low power operation.

7:08 AM

11.2 A 26.5625-to-106.25Gb/s XSR SerDes with 1.55pJ/b Efficiency in 7nm CMOS

Ravi Shivnaraine, Rambus, Toronto, Canada

In Paper 11.2, Rambus shows an eight-lane 106.25Gb/s/lane XSR SerDes macro aimed at enabling co-packaged optics. The corresponding beachfront throughput is 722Gb/s/mm and energy efficiency is 1.55pJ/b.

7:16 AM

11.3 A 480Gb/s/mm 1.7pJ/b Short-Reach Wireline Transceiver Using Single-Ended NRZ for Die-to-Die Applications

Scott D. Huss, Cadence, Cary, NC

In Paper 11.3, Cadence proposes a short-reach single-ended signaling macro that uses spatial 6b/7b encoding to minimize ground reference noise. The link operates at 40Gb/s/pin with a 1.7pJ/b energy efficiency and provides 480Gb/s/mm bandwidth density.

7:20 AM

11.4 A High-Accuracy Multi-Phase Injection-Locked 8-Phase 7GHz Clock Generator in 65nm with 7b Phase Interpolators for High-Speed Data Links

Zhaowen Wang, Columbia University, New York, NY

In Paper 11.4, Columbia University describes a 7b phase interpolator (PI) using a quadrature delay line coupled with a multi-phase injection-locked ring oscillator. The measured linearity of the PI is 1.76LSB INLpp and 1.13LSB DNLpp at 7GHz, which can be utilized in low-jitter high-phase-accuracy clock and data recovery.

7:24 AM

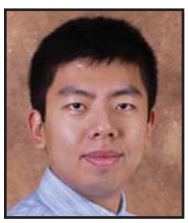
11.5 A 23.9-to-29.4GHz Digital LC-PLL with a Coupled Frequency Doubler for Wireline Applications in 10nm FinFET

Dongseok Shin, Intel, Hillsboro, OR

In Paper 11.5, Intel presents a digital PLL with a current-reuse LC-DCO coupled into a frequency doubler. A frequency tracking loop is proposed to optimize phase noise performance across 23.9-29.4GHz, and it achieves a 65fs$_{rms}$ random jitter at a transmitter output after a 1st-order 4MHz-BW CDR.

11

7:32 AM



11.6 A 100Gb/s -8.3dBm-Sensitivity PAM-4 Optical Receiver with Integrated TIA, FFE and Direct-Feedback DFE in 28nm CMOS

Hao Li, Intel, Hillsboro, OR

In Paper 11.6, Intel demonstrates a single chip 100Gb/s PAM-4 optical receiver in a 28nm bulk CMOS process. It employs a 2-tap FFE and 2-tap direct feedback DFE to achieve -8.3dBm optical sensitivity at 2.4E-4 BER.

7:40 AM

11.7 A 56Gb/s 50mW NRZ Receiver in 28nm CMOS

Atharav Atharav, University of California, Los Angeles, CA

In Paper 11.7, UCLA demonstrates a high-performance NRZ CDR combined with a high-pass feedforward CTLE and a dual loop DFE in 28nm CMOS technology. It is capable of equalizing 25dB channel loss at 28GHz while providing a bathtub eye opening of 0.4UI at BER<1E-12.

7:48 AM

11.8 An Echo-Cancelling Front-End for 112Gb/s PAM-4 Simultaneous Bidirectional Signaling in 14nm CMOS

Ramin Farjadrad, Marvell, Santa Clara, CA

In Paper 11.8, Marvell demonstrates a TX signal and echo cancellation scheme to enable simultaneous bidirectional signaling across a lossy channel at up to 56Gb/s PAM-4 in each direction, or 112Gb/s aggregate per channel. A novel analog hybrid canceler suppresses the TX signal and its dominant reflections by 26dB across the 14GHz signal band.

7:56 AM

11.9 A 105Gb/s Dielectric-Waveguide Link in 130nm BiCMOS Using Channelized 220-to-335GHz Signal and Integrated Waveguide Coupler

Jack W. Holloway, Massachusetts Institute of Technology, Cambridge, MA and Raytheon, Tewksbury, MA

In Paper 11.9, MIT shows a 105Gb/s link operating over a 30cm-long dielectric ribbon waveguide. The link, implemented in 130nm BiCMOS, modulates and demodulates data across three channels covering a 220-to-340GHz frequency band with each channel carrying 35Gb/s.