Session 24 Overview: *Advanced Embedded Memories*

MEMORY SUBCOMMITTEE

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Advancements in embedded memories continue to enable improvements in system designs spanning from automotive to high-performance computing markets. SRAM continues to be a critical technology enabler across the full spectrum of the semiconductor industry. RRAM has emerged as a promising technology for scaling embedded non-volatile memory into advanced nodes; with applications in consumer electronics, self-driving vehicles, intelligent edge devices and more. This session details recent advancements in SRAM and RRAM technology and circuits. The first paper describes an ultra-high-performance and low-power sensing technique for single-ended 8T SRAM arrays. The second paper outlines a state-of-the-art RRAM reporting record bit density. The third paper showcases a GAA SRAM design and its supporting assist circuitry. The final paper outlines a standard-cell based SRAM design for small macros: demonstrating high-performance and ultra-low operating voltages.

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7:00 AM

24.1 A 6.2 GHz Single Ended Current Sense Amplifier (CSA) Based Compileable 8T SRAM in 7nm FinFET Technology

Alexander Fritsch, IBM, Boeblingen, Germany

In Paper 24.1, IBM describes a single-ended current-sense amplifier implemented for an 8T SRAM array with 7nm FinFETs. The array operates at 6.2GHz from a 1.0V supply and at 2GHz from a 0.5V supply, while saving 10-12% of power compared to conventional domino read circuits.

7:08 AM

24.2 A 14nm-FinFET 1Mb Embedded 1T1R RRAM with a 0.022μm² Cell Size Using Self-Adaptive Delayed Termination and Multi-Cell Reference

Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China and Zhejiang Lab, Hangzhou, China

In Paper 24.2, the Chinese Academy of Sciences presents a 14nm FinFET 1Mb RRAM with the smallest published bitcell size of 0.022um². A new self-adaptive delayed termination (SADT) write scheme improves the creation of robust conductive filaments and enables up to an 87% reduction in R_{ON} related failures.

7:16 AM

24.3 A 3nm Gate-All-Around SRAM Featuring an Adaptive Dual-BL and an Adaptive Cell-Power Assist Circuit

Taejoong Song, Samsung Electronics, Hwaseong, Korea

In Paper 24.3, Samsung demonstrates a 3nm Gate-All-Around SRAM featuring improved ADBL and ACP circuit assists to increase cell operating margins. ADBL and ACP combine to improve minimum operating voltage by 230mV, based on results from a GAA SRAM testchip.

7:24 AM

24.4 A 5nm 5.7GHz@1.0V and 1.3GHz@0.5V 4kb Standard-Cell-Based Two-Port Register File with a 16T Bitcell with No Half-Selection Issue

Hidehiro Fujiwara, TSMC, Hsinchu, Taiwan

In Paper 24.4, TSMC presents a 5nm standard-cell based 16T SRAM macro targeted for small capacity macro applications with improved integration to memory periphery circuits. A 4kb array with this implementation achieves 5.7GHz operation from a 1.0V supply, with a minimum operating voltage floor of 0.35V.