Session 13 Overview: *Cryo-CMOS for Quantum Computing*

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

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Cryogenic CMOS (cryo-CMOS) support of quantum processors is becoming a necessity to ensure the continuous growth of qubit count, so as to achieve scalable, fault-tolerant quantum computers. The first paper of the session describes an integrated controller for spin qubits that performs state manipulation, readout, and gate pulsing fabricated in 22nm FinFET CMOS technology. The second paper presents a fully integrated SoC for spin qubit interface based on RF reflectometry of quantum dots, all implemented in 40nm CMOS technology, for scalable quantum systems operating at 3.5K. The third paper also focuses on scalable RF based readout of spin qubits for a record 0.17mW/qubit power requirement, operating at 4.2K. The fourth paper proposes a 1GS/s A/D converter for low-power digitization of the signal measured from a qubit readout that achieves a FOM of 15fJ/conv.-step at 4K.

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7:45 AM

13.1 A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology

Jong-Seok Park, Intel, Hillsboro, OR

In Paper 13.1, Intel describes an integrated control/readout SoC to drive up to 16 qubits and read up to 6 qubits, and pulse up to 22 gates simultaneously. The chip, fabricated in 22nm FinFET technology, operates at 4K.

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13.2 A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Andrea Ruffino, EPFL, Neuchâtel, Switzerland

In Paper 13.2, EPFL presents a cryo-CMOS SoC for the readout of spin qubits based on an intermediate-IF I/Q receiver with frequency synthesizer operating at 5-to-6.5GHz with a 70dB gain and 0.55dB noise figure. The chip allows to read up to 70 qubits dissipating 1.5mW/qubit.

8:01 AM

13.3 A 6-to-8GHz 0.17mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40nm CMOS Technology

Bagas Prabowo, Delft University of Technology, Delft, The Netherlands and QuTech, Delft, The Netherlands

In Paper 13.3, Delft University of Technology proposes a cryo-CMOS readout chip for spin qubits, achieving 58dB gain and 0.6dB noise figure, all at 4.2K.

8:09 AM

13.4 A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Gerd Kiene, Delft University of Technology, Delft, The Netherlands and QuTech, Delft, The Netherlands

In Paper 13.4, Delft University of Technology presents an A/D conversion applied to measurements of qubits after readout. The proposed 1GS/s ADC achieves 36.2dB SNDR at 4K, supporting multiple qubit readout at less than 0.5mW/qubit.