Session 35 Overview:
Adaptive Digital Techniques for Variation Tolerant Systems
DIGITAL CIRCUITS SUBCOMMITTEE

Session Chair:
Arijit Raychowdhury
Georgia Institute of Technology
Atlanta, GA

Session Co-Chair:
Mijung Noh
Samsung Electronics, Korea

Session Moderator:
Keith Bowman
Qualcomm, Raleigh, NC

Processors continue to improve energy efficiency through an integration of on-die sensors, real-time adaptation and closed-loop software management. The three papers in this session exemplify techniques that demonstrate such improvements on large-scale processors. In commercial 7nm processors from MediaTek and Qualcomm, the authors demonstrate 13% power and 11% performance improvements, respectively. Dolphin Design and collaborators demonstrate an adaptive body-biasing technique in 22nm FDSOI technology realizing a 30% power reduction.

35.1   An Octa-Core 2.8/2GHz Dual-Gear Sensor-AssistedHigh-Speed and Power-Efficient CPU in 7nm FinFET 5G Smartphone SoC

Bo-Jr Huang, MediaTek, Hsinchu, Taiwan

In Paper 35.1, MediaTek introduces several sensor-assisted guard-band reduction techniques applied on a 7nm Octa-Core processor. With sensor assistance, the CPU operates at 2.8GHz with 13% reduction in power in a fully integrated 5G multi-mode smartphone SoC that supports the sub-6GHz band with 2.6Gbps upload and 4.7Gbps download speeds.

35.2   A 0.021mm² PVT-Aware Digital-Flow-Compatible Adaptive Back-Biasing Regulator with Scalable Drivers Achieving 450% Frequency Boosting and 30% Power Reduction in 22nm FDSOI Technology

Andrea Bonzo, Dolphin Design, Meylan, France

In Paper 35.2, Dolphin Design in collaboration with CEA-Leti and GlobalFoundries demonstrate a PVT-aware, adaptive and scalable back-biasing regulator in 22nm FDSOI technology. Statistical analysis is carried out on 316 dies and the proposed technique brings up to 30% power reduction by decreasing the minimal power supply by 100mV, while maintaining the target operating frequency (50MHz).

35.3   Thread-Level Power Management for a Current- and Temperature-Limiting System in a 7nm Hexagon Processor

Vijay Kiran Kalyanam, Qualcomm, Austin, TX

In Paper 35.3, Qualcomm presents a thread-level power management (TPM) technique in a 7nm Hexagon processor. TPM exploits low-power phases during thread execution to appropriately adjust the thread instruction issue to achieve a higher performance at a target power as compared to global throttling. Silicon measurements demonstrate an 11% higher performance for a multi-threaded machine-learning application.

35